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1 Description and block circuit diagram

1.1 Description

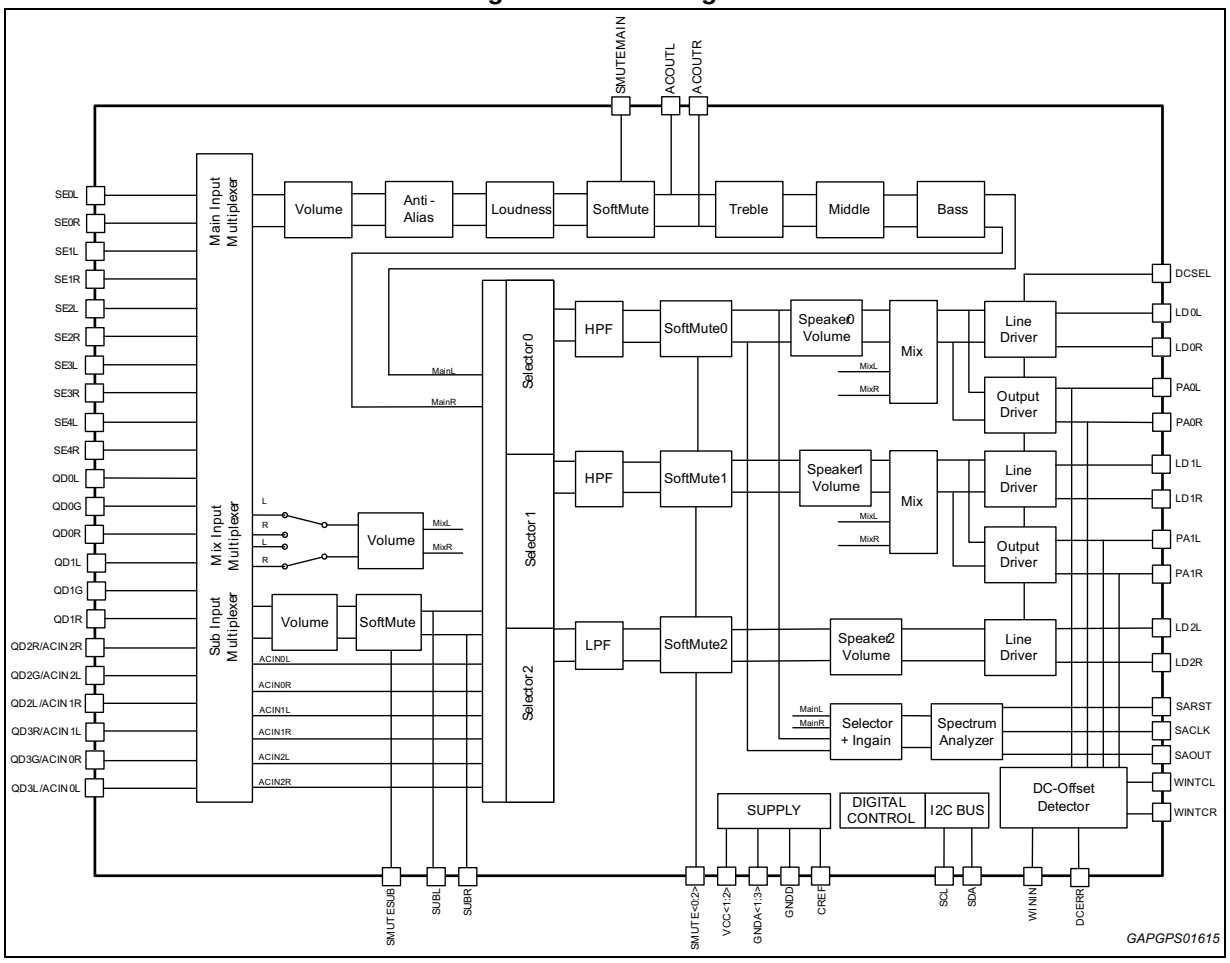
The TDA7715 is a high performance signal processor specifically designed for car radio applications.

The device includes a high performance audio processor with fully integrated audio filters and new soft-step architecture.

The digital control allows programming in a wide range of filter characteristics.

1.2 Block circuit diagram

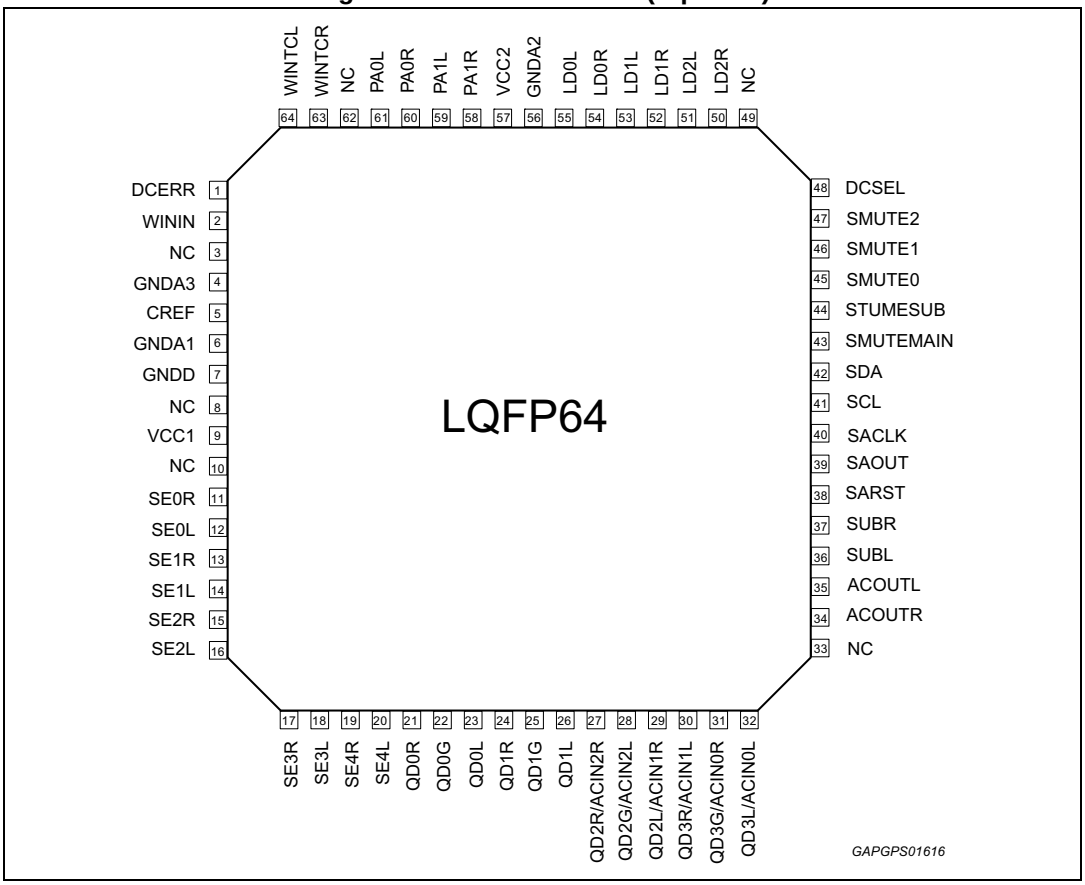
Figure 1. Block diagram



2 Pins connection and description

2.1 Pins connection

Figure 2. Pins connection (top view)



2.2 Pins description

Table 2. Pins description

N#	Pin name	Description	I/O
1	DCERR	DC offset detector output	O
2	WININ	DC offset detector input	I
3	NC	No connected	NC
4	GNDA3	Analog Ground	S
5	CREF	Reference capacitor	O
6	GNDA1	Analog Ground	S
7	GNDD	Digital Ground	S
8	NC	No connected	NC

Table 2. Pins description (continued)

N#	Pin name	Description	I/O
9	VCC1	Supply	S
10	NC	No connected	NC
11	SE0R	Single-end input right	I
12	SE0L	Single-end input left	I
13	SE1R	Single-end input right	I
14	SE1L	Single-end input left	I
15	SE2R	Single-end input right	I
16	SE2L	Single-end input left	I
17	SE3R	Single-end input right	I
18	SE3L	Single-end input left	I
19	SE4R	Single-end input right	I
20	SE4L	Single-end input left	I
21	QD0R	Quasi-differential stereo inputs right	I
22	QD0G	Quasi-differential stereo inputs common	I
23	QD0L	Quasi-differential stereo inputs left	I
24	QD1R	Quasi-differential stereo inputs right	I
25	QD1G	Quasi-differential stereo inputs common	I
26	QD1L	Quasi-differential stereo inputs left	I
27	QD2R/ACIN2R	Quasi-differential stereo inputs right or ac-coupling input	I
28	QD2G/ACIN2L	Quasi-differential stereo inputs common or ac-coupling input	I
29	QD2L/ACIN1R	Quasi-differential stereo inputs left or ac-coupling input	I
30	QD3R/ACIN1L	Quasi-differential stereo inputs right or ac-coupling input	I
31	QD3G/ACIN0R	Quasi-differential stereo inputs common or ac-coupling input	I
32	QD3L/ACIN0L	Quasi-differential stereo inputs left or ac-coupling input	I
33	NC	No connected	NC
34	ACOUTR	AC coupling output, right channel	O
35	ACOUTL	AC coupling output, left channel	O
36	SUBL	Sub channel output left	O
37	SUBR	Sub channel output right	O
38	SARST	Spectrum analyzer reset	I
39	SAOUT	Spectrum analyzer analog voltage output	O
40	SACLK	Spectrum analyzer clock input	I
41	SCL	I^2C bus clock	I
42	SDA	I^2C bus data	I/O
43	SMUTEMAIN	External mute pin for main channel	I

Table 2. Pins description (continued)

N#	Pin name	Description	I/O
44	SMUTESUB	External mute pin for sub channel	I
45	SMUTE0	External mute pin for speaker, signal path 0	I
46	SMUTE1	External mute pin for speaker, signal path 1	I
47	SMUTE2	External mute pin for speaker, signal path 2	I
48	DCSEL	Output DC level select	I
49	NC	No connected	NC
50	LD2R	Line driver output right	O
51	LD2L	Line driver output left	O
52	LD1R	Line driver output right	O
53	LD1L	Line driver output left	O
54	LD0R	Line driver output right	O
55	LD0L	Line driver output left	O
56	GNDA2	Analog Ground	S
57	VCC2	Supply	S
58	PA1R	Out-section rear output, right channel	O
59	PA1L	Out-section rear output, left channel	O
60	PA0R	Out-section front output, right channel	O
61	PA0L	Out-section front output, left channel	O
62	NC	No connected	NC
63	WINTCR	DC offset detector filter output right channel	O
64	WINTCL	DC offset detector filter output left channel	O

3 Electrical specifications

3.1 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-to-ambient	50	°C/W

3.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Operating supply voltage	13	V
V_{in_max}	Maximum voltage for signal input pins	7	V
T_{amb}	Operating ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

3.3 Electrical characteristics

V_{CC} = 11.5 V; T_{amb} = 25 °C; R_L = 10 kΩ; all gains = 0 dB; f = 1 kHz; Input = SE1; Output = PAout; unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply						
V_{cc}	Supply voltage	-	7.5	11.5	12.5	V
Is	Supply current	-	48	55	62	mA
Input selector						
R_{IN}	Input resistance	All single ended inputs	70	100	130	kΩ
V_{CL}	Clipping level	Input Gain = 0 dB, THD = 1%	-	2	-	V_{RMS}
S_{IN}	Input separation	-	80	100	-	dB
Differential stereo inputs						
R_{in}	Input resistance	Differential	70	100	130	kΩ
CMRR	Common mode rejection ratio for main source	V_{CM}=1 V_{RMS} @ 1 kHz	46	60	-	dB
		V_{CM}=1 V_{RMS} @ 10 kHz	46	60	-	dB
Loudness control						
A_{MAX}	Max attenuation (1)	-	14	15	16	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A_{STEP}	Step resolution (1)	-	0.5	1	1.5	dB
f_{Peak}	Peak frequency (2)	f_{P1}	-	400	-	Hz
		f_{P2}	-	800	-	Hz
		f_{P3}	-	2400	-	Hz
Volume control						
G_{MAX}	Max gain (1)	-	21	23	25	dB
A_{MAX}	Max attenuation (1)	-	-26	-23	-20	dB
A_{STEP}	Step resolution (1)	-	0.5	1	1.5	dB
E_A	Attenuation set error	G = -23 to +23 dB	-1.5	0	1.5	dB
E_T	Tracking error	Gain difference of left/right	-	-	0.8	dB
V_{DC}	DC steps	Adjacent attenuation steps	-	0.1	3	mV
		Adjacent gain steps	-	0.5	5	mV
Soft-step						
T_{SS}	Soft step time	T_1	5	7.5	12.5	ms
		T_2	10	15	25	ms
Soft-mute						
A_{MUTE}	Mute attenuation	-	80	100	-	dB
T_{D1}	Delay time (main & sub channel)	T_1	0.4	0.5	0.6	ms
		T_2	3	4	5	ms
		T_3	6	8	10	ms
		T_4	14	16	18	ms
T_{D2}	Delay time (speaker)	T_1	3	4	5	ms
		T_2	6	8	10	ms
		T_3	29	32	35	ms
		T_4	60	64	68	ms
V_{TH_Low}	Low threshold for MUTE pin (3)	-	-	-	0.8	V
V_{TH_High}	High threshold for MUTE pin (3)	-	2.4	-	-	V
RPU	Internal pull-up resistor for MUTE Pin	-	25	45	65	kΩ
VPU	Internal pull-up Voltage for MUTE Pin	-	3.1	3.3	3.5	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Bass control						
Fc	Center frequency (2)	f_{C0}	-	60	-	Hz
		f_{C1}	-	70	-	Hz
		f_{C2}	-	80	-	Hz
		f_{C3}	-	100	-	Hz
		f_{C4}	-	110	-	Hz
		f_{C5}	-	120	-	Hz
		f_{C6}	-	130	-	Hz
		f_{C7}	-	150	-	Hz
Q_{BASS}	Quality factor (2)	Q_1	-	1	-	-
		Q_2	-	1.25	-	-
		Q_3	-	1.5	-	-
		Q_4	-	2	-	-
C_{RANGE}	Control range (1)	-	±14	±15	±16	dB
A_{STEP}	Step resolution (1)	-	0.5	1	1.5	dB
DC_{GAIN}	Bass DC gain (1)	DC = off	-1	0	+1	dB
		DC = on, Gain= 14 dB	3.5	4.4	5.5	dB
Middle control						
C_{RANGE}	Control range (1)	-	±14	±15	±16	dB
A_{STEP}	Step resolution (1)	-	0.5	1	1.5	dB
Fc	Center frequency (2)	f_{C1}	-	500	-	Hz
		f_{C2}	-	1	-	kHz
		f_{C3}	-	1.5	-	kHz
		f_{C4}	-	2	-	kHz
Q_{Middle}	Quality factor (2)	Q_1	-	1	-	-
		Q_2	-	2	-	-
Treble control						
C_{RANGE}	Control Range (1)	-	±14	±15	±16	dB
A_{STEP}	Step Resolution (1)	-	0.5	1	1.5	dB
Fc	Center frequency (2)	f_{C1}	-	10	-	kHz
		f_{C2}	-	12.5	-	kHz
		f_{C3}	-	15	-	kHz
		f_{C4}	-	17.5	-	kHz

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
AC coupling						
R_{IN}	Input resistance	AC inputs	70	100	130	kΩ
V_{CL}	Clipping level	flat, THD = 1%	-	2	-	V_{RMS}
R_{OUT}	Output impedance	AC outputs	-	30	100	Ω
Speaker volume						
G_{MAX}	Max gain (1)	-	22	23	24	dB
A_{MAX}	Max attenuation (1)	-	-85	-79	-73	dB
A_{STEP}	Step resolution (1)	-	0.5	1	1.5	dB
A_{MUTE}	Mute attenuation	-	80	90	-	dB
E_E	Attenuation set error	G = -20 to +15 dB	-1	-	1	dB
		G = -20 to -79 dB	-4	-	4	dB
V_{DC}	DC steps	Adjacent attenuation steps	-	0.1	3	mV
		Adjacent gain steps	-	0.5	7	mV
Highpass						
F_{HP}	Highpass corner frequency (2)	f_{C0}	-	50	-	Hz
		f_{C1}	-	60	-	Hz
		f_{C2}	-	80	-	Hz
		f_{C3}	-	100	-	Hz
		f_{C4}	-	120	-	Hz
		f_{C5}	-	150	-	Hz
		f_{C6}	-	180	-	Hz
		f_{C7}	-	220	-	Hz
Lowpass						
F_{LP}	Lowpass corner frequency (2)	f_{C0}	-	50	-	Hz
		f_{C1}	-	60	-	Hz
		f_{C2}	-	80	-	Hz
		f_{C3}	-	100	-	Hz
		f_{C4}	-	120	-	Hz
Audio outputs						
V_{CL}	Clipping level	THD = 0.3%; V_{CC} = 8.5 V PA OUTPUT	-	2	-	V_{RMS}
		THD = 0.3%; V_{CC} = 8.5 V LD OUTPUT; Low gain	-	2.5	-	V_{RMS}
		THD = 0.3%; V_{CC} = 11.5 V LD OUTPUT; High gain	-	3.55	-	V_{RMS}

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{OUT}	Output impedance	-	-	30	100	Ω
R_L	Output load resistance	-	2	-	-	kΩ
C_L	Output load capacitor	-			10	nF
V_{DC}	Output DC level	PA OUTPUT	3.8	4.0	4.2	V
		LD OUTPUT; Low gain	3.8	4.0	4.2	V
		LD OUTPUT; High gain	5.5	5.75	5.9	V
G_{OUT}	Output gain	PA OUTPUT	2	3	4	dB
		LD OUTPUT; Low gain	4	5	6	dB
		LD OUTPUT; High gain	7	8	9	dB
V_{TH_Low}	Low threshold for DESEL pin (3)	-	-	-	0.8	V
V_{TH_High}	High threshold for DCSEL pin (3)	-	2.4	-		V
R_{PU}	Internal pull-up resistor for DCSEL pin	-	32	50	68	kΩ
V_{PU}	Internal pull-up voltage for DCSEL Pin	-	3.1	3.3	3.5	V
V_{th}	Speaker limiter threshold	PA OUTPUT	1	1.5	2	Vpp
			2.5	3	3.5	Vpp
			3.5	4	4.5	Vpp
Auto mix detection						
V_{th}	Auto mix detect threshold	V_1	1	5	12	mV
		V_2	5	10	20	mV
		V_3	5	15	30	mV
		V_4	10	20	40	mV
		V_5	15	25	45	mV
		V_6	20	50	80	mV
		V_7	50	75	120	mV
		V_8	80	100	150	mV
T_{attach}	Attach time	T_1	0.4	0.5	0.6	ms
		T_2	0.8	1	1.2	ms
		T_3	1.6	2	2.4	ms
		T_4	3.5	4	4.5	ms
		T_5	7	8	9	ms
		T_6	14	16	18	ms

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
$T_{release}$	Release time	T_1		100	125	150	ms
		T_2		200	250	300	ms
		T_3		400	500	600	ms
		T_4		800	1000	1200	ms
		T_5		1500	2000	2500	ms
		T_6		3000	4000	5000	ms
A_{MAX}	Attenuation	Auto mix programmable attenuation		17	20	23	dB
A_{STEP}	Step resolution	-		0.5	1	1.5	dB
G_{mix}	Mix gain	-		5	6	7	dB
DC offset detection							
V_{th}	Zero comp. window size	V_1		±5	±30	±60	mV
		V_2		±30	±60	±90	mV
		V_3		±60	±90	±120	mV
		V_4		±90	±120	±150	mV
T_{sp}	Max rejected spike length	-		4	11	25	µs
		-		8	22	38	µs
		-		10	33	55	µs
$I_{CHDCErr}$	DCErr charge current	-		3	5	6	µA
$I_{DISDCErr}$	DCErr discharge current	-		3.5	5	7.5	mA
V_{OutH}	DCErr high voltage	-		3.1	3.3	3.6	V
V_{OutH}	DCErr low voltage	-		-	100	500	mV
V_{TH_Low}	Low threshold for WinIn pin (3)	-		-	-	0.7	V
V_{TH_High}	High threshold for WinIn pin (3)	-		2.8	-	-	V
R_{PU}	Internal pull-up resistor for WinIn pin	-		32	50	68	kΩ
V_{PU}	Internal pull-up voltage for WinIn pin	-		3.1	3.3	3.5	V
Spectrum analyzer							
V_{SAout}	Output voltage range (4)	V_i = SE, In-gain = 0 dB, R_{LOAD} = 1 MΩ	V_i = 1 Vrms	-	1.6	-	V
			V_i = AC-short	-	50	200	mV
			V_i = V_i (max)	3.1	3.3	3.5	V
V_{thL}	Low threshold voltage	for SACLK pin for SARST pin		- -	- -	1.4 1.4	V
V_{thH}	High threshold voltage	for SACLK pin for SARST pin		1.6 1.6	- -	- -	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{i_max}	Maximum input voltage	for SACLK and SARST pins		-	5.5	-	V
C_{RANGE}	In-gain control range	-		5.5	6	6.5	dB
A_{STEP}	In-gain step resolution	-		1.5	2	2.5	dB
f_{C1}	Center frequency, band 1 (2)	-		-	62.5	-	Hz
f_{C2}	Center frequency, band 2 (2)	-		-	125	-	Hz
f_{C3}	Center frequency, band 3 (2)	-		-	250	-	Hz
f_{C4}	Center frequency, band 4 (2)	-		-	500	-	Hz
f_{C5}	Center frequency, band 5 (2)	-		-	1	-	kHz
f_{C6}	Center frequency, band 6 (2)	-		-	2	-	kHz
f_{C7}	Center frequency, band 7 (2)	-		-	4	-	kHz
f_{C8}	Center frequency, band 8 (2)	-		-	8	-	kHz
f_{C9}	Center frequency, band 9 (2)	-		-	16	-	kHz
Q_f	Filter quality factor (1)	Q_1		-	1.75	-	-
		Q_2		-	3.5	-	-
T_{SAclk}	Read-out clock frequency (4)	-		1		100	kHz
T_{SAdel}	Analog output delay time (4)	CLoad at SAout-pin = 100 pF		-	1	2	µs
T_{repeat}	Read-out cycle repeat time (4)	Recommended refresh rate		50	-	-	ms
T_{intres}	Internal reset time (4)	Auto-reset mode enabled		4	5	6	ms
T_{SAres}	Reset pulse time (4)	Auto-reset mode disabled		500	-	-	ns
T_{settle}	Band pass filter settling time (4)	-		30	-	-	ms
General							
e_{NO}	Output noise	BW = 20 Hz to 20 kHz;	PA OUTPUT	-	14	20	µV
		A-Weighted; all gain = 0dB	LD OUTPUT; Low gain	-	15	20	µV
			LD OUTPUT; High gain	-	21	30	µV
		BW = 20 Hz to 20 kHz; A-Weighted, Output muted	PA OUTPUT	-	12	20	µV
			LD OUTPUT; Low gain	-	12	20	µV
			LD OUTPUT; High gain	-	16	30	µV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
S/N	Signal to noise ratio	A-weighted; all gain = 0dB	PA OUTPUT; Vo = 2 V_{RMS}	100	104	-	dB
			LD OUTPUT; Low gain; Vo = 2.5V_{RMS}	100	104	-	dB
			LD OUTPUT; Vo =3.55V_{RMS}	100	104	-	dB
D	Distortion	VIN=1$V_{RMS;}$ all gain = 0dB	PA OUTPUT	-	0.01	0.1	%
			LD OUTPUT; Low gain	-	0.01	0.1	%
			LD OUTPUT; High gain	-	0.01	0.1	%
S_C	Channel Separation left/right	-		75	90	-	dB

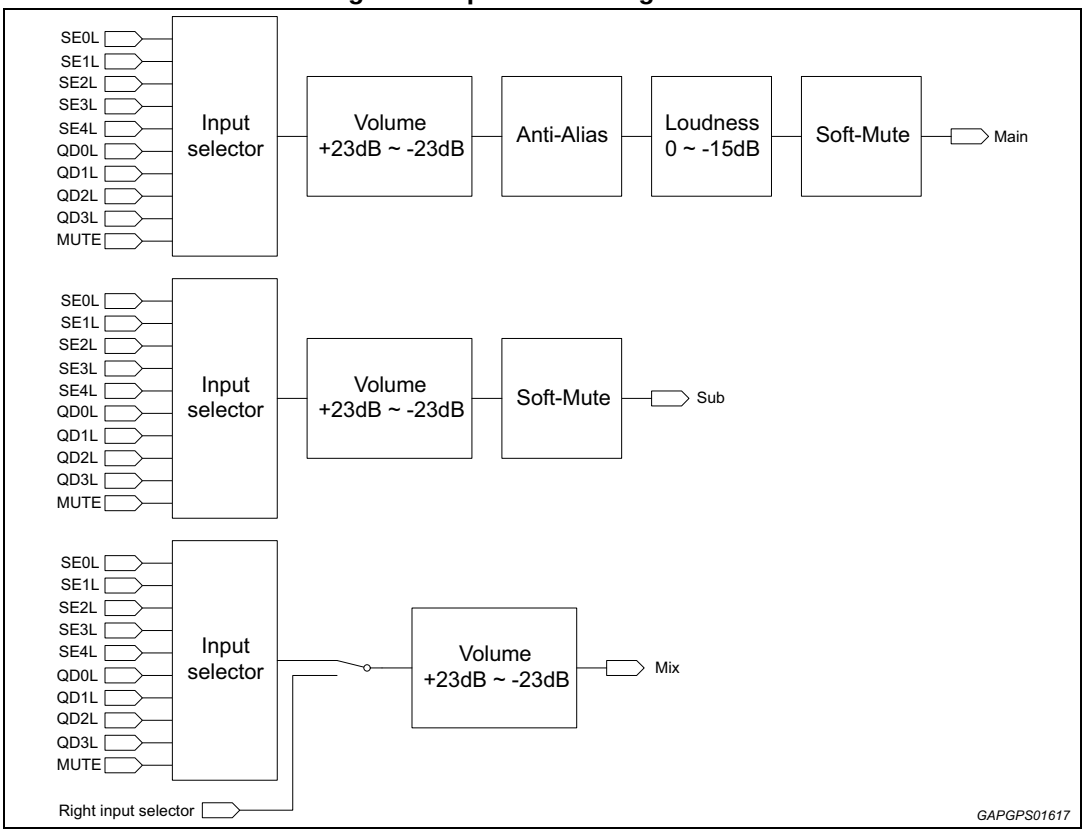
1. Measure performed in DC.
2. Value guaranteed by measuring correlated parameter.
3. Verified only in characterization.
4. Guaranteed by design.

4 Description of audio processor

4.1 Input stage

Four quasi-differential stereo input and five single-ended inputs are available. The input-section of the TDA7715 incorporates three independent stereo signal paths, where each of them can be connected to a variety of inputs. For simplicity only the left inputs are shown.

Figure 3. Input section signal flow



4.1.1 Single-ended stereo input (SE0, SE1, SE2, SE3, SE4)

The input-impedance at each input is 100 kΩ and the attenuation is fixed to -3 dB for incoming signals.

4.1.2 Quasi-differential stereo Input (QD0, QD1, QD2, QD3)

The QD input is implemented as a buffered quasi-differential stereo stage with 100 kΩ input-impedance at each input. There is -3 dB attenuation at QD input stage.

4.1.3 Fast charge

Each differential input pin features a "fast-charge" switch allowing to quickly charge any external large coupling capacitors upon power-on of the device. When the device is powered-on, the “fast-charge” switches are automatically turned on, for normal operation these switches need to be released by any programming of byte_0.

4.2 Volume

A ±3 dB input gain is selectable in volume stage. When the volume-level is changed audible clicks could appear at the output. The root cause of those clicks could either be a DC-Offset before the volume-stage or a sudden change in the envelope of the audio signal. With the soft-step feature both kind of clicks could be reduced to a minimum and are no longer audible. The blend-time from one step to the next is programmable and can be set 7.5 ms or 15 ms. The soft-step control is described in detail in *Section 4.10*.

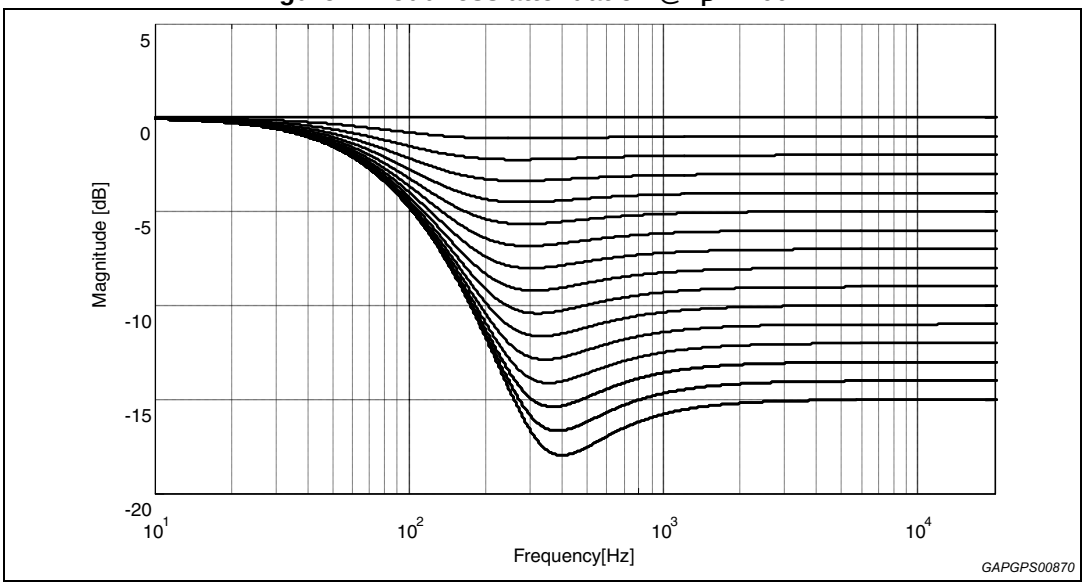
4.3 Loudness

There are four parameters programmable in the loudness stage.

4.3.1 Loudness attenuation

Figure 4 shows the attenuation as a function of frequency at f_P = 400 Hz

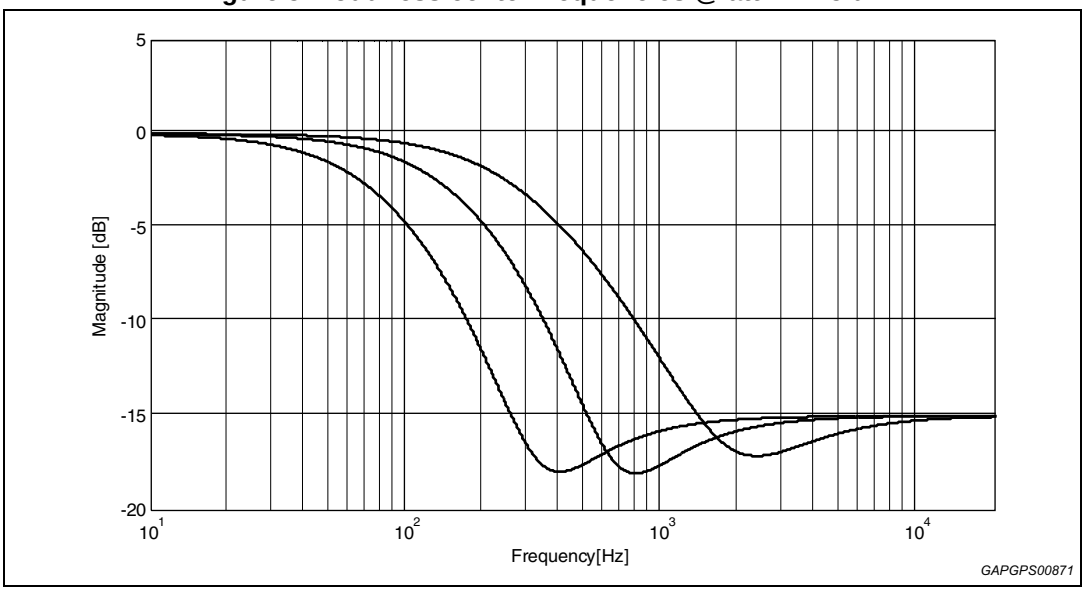
Figure 4. Loudness attenuation @ f_P = 400 Hz



4.3.2 Peak frequency

Figure 5 shows the four possible peak-frequencies at 400, 800 and 2400 Hz

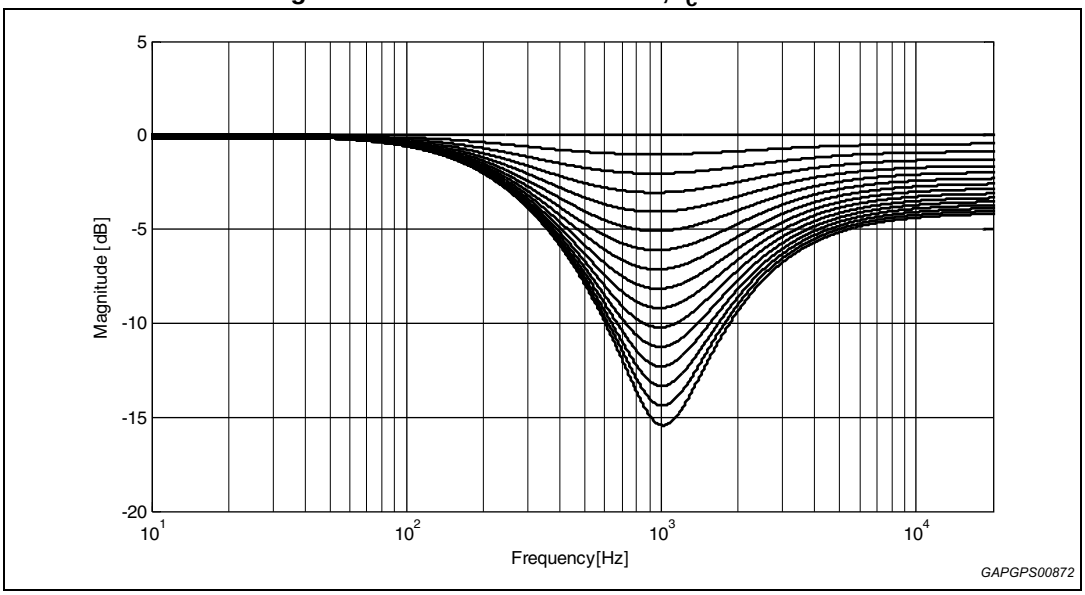
Figure 5. Loudness center frequencies @ attn. = 15 dB



4.3.3 High frequency boost

Figure 6 shows the different loudness shapes in low & high frequency boost.

Figure 6. Loudness attenuation, f_c = 2.4 kHz



4.3.4 Flat mode

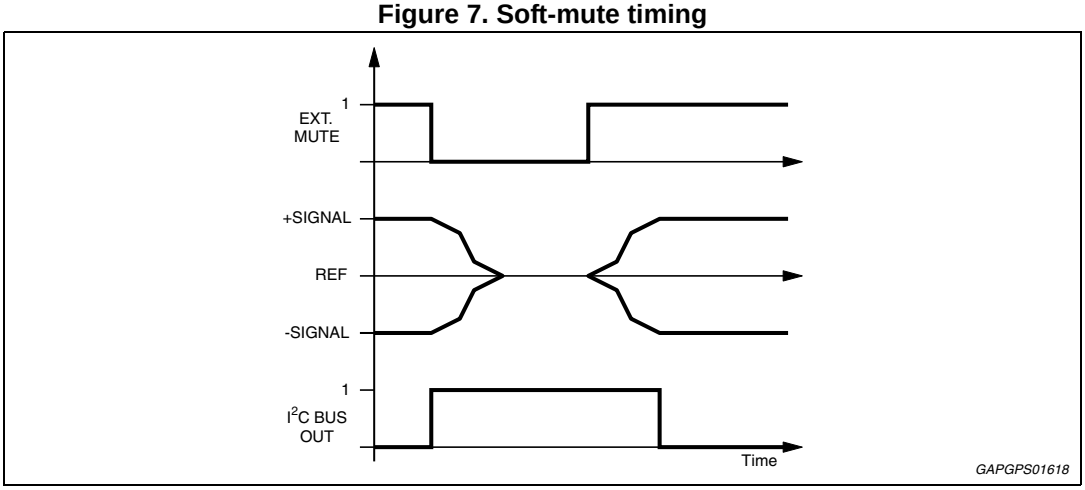
In flat mode the loudness stage works as a 0 dB to -15 dB attenuator.

4.4 Soft-mute

The digitally controlled soft-mute stage allows muting/de-muting the signal with an I^2C bus programmable slope. The mute process can be activated either by the soft-mute pin or by the I^2C-bus. This slope is realized in a special S-shaped curve to mute slowly in the critical regions (see *Figure 7*).

For timing purposes the soft-mute bit of the I^2C bus output register is set to 1 from the start of muting until the end of de-muting.

Figure 7. Soft-mute timing



Note: Please note that a started Mute-action is always terminated and could not be interrupted by a change of the mute –signal.

In this device an auto-mute function is available to reduce the complexity of programming. When auto-mute is on, all setting related to filter will trigger an auto-mute for Smute0, Smute1 and Smute2. The auto-mute procedure is as follows:

a) Filter setting is changed by I^2C, but the changed setting is blocked by auto-mute
b) Smute0/1/2 soft-mute is triggered
c) Filter setting is changed after soft-mute is finished
d) Smute0/1/2 is de-muted

The filter setting which will activate auto-mute is as follows:

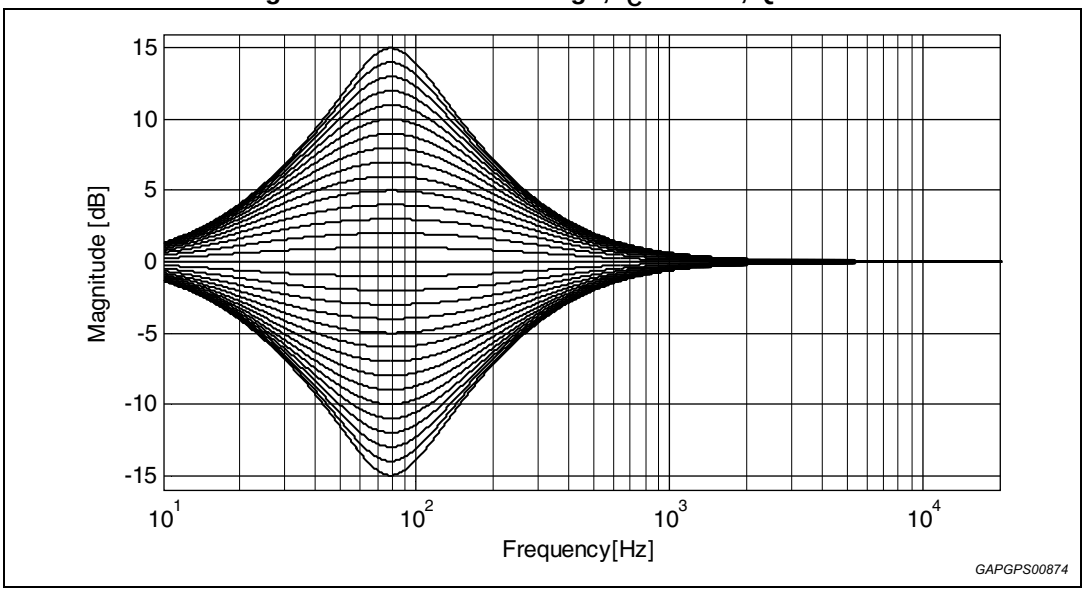
a) Loudness: center frequency, high boost
b) Treble: center frequency
c) Middle: center frequency, quality factor
d) Bass: center frequency, quality factor, DC mode
e) LPF: corner frequency, phase inversion
f) HPF: corner frequency, phase inversion

4.5 Bass

4.5.1 Bass attenuation

Figure 8 shows the control range in the frequency domain at 80 Hz center frequency.

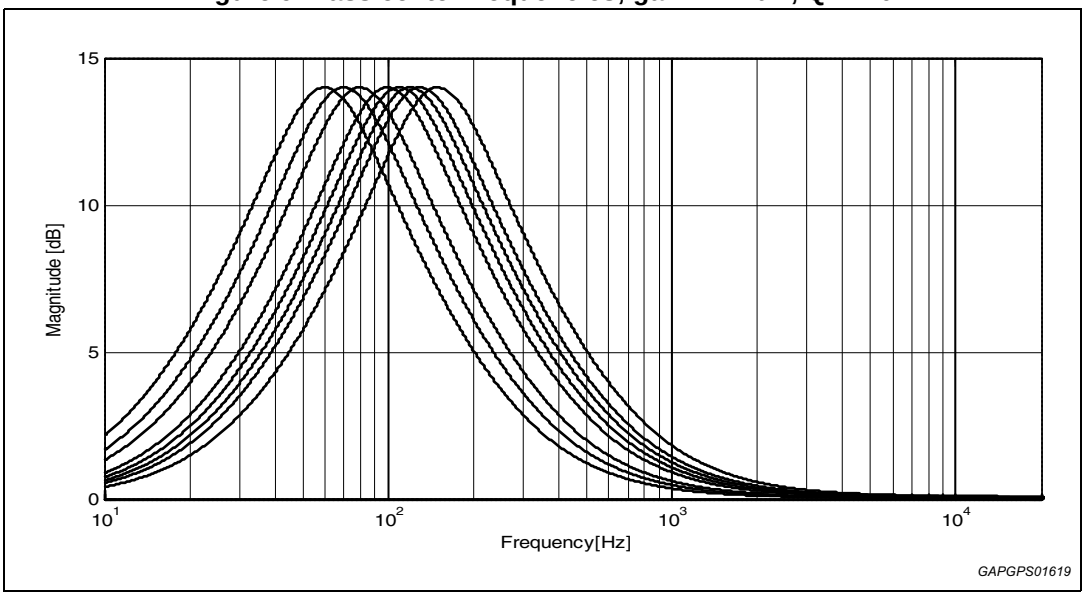
Figure 8. Bass control range; f_C = 80 Hz, Q = 1.0



4.5.2 Center frequency

Figure 9 shows all the selectable center frequencies at a gain of 14 dB.

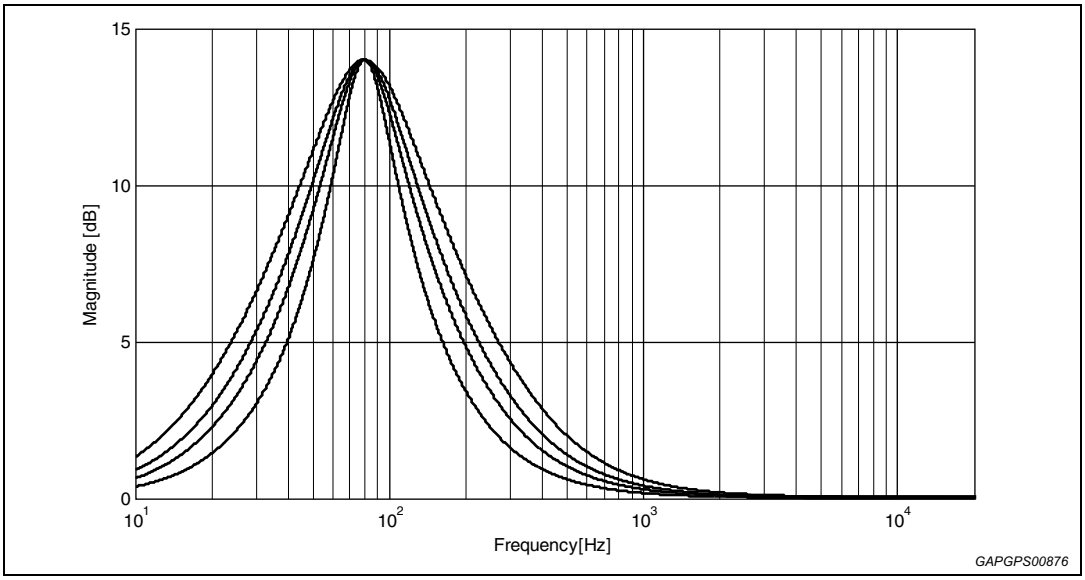
Figure 9. Bass center frequencies; gain = 14 dB, Q = 1.0



4.5.3 Quality factors

Figure 10 shows the four selectable filter quality factors at a gain of 14 dB.

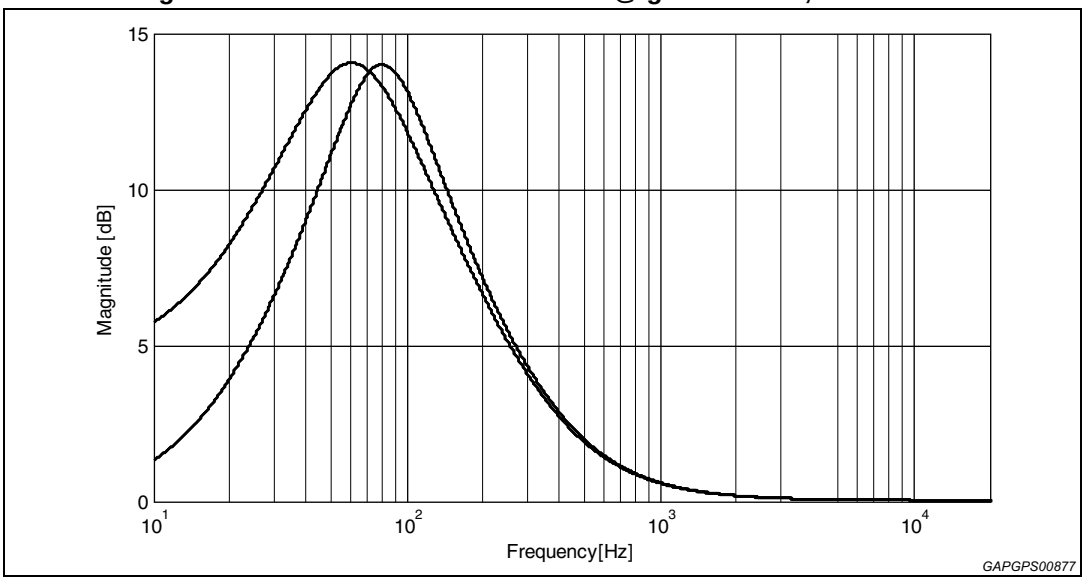
Figure 10. Bass filter quality factors; f_C = 80 Hz, gain = 14 dB.



4.5.4 DC Mode

Figure 11 shows the effect of the DC-mode at a filter gain of 15 dB. In this mode the DC-gain is increased by 4.4 dB. In addition the programmed center frequencies and quality factors are decreased by 25%, which realizes alternative frequency responses.

Figure 11. Bass normal and DC mode @ gain = 14 dB, fc = 80 Hz



Note: The center frequency, Q and DC-mode can be independently set.

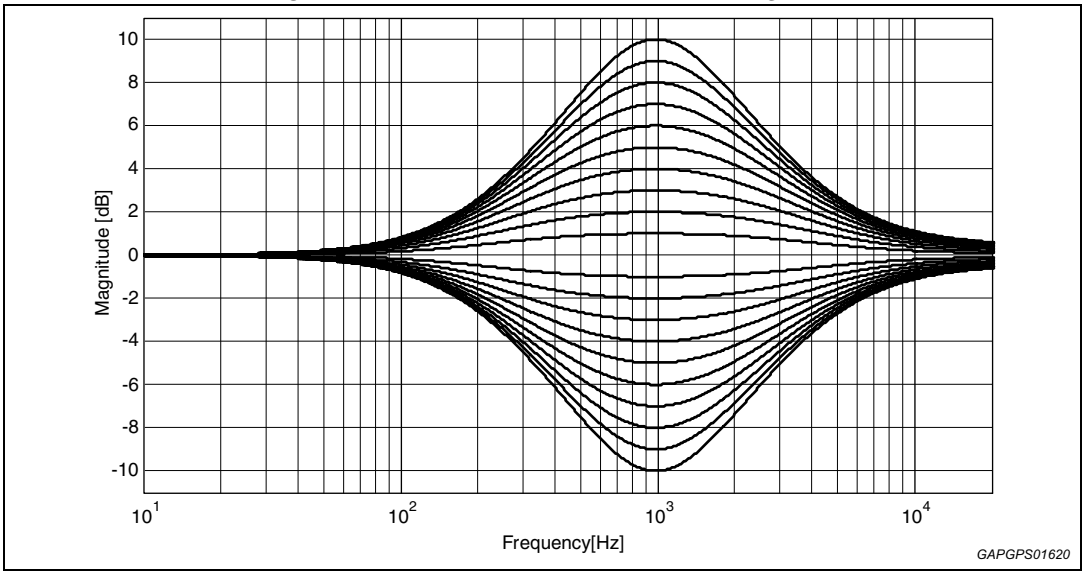
4.6 Middle

There are three parameters programmable in the mid-filter stage.

4.6.1 Middle attenuation

Figure 12 shows the attenuation as a function of frequency at a center frequency of 1 kHz.

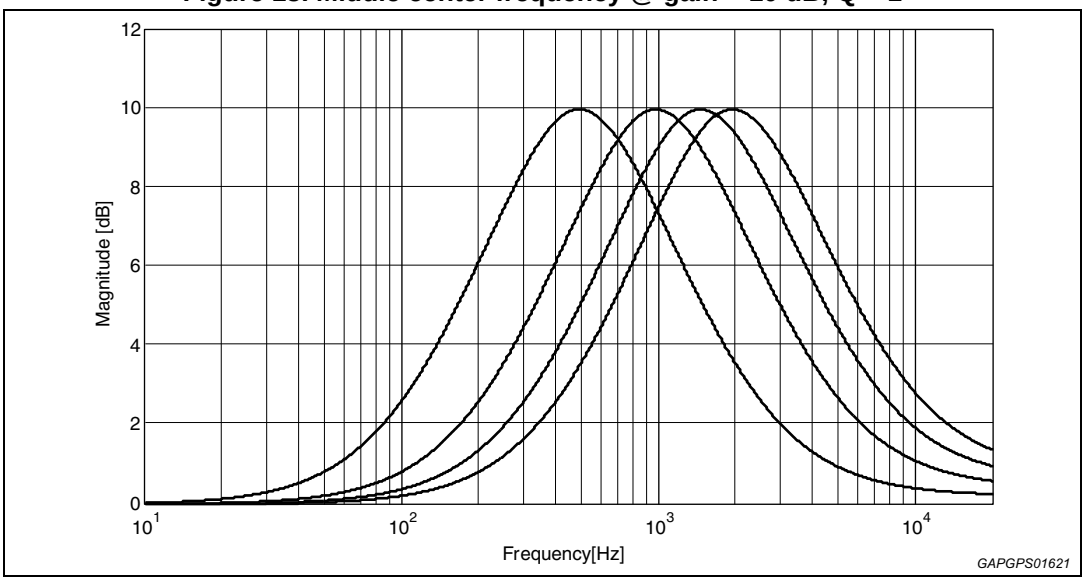
Figure 12. Middle control @ fc = 1 kHz, Q = 1



4.6.2 Middle center frequency

Figure 13 shows the four possible center frequencies 500 Hz, 1 kHz, 1.5 kHz and 2.5 kHz.

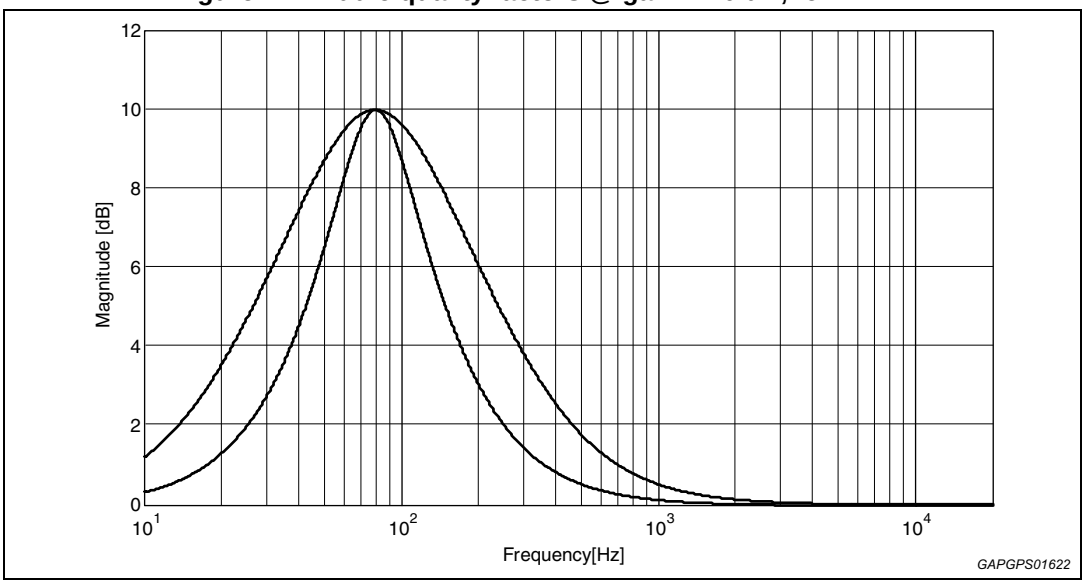
Figure 13. Middle center frequency @ gain = 10 dB, Q = 1



4.6.3 Quality factors

Figure 14 shows the two possible quality factors 1 and 2

Figure 14. Middle quality factors @ gain = 10 dB, fc =1 kHz



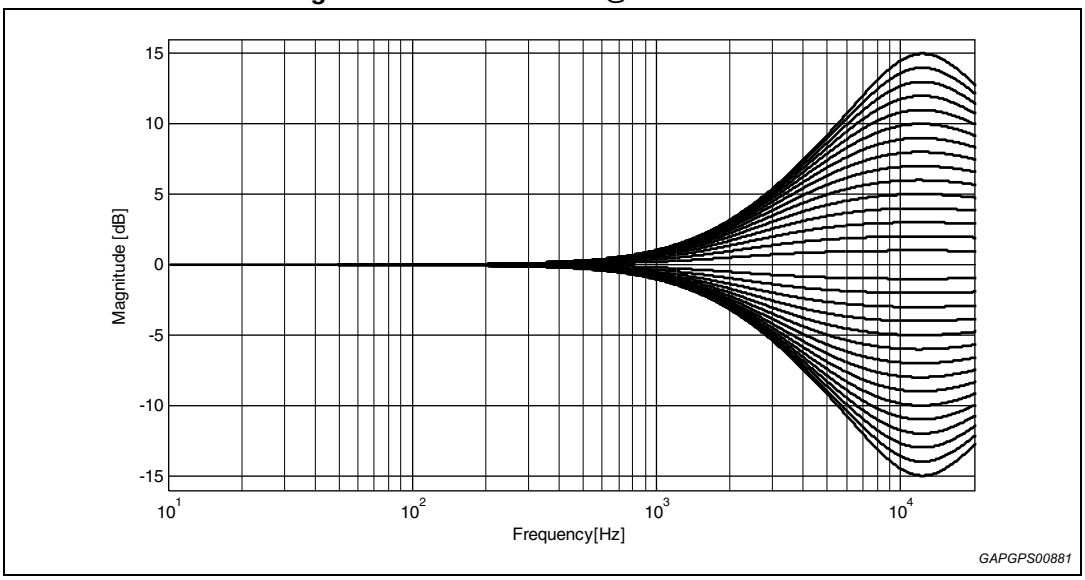
4.7 Treble

There are two parameters programmable in the treble stage.

4.7.1 Treble attenuation

Figure 15 shows the attenuation as a function of frequency at a center frequency of 17.5 kHz.

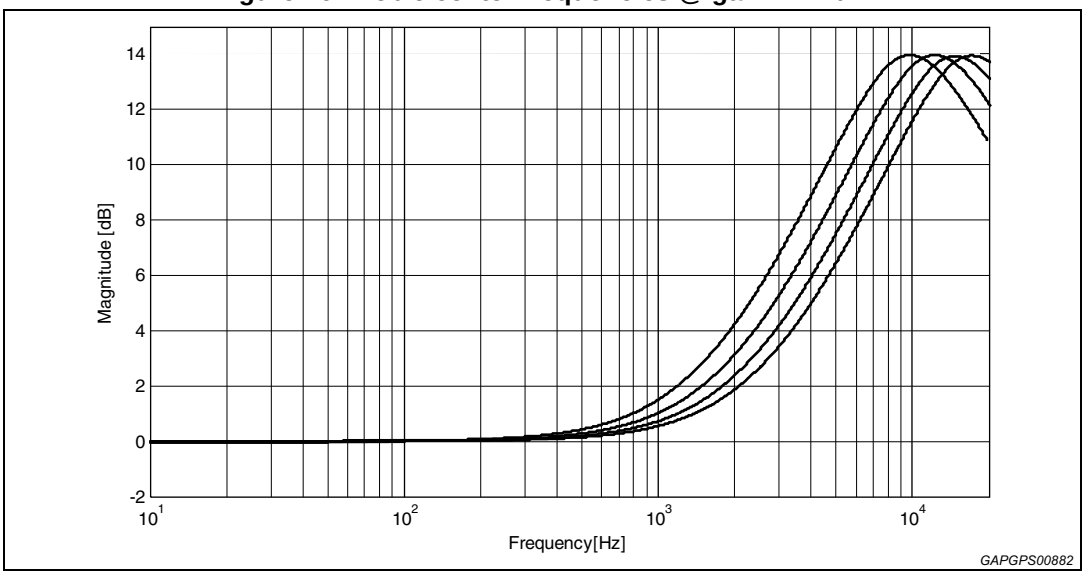
Figure 15. Treble control @ fc = 17.5 kHz



4.7.2 Center frequency

Figure 16 shows the four possible center frequencies 10k, 12.5k, 15k and 17.5 kHz.

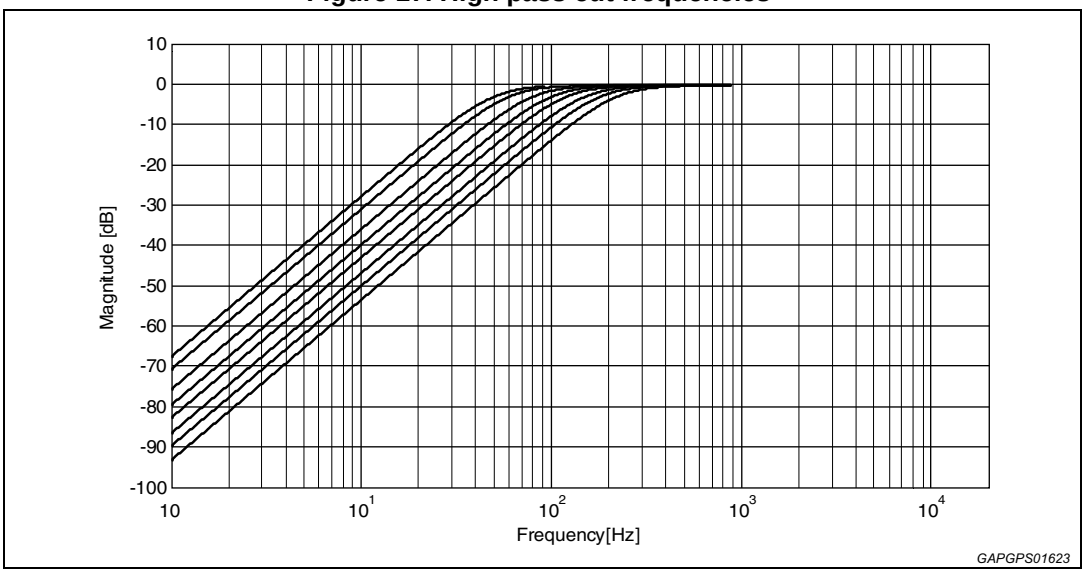
Figure 16. Treble center frequencies @ gain = 14 dB



4.8 High pass filter

The high pass filter has 2 order filter characteristics with programmable cut-off frequency (50/60/80/100/120/150/180/220 Hz)

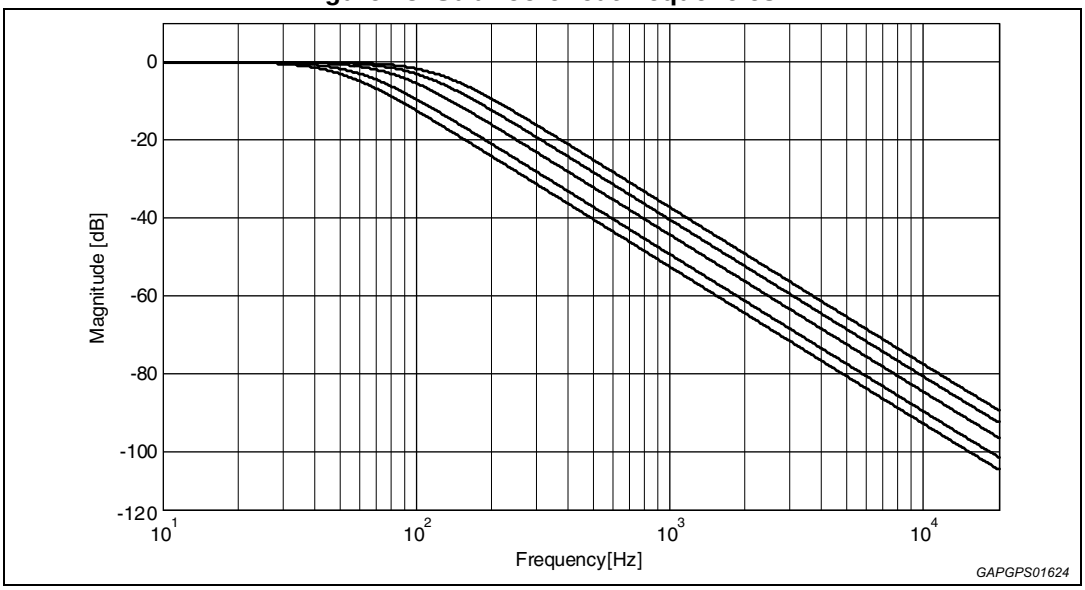
Figure 17. High pass cut frequencies



4.9 Low pass filter

The subwoofer lowpass filter has Butterworth characteristics with programmable cut-off frequency (50/60/80/100/120 Hz). The output phase can be selected between 0 deg and 180 deg. The input of subwoofer takes signal from bass filter output or output of input mux.

Figure 18. Subwoofer cut frequencies



4.10 Soft-step

In this device, the soft-step function is available for volume, speaker, loudness, treble, middle and bass block. With the soft-step function, the audible noise of DC offset or the sudden change of signal can be avoided when adjusting the gain setting of the block.

For each block, the soft-step function is controlled by soft-step on/off control bit in the control table. The soft-step transient time selection (7.5 ms or 15 ms) is common for all blocks and it is controlled by soft-step time control bit. The soft-step operation of all blocks has a common centralized control. In this case, a new soft-step operation will not be started before the completion of previous soft-step.

There are two different modes to activate the soft-step operation. The soft-step operation can be started right after I^2C data sending, or the soft-step can be activated in parallel after data sending of several different blocks. The two modes are controlled by the ‘act bit’ (it is normally bit7 of the byte.) of each byte. When act bit is ‘0’, which means action, the soft-step is activated right after the date byte is sent. When the act bit is ‘1’, which means wait, the block goes to wait for soft-step status. In this case, the block will wait for some other block to activate the operation. The soft-step operation of all blocks in wait status will be done together with the block which activates the soft-step. With this mode, all specific blocks can do the soft-step in parallel. This avoids waiting when the soft-step is operated one by one. Please note that if a block is set to ‘gain1’ with act bit = 1, later this block is set to ‘gain2’ with act bit = 0, in this case the block will do a soft-step from the currently set gain to ‘gain2’ but not from the currently set gain to ‘gain1’ then to ‘gain2’.

Chip Addr	Sub Addr	0xxxxxxx

|← Soft-step start here

Chip Addr	Sub Addr	1xxxxxxx	1xxxxxxx	.....	0xxxxxxx

|← Soft-step start here for all

4.11 DC Offset Detector

Using the DC offset detection circuit (*Figure 19*) an offset voltage difference between the audio power amplifier and the TDA7715's Front and Rear outputs can be detected, preventing serious damage to the loudspeakers. The circuit compares whether the signal crosses the zero level at the loudspeaker output of the audio power amplifier at the same time as at the output of the TDA7715. The output of the zero-window-comparator of the power amplifier must be connected with the WinIn-input of the TDA7715. The WinIn-input has an 50 kΩ internal pull-up resistor connected to 3.3 V. It is recommended to drive this pin with open-collector outputs or equivalent.

To compensate for errors at low frequencies the WinTCL/R-pin is implemented, with external capacitors introducing the same delay = 15kΩ*Cext as the one caused by the AC-coupling between the TDA7715 and the input of the power amplifier. For the zero window comparators, the time constant for spike rejection as well as the threshold are programmable.

See *Electrical characteristics on page 10*.

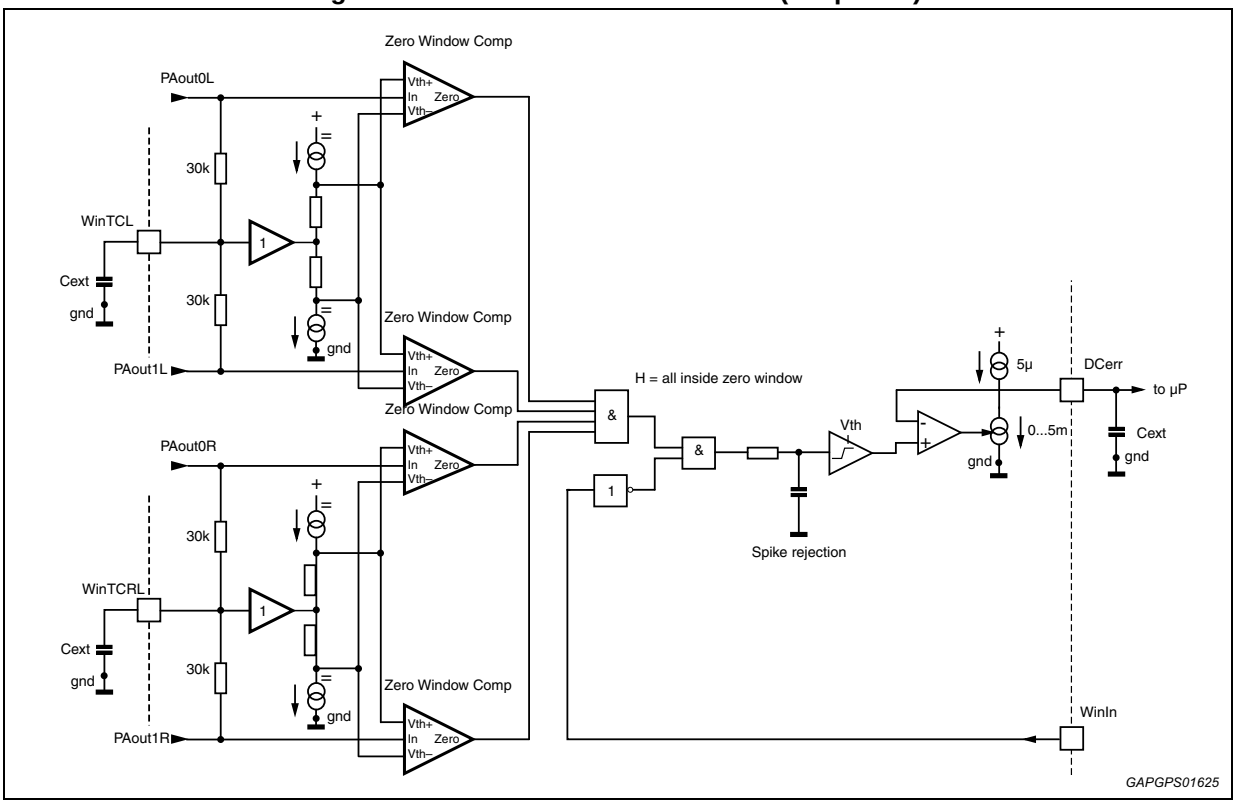
A low-active DC-offset error signal appears at the DCErr output if the next conditions are both true:

a) Front and rear outputs are inside zero crossing windows.

b) The Input voltage Vwinin is logic low whenever at least one output of the power amplifier is outside the zero crossing windows.

After power-on, the external attached capacitor is rapidly charged (fast-charge) to overcome a false indication. For normal operation these switches need to be released by any programming of byte_0. After that, the “fast-charge” switches can be turned on/off by setting “fast charge = on/off”.

Figure 19. DC offset detection circuit (simplified)



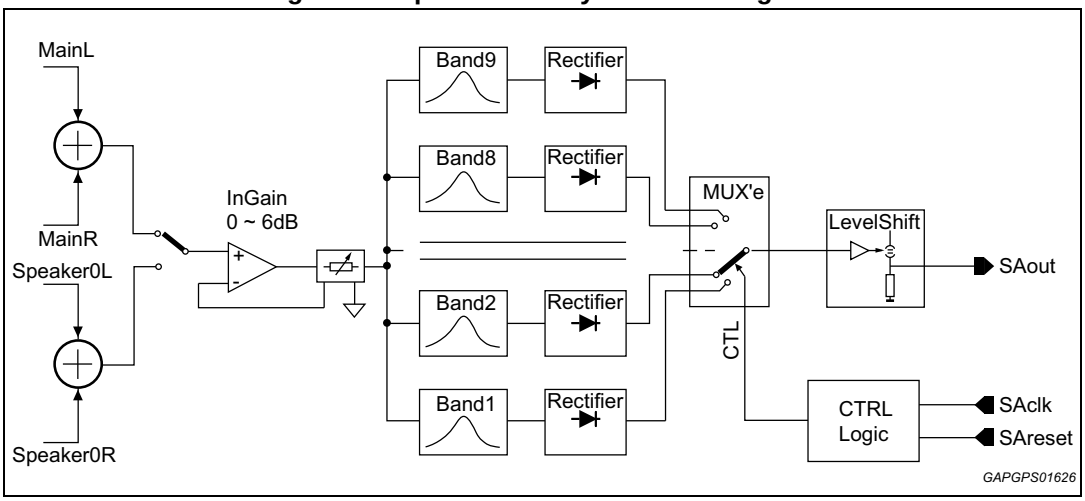
4.12 Spectrum analyzer

A fully integrated nine-band spectrum analyzer is present in the TDA7715 (*Figure 20*). The spectrum analyzer consists of nine band pass filters followed by rectifiers with sample capacitors that store the maximum peak signal level for each band since the last read cycle.

This peak signal level can be read by a microprocessor at the SAout-pin. To allow easy interfacing to an analog input-port of a microprocessor, the output voltage at this pin is referred to device ground. Since the output voltage follows the peak level linearly, the microprocessor should take care of a logarithmic conversion (e.g. logarithmic look-up table).

The spectrum analyzer's input signal is either the mono-sum of main channel output or speaker channel 0. In order to have some influence on the visual behavior in a given application the filter quality for all band-pass filters may be programmed for two different qualities, with the higher filter quality creating a faster, more differentiating optical response. If the spectrum analyzer is disabled, the SAclk-pin and SArst-pin should be tied to ground.

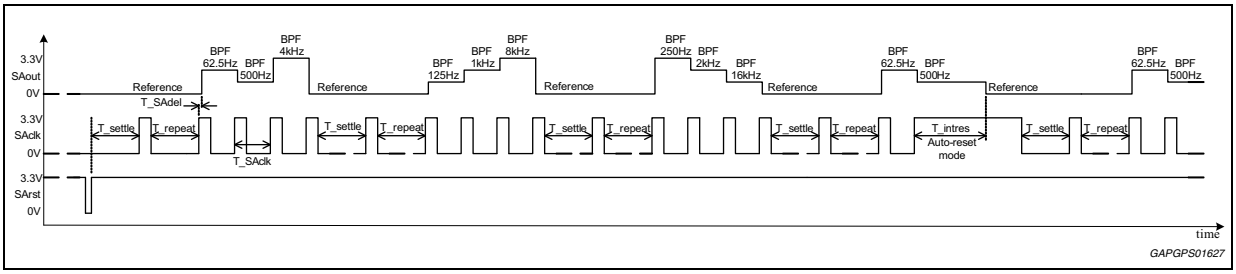
Figure 20. Spectrum analyzer block diagram



The microprocessor starts a read cycle with a negative going clock edge at the SAclk input. On the following positive clock edges, the stored peak signal level of the band pass filters is subsequently switched to SAout. Each analog output value is valid after the time T_{SAdel}.

A reset is generated whenever SAclk remains high for the time T_{intres}. Note that a proper reset requires the clock signal SAclk to be held at high potential and that the reset is not repetitive. Once a reset was triggered, a new read-out cycle should not be initiated before the time T_{repeat} has passed. This allows sufficient settling of the filters. *Figure 21* illustrates the read cycle timing of the spectrum analyzer.

Figure 21. Read cycle timing diagram



4.13 Output stage

The output-section (*Figure 22*) incorporates three independent stereo signal paths, where each one can be connected to three AC-coupled, single-ended inputs and to some dedicated signals originating from the input-section and/or main-signal-path. The input-impedance at each AC-coupled input is 100 kΩ and the attenuation is fixed to -3 dB for incoming signals.

Signal path 0 and 1 (front and rear) may optionally enter high-pass filters whereas signal path 2(other) can be low-pass filtered for subwoofer applications. Anti-radiation filters are integrated for all signal paths. Soft-mute stages and a soft-step volume, that offer fast and click-less muting and/or volume changing follow all three filters.

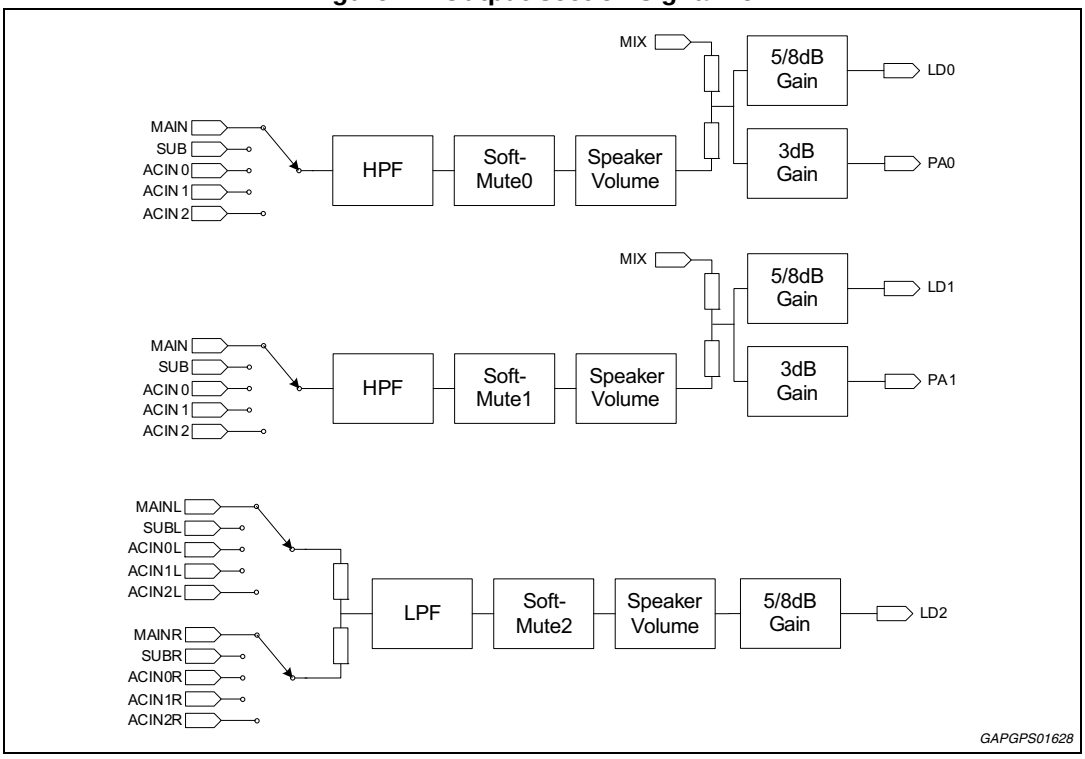
Five stereo pairs of output buffers finally complete the output-section: Signal-path 2 exclusively feeds a line driver output that is capable of 3.55 V_{RMS} output level as required by external (remote) power amplifiers. The signal-paths 0 & 1 feature both, a line driver output

and a dedicated internal (on board) power amplifier output with 3 dB fixed gain. To maximize the line-driver output swing, when the power supply option (V_{CC} = 11.5 V) is not needed or available, the line-driver output stages may be programmed for lower gain, still delivering 2.5 V_{RMS} (V_{CC} = 8.5 V).

The output gain of line-driver is configurable to fit different applications. A dedicated pin (DCSEL) is used to set the desired configuration during power-on of the Device, thus avoiding the DC voltage step of the speaker output which would occur should the configuration be done run-time. The configuration is made by connecting this pin to ground (AC Gain = 5 dB, DC level = 4 V) or leave it open (AC Gain = 8 dB, DC level = 5.75 V). The output gain can anyway be changed after power-on by DCSEL pin (high or low) with 'pin influence for output DC level select = PIN', or by I^2C bus (Output DC level) with 'pin influence for output DC level select = I^2C'.

A speaker-limiter is integrated to limit the signal level of output driver which feeds the power amplifier (PA0L, PA0R, PA1L and PA1R). The speaker-limiter-threshold can be set as 1.5 Vpp, 3 Vpp, 4 Vpp or turned-off.

Figure 22. Output-section signal flow



4.14 Mixing

In this device, a very flexible mixing function (*Figure 23*) is available to meet all kind of applications. The mixing input is selected by a mixing-multiplexer which is described in *Section 4.1*. After mixing multiplexer and mixing volume, the mixing signal is mixed with speaker0 or speaker1 volume output. The following 0/6 dB mixing gain offers 2 kind of mixing option, -6 dB/-6 dB mixing or 0 dB/0 dB mixing.

An auto-mix-detector is available to detect the mixing signal level and do the mixing and un-mixing automatically. The auto-mix procedure is different for speaker0 and speaker1.

The speaker0 auto-mix working procedure is as follows:

a) Auto-mix-detector detects if the mixing signal amplitude is higher than ‘auto-mix-detect-threshold’ for ‘auto-mix-attach-time’

b) If a) is positive, speaker0 volume will be attenuated ‘auto-mix-programmable-attenuation’

c) Mixing is activated

d) Auto-mix-detector detects if the mixing signal amplitude is lower than ‘auto-mix-detect-threshold’ for ‘auto-mix-release-time’

e) If d) is positive, speaker0 volume will return to the old setting

f) Un-mixing is activated

The speaker1 auto-mix working procedure is as follows:

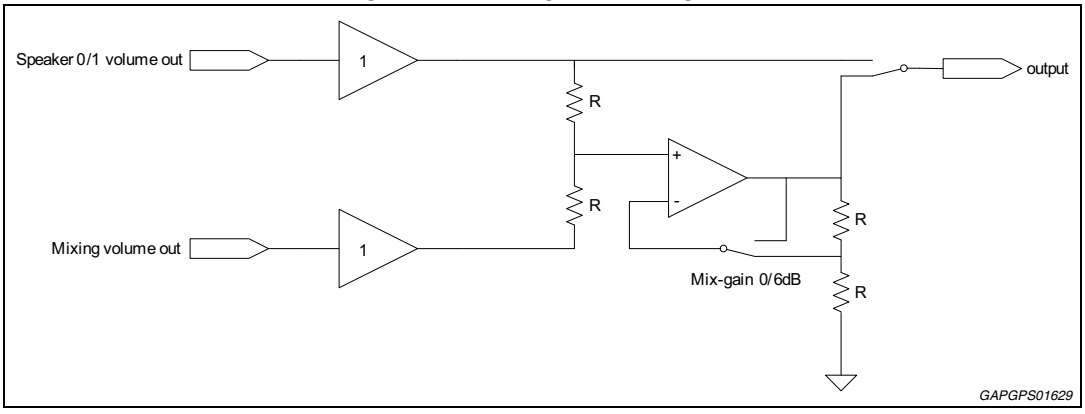
a) Auto-mix-detector detects if the mixing signal amplitude is higher than ‘auto-mix-detect-threshold’ for ‘auto-mix-attach-time’

b) If a) is positive, Mixing is activated

c) Auto-mix-detector detects if the mixing signal amplitude is lower than ‘auto-mix-detect-threshold’ for ‘auto-mix-release-time’

d) If c) is positive, Un-mixing is activated

Figure 23. Mixing block diagram



4.15 Audio processor testing

In the test mode, which can be activated by setting bit D7 of the I^2C subaddress byte and bit D0 of the TEST I byte, several internal signals are available at SARST pin.

External clock can be applied to SMUTEMAIN pin by setting bit D2 of the TEST II byte.

4.16 Application note

Figure 24. Application schematic

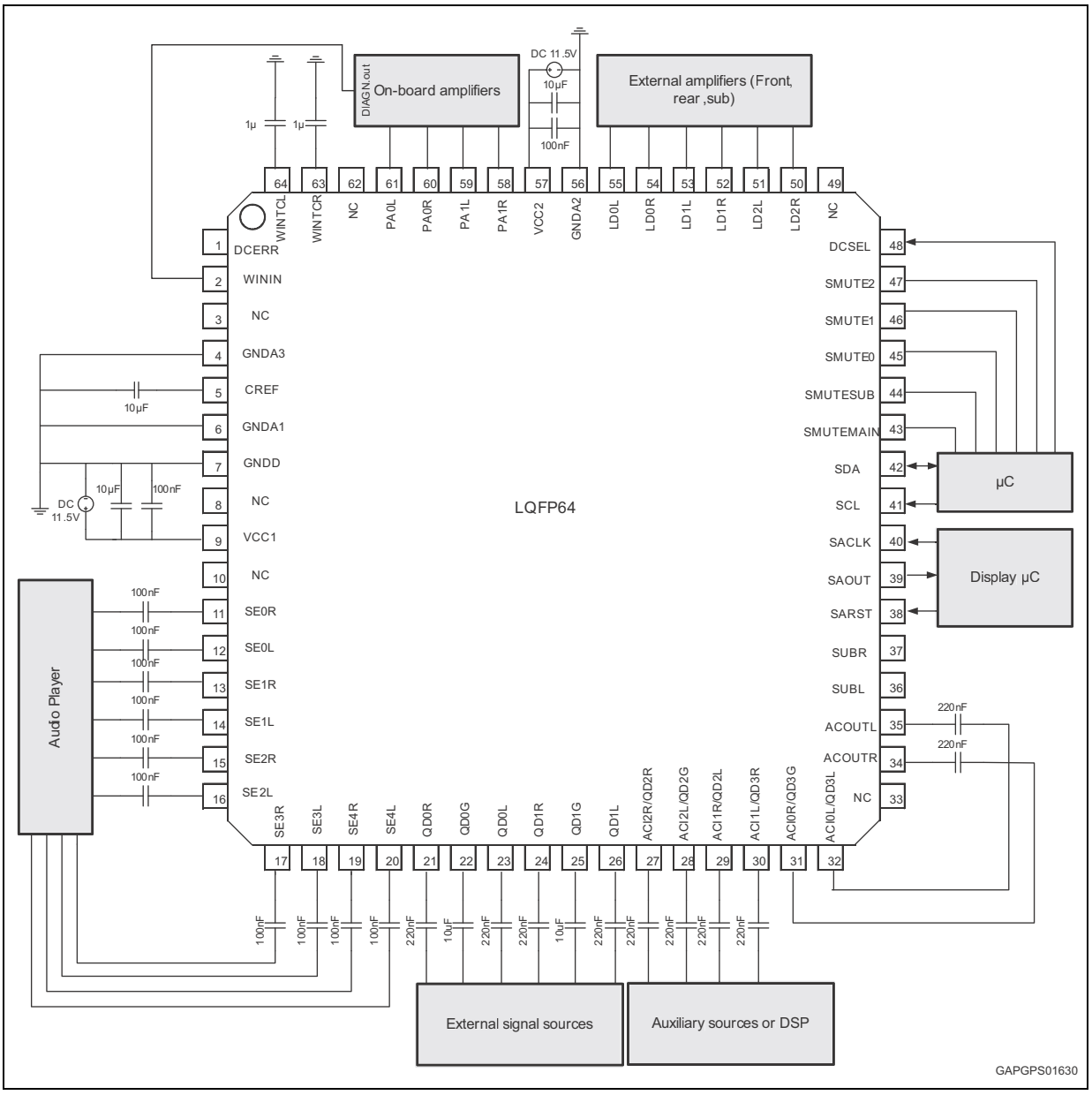


Figure 24 shows a proposal for a typical application. However, the figure only represents one possible interconnection scheme with other devices (The shaded blocks could represent a complex digital sound reproducing/processing system). All reported capacitor values are indicative, their actual value depending on girdling impedances of the real application. This is especially true for the capacitors located at the WinTC-pins as can be read in *Section 4.11*.

Note: In case the DC-detector function is not assessed in the application it is recommended to short both the WinTC-pins 63 and 64 to device-ground.

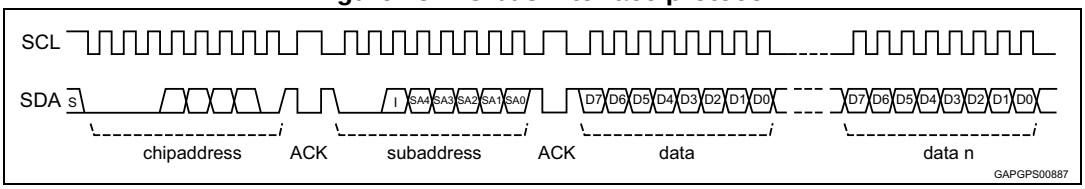
5 I²C bus specification

5.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- the max. clock speed is 400kbits/s
- 3.3 V logic compatible

Figure 25. I²C bus interface protocol



S = Start

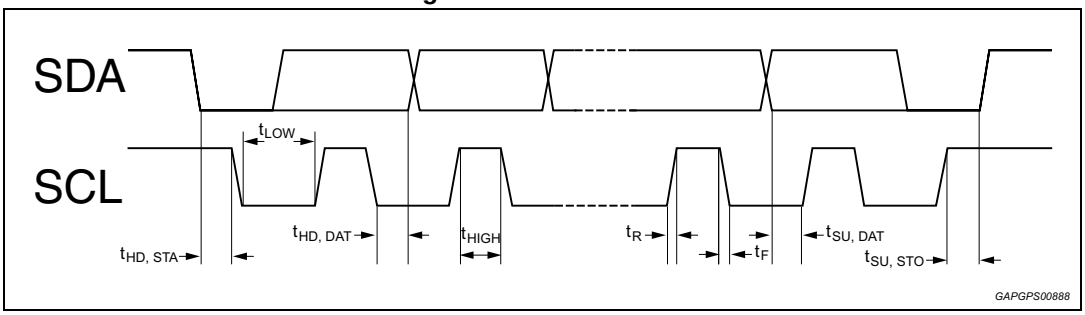
ACK = Acknowledge

5.2 I²C bus electrical characteristics

Table 6. I²C bus electrical characteristics

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL clock frequency	-	400	kHz
V_{IH}	High level input voltage	2.4	-	V
V_{IL}	Low level input voltage	-	0.8	V
$t_{HD,STA}$	Hold time for START	0.6	-	µs
$t_{SU,STO}$	Setup time for STOP	0.6	-	µs
t_{LOW}	Low period for SCL clock	1.3	-	µs
t_{HIGH}	High period for SCL clock	0.6	-	µs
t_F	Fall time for SCL/SDA	-	300	ns
t_R	Rise time for SCL/SDA	-	300	ns
$t_{HD,DAT}$	Data hold time	0	-	ns
$t_{SU,DAT}$	Data setup time	100	-	ns

Figure 26. I²C bus data



5.2.1 Receive mode

S	1	0	0	0	1	0	0	R/W	ACK	TS	X	AI	A4	A3	A2	A1	A0	ACK	DATA	ACK	P

S = Start

R/W = "0" -> Receive mode (Chip can be programmed by µP)

"1" -> Transmission mode (Data could be received by µP)

ACK = Acknowledge

P = Stop

TS = Testing mode

AI = Auto increment

5.2.2 Transmission mode

S	1	0	0	0	1	0	0	R/W	ACK	X	BZ	MT	SMM	SMS	SM2	SM1	SM0	ACK	P

BZ = Soft-step busy (‘0’ = Busy)

AMT = Auto Mix Detection (‘1’ = Auto-Mix Detected)

SMM = Soft-mute activated for main channel (‘1’ = Soft-muted)

SMS = Soft-mute activated for sub channel (‘1’ = Soft-muted)

SM2 = Soft-mute activated for speaker2 (‘1’ = Soft-muted)

SM1 = Soft-mute activated for speaker1 (‘1’ = Soft-muted)

SM0 = Soft-mute activated for speaker0 (‘1’ = Soft-muted)

X = Not used

The transmitted data is automatically updated after each ACK. Transmission can be repeated without new chip address.

5.2.3 Reset condition

A power-on-reset is invoked if the supply voltage is below than 3.5 V. After that the registers are initialized to the default data written in following tables.

Table 7. Subaddress (receive mode)

MSB							LSB	Function
I2	I1	I0	A4	A3	A2	A1	A0	
0 1	-	-	-	-	-	-	-	**Testing mode** Off On
-	x	-	-	-	-	-	-	**Not used**
-	-	0 1	-	-	-	-	-	**Auto increment mode** Off On
-	-	-	0	0	0	0	0	Main / Sub selector
-	-	-	0	0	0	0	1	Mix selector / Anti-alias
-	-	-	0	0	0	1	0	Volume main
-	-	-	0	0	0	1	1	Volume sub
-	-	-	0	0	1	0	0	Volume Mix
-	-	-	0	0	1	0	1	Soft-step
-	-	-	0	0	1	1	0	Soft-mute I
-	-	-	0	0	1	1	1	Soft-mute II / Middle
-	-	-	0	1	0	0	0	Loudness
-	-	-	0	1	0	0	1	Treble filter
-	-	-	0	1	0	1	0	Middle filter
-	-	-	0	1	0	1	1	Bass filter
-	-	-	0	1	1	0	0	Bass / Low pass filter
-	-	-	0	1	1	0	1	High pass filter
-	-	-	0	1	1	1	0	Speaker0/1 source selector
-	-	-	0	1	1	1	1	Output gain / Speaker2 source selector / Middle
-	-	-	1	0	0	0	0	Speaker0L attenuation
-	-	-	1	0	0	0	1	Speaker0R attenuation
-	-	-	1	0	0	1	0	Speaker1L attenuation
-	-	-	1	0	0	1	1	Speaker1R attenuation
-	-	-	1	0	1	0	0	Speaker2L attenuation
-	-	-	1	0	1	0	1	Speaker2R attenuation
-	-	-	1	0	1	1	0	Auto-mix I
-	-	-	1	0	1	1	1	Auto-mix II
-	-	-	1	1	0	0	0	Auto-mix III
-	-	-	1	1	0	0	1	DC-detector / Speaker-limiter
-	-	-	1	1	0	1	0	Spectrum analyzer
-	-	-	1	1	0	1	1	Test I
-	-	-	1	1	1	0	0	Test II
-	-	-	1	1	1	0	1	Test III

5.3 Data byte specification

Table 8. Main / sub selector (0)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Main Source Selector
				0	0	0	0	SE0
				0	0	0	1	SE1
				0	0	1	0	SE2
				0	0	1	1	SE3
				0	1	0	0	SE4
				0	1	0	1	QD0
-	-	-	-	0	1	1	0	QD1
				0	1	1	1	QD2
				1	0	0	0	QD3
				1	0	0	1	MUTE
				1	0	1	0	MUTE
				1	0	1	1	MUTE
				1	1	x	x	MUTE
								Sub Source Selector
0	0	0	0					SE0
0	0	0	1					SE1
0	0	1	0					SE2
0	0	1	1					SE3
0	1	0	0					SE4
0	1	0	1					QD0
0	1	1	0	-	-	-	-	QD1
0	1	1	1					QD2
1	0	0	0					QD3
1	0	0	1					MUTE
1	0	1	0					MUTE
1	0	1	1					MUTE
1	1	x	x					MUTE

Table 9. Mix selector / anti-alias / fast charge (1)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Mix Source Selector
				0	0	0	0	SE0
				0	0	0	1	SE1
				0	0	1	0	SE2
				0	0	1	1	SE3
				0	1	0	0	SE4
-	-	-	-	0	1	0	1	QD0
				0	1	1	0	QD1
				0	1	1	1	QD2
				1	0	0	0	QD3
				1	0	0	1	MUTE
				1	0	1	0	MUTE
				1	0	1	1	MUTE
				1	1	x	x	<u>MUTE</u>
								Mix Left channel
-	-	-	0	-	-	-	-	<u>Left</u>
			1					Right
								Mix Right channel
-	-	0		-	-	-	-	Left
		1						<u>Right</u>
								Anti-alias filter
-	0	-	-	-	-	-	-	<u>On</u>
	1							Off
								AC-Coupling / QD selection
0	-	-	-	-	-	-	-	AC
1								<u>QD</u>

Table 10. Volume main/sub/mix (2-4)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
		0	0	0	0	0	0	+0dB
		0	0	0	0	0	1	+1dB
		:	:	:	:	:	:	:
		0	0	1	1	1	1	+15dB
		0	1	0	0	0	0	+16dB
		:	:	:	:	:	:	:
		0	1	0	1	1	1	+23dB
		0	1	1	0	0	0	Not used
-	-	:	:	:	:	:	:	:
		0	1	1	1	1	1	Not used
		1	0	0	0	0	0	-0dB
		:	:	:	:	:	:	:
		1	0	1	1	1	1	-15dB
		:	:	:	:	:	:	:
		1	1	0	1	1	1	-<u>23dB</u>
		:	:	:	:	:	:	:
		1	1	1	1	1	1	Not used
								Volume soft-step
-	0	-	-	-	-	-	-	On
	1							<u>Off</u>
								Soft-step action
0	-	-	-	-	-	-	-	act
1								<u>wait</u>

Table 11. Soft-step (5)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Loudness soft-step** On Off
-	-	-	-	-	-	0 1	-	**Treble soft-step** On Off
-	-	-	-	-	0 1	-	-	**Middle soft-step** On Off
-	-	-	-	0 1	-	-	-	**Bass soft-step** On Off
-	-	-	0 1	-	-	-	-	**Speaker0/Mixing soft-step** (1) On Off
-	-	0 1	-	-	-	-	-	**Speaker1 soft-step** On Off
-	0 1	-	-	-	-	-	-	**Speaker2 soft-step** On Off
0 1	-	-	-	-	-	-	-	**Soft-step time** 7.5ms 15ms

1. Mixing soft-step need to be turned on/off with speaker0 soft-step.

Table 12. Soft-mute I (6)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	x	x	x	x	**Not used**
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**Soft-mute time (Main/SUB)** 0.5ms 4ms 8ms 16ms
0 0 1 1	0 1 0 1	-	-	-	-	-	-	**Soft-mute time (Speaker0/1/2)** 4ms 8ms 32ms 64ms

Table 13. Soft-mute II / middle (7)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Pin influence for mute** Pin and IIC IIC
-	-	-	-	-	-	0 1	-	**Auto-mute** On Off
-	-	-	-	-	0 1	-	-	**Soft-mute main** On Off
-	-	-	-	0 1	-	-	-	**Soft-mute sub** On Off
-	-	-	0 1	-	-	-	-	**Soft-mute Speaker0** On Off
-	-	0 1	-	-	-	-	-	**Soft-mute Speaker1** On Off
-	0 1	-	-	-	-	-	-	**Soft-mute Speaker2** On Off
0 1	-	-	-	-	-	-	-	**Middle quality factor** 1.0 2.0

Table 14. Loudness (8)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	0 0 : 1 1	0 0 : 1 1	0 0 : 1 1	0 1 : 0 1	**Attenuation** 0dB -1dB : -14dB -15dB
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**Center frequency** Flat 400Hz 800Hz 2400Hz
-	0 1	-	-	-	-	-	-	**High boost** On Off
0 1	-	-	-	-	-	-	-	**Soft**-step action act wait

Table 15. Treble filter (9)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	0 : 0 : 0 0 1 1 : 1 : 1	1 ; 1 : 0 0 0 0 : 1 : 1	1 : 0 : 0 0 0 0 : 0 : 1	1 : 1 : 0 0 0 0 : 1 : 1	1 : 0 : 1 0 0 1 : 0 : 1	**Gain/Attenuation** +15dB : +10dB : +1dB 0dB 0dB -1dB : -10dB : -15dB
-	0 0 1 1	0 1 0 1	-	-	-	-	-	**Treble center frequency** 10.0kHz 12.5kHz 15.0kHz 17.5kHz
0 1	-	-	-	-	-	-	-	**Soft-step action** act wait

Table 16. Middle filter (10)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
			0	1	1	1	1	+15dB
			:	;	:	:	:	:
			0	1	0	1	0	+10dB
			:	:	:	:	:	:
			0	0	0	0	1	+1dB
-	-	-	0	0	0	0	0	0dB
			1	0	0	0	0	0dB
			1	0	0	0	1	-1dB
			:	:	:	:	:	:
			1	1	0	1	0	-10dB
			:	:	:	:	:	:
			1	1	1	1	1	-15dB
								Middle center frequency
	0	0						500Hz
-	0	1	-	-	-	-	-	1000Hz
	1	0						1500Hz
	1	1						2000Hz
								Soft-step action
0	-	-	-	-	-	-	-	act
1								wait

Table 17. Bass filter (11)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
			0	1	1	1	1	+15dB
			0	1	1	1	0	+14dB
			:	:	:	:	:	:
			0	0	0	0	1	+1dB
-	-	-	0	0	0	0	0	0dB
			1	0	0	0	0	0dB
			1	0	0	0	1	-1dB
			:	:	:	:	:	:
			1	1	1	1	0	-14dB
			1	1	1	1	1	-15dB
								Bass quality factor
	0	0						1.0
-	0	1	-	-	-	-	-	1.25
	1	0						1.5
	1	1						2.0
								Soft-step action
0	-	-	-	-	-	-	-	act
1								wait

Table 18. Bass / low pass filter (12)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Bass center frequency
					0	0	0	60Hz
					0	0	1	70Hz
					0	1	0	80Hz
-	-	-	-	-	0	1	1	100Hz
					1	0	0	110Hz
					1	0	1	120Hz
					1	1	0	130Hz
					1	1	1	150Hz
								Bass DC mode
-	-	-	-	0	-	-	-	On
				1				Off
								Low pass filter corner frequency
	0	0	0					50Hz
	0	0	1					60Hz
-	0	1	0	-	-	-	-	80Hz
	0	1	1					100Hz
	1	x	x					120Hz
								Low pass filter output phase
0	-	-	-	-	-	-	-	180 deg
1								0 deg

Table 19. High pass filter (13)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-		**HPF output phase Speaker0**
							0	180 deg
							1	0 deg
-	-	-	-				-	**HPF corner frequency Speaker0**
				0	0	0		50Hz
				0	0	1		60Hz
				0	1	0		80Hz
				0	1	1		100Hz
				1	0	0		120Hz
				1	0	1		150Hz
				1	1	0		180Hz
				1	1	1		220Hz
-	-	-		-	-	-		**HPF phase Speaker1**
			0					180 deg
			1					0 deg
								HPF corner frequency Speaker1
0	0	0						50Hz
0	0	1						60Hz
0	1	0						80Hz
0	1	1	-	-	-	-	-	100Hz
1	0	0						120Hz
1	0	1						150Hz
1	1	0						180Hz
1	1	1						220Hz

Table 20. Speaker0/1 source selector (14)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-		0 0 0 0 1	0 0 1 1 x	0 1 0 1 x	**Speaker0 source selector** acin0 acin1 acin2 sub main
-	-	-	-	0 1	-	-		**High pass filter bypass Speaker0** Bypass High pass filter
-	0 0 0 0 1	0 0 1 1 x	0 1 0 1 x	-	-	-	-	**Speaker1 source selector** acin0 acin1 acin2 sub main
0 1	-	-	-	-	-	-	-	**High pass filter bypass Speaker1** Bypass High pass filter

Table 21. Output gain / speaker2 source selector (15)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Pin Influence for output DC level select** Pin IIC
-	-	-	-	-	-	0 1	-	**Output DC level** 4V (AC Gain = 5dB) 5.75V (AC Gain = 8dB)
-	-	-	0 0 0 0 1	0 0 1 1 x	0 1 0 1 x	-	-	**Speaker2 source selector** acin0 acin1 acin2 sub main
	0 0 1	0 1 x						**Low pass filter bypass** Low pass filter Mono-sum bypass Stereo bypass
x								**Not used**

Table 22. Speaker attenuation (0L/0R/1L/1R/2L/2R) (16-21)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
	0	0	0	0	0	0	0	+0dB
	0	0	0	0	0	0	1	+1dB
	:	:	:	:	:	:	:	:
	0	0	0	1	1	1	1	+15dB
	0	0	1	0	0	0	0	+16dB
	:	:	:	:	:	:	:	:
	0	0	1	0	1	1	1	+23dB
	0	0	1	1	0	0	0	Not used
	:	:	:	:	:	:	:	:
	0	0	1	1	1	1	1	Not used
-	0	1	0	0	0	0	0	-0dB
	:	:	:	:	:	:	:	:
	0	1	0	1	1	1	1	-15dB
	:	:	:	:	:	:	:	:
	0	1	1	0	1	1	1	-23dB
	:	:	:	:	:	:	:	:
	1	0	0	0	0	0	0	-32dB
	:	:	:	:	:	:	:	:
	1	1	0	0	0	0	0	-64dB
	:	:	:	:	:	:	:	:
	1	1	0	1	1	1	1	-79dB
	1	1	1	x	x	x	x	mute
								Soft-step action
0	-	-	-	-	-	-	-	act
1								wait

Table 23. Auto-mix I (22)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Auto mix programmable attenuation
			0	0	0	0	0	0dB
			0	0	0	0	1	-1dB
			:	:	:	:	:	:
			0	1	1	1	0	-14dB
			0	1	1	1	1	-15dB
-	-	-	:	:	:	:	:	:
			1	0	0	1	1	-19dB
			1	0	1	0	0	-20dB
			1	0	1	0	1	Reserved
			1	0	1	1	0	Reserved
			1	0	1	1	1	Reserved
			1	1	x	x	x	Reserved
								Auto mix detect threshold
0	0	0						5mv
0	0	1						10mv
0	1	0						15mv
0	1	1	-	-	-	-		20mv
1	0	0						25mv
1	0	1						50mv
1	1	0						75mv
1	1	1						100mv

Table 24. Auto-mix II (23)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Auto mix release time
					0	0	0	125ms
					0	0	1	250ms
					0	1	0	500ms
-	-	-	-	-	0	1	1	1000ms
					1	0	0	2000ms
					1	0	1	4000ms
					1	1	x	4000ms
								Auto mix attach time
		0	0	0				0.5ms
		0	0	1				1ms
		0	1	0				2ms
-	-	0	1	1	-	-	-	4ms
		1	0	0				8ms
		1	0	1				16ms
		1	1	x				16ms
								Mix mode (1)
-	0	-	-	-	-	-	-	Auto mix
	1							IIC
x	-	-	-	-		-	-	Not used

1. When mix mode is changed, byte 24 need to be sent as well.

Table 25. Auto-mix III (24)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**IIC mix speaker0** Bypass Mix
-	-	-	-	-	-	0 1	-	**Mix gain speaker0** 0dB (-6dB/-6dB mix) 6dB (0dB/0dB mix)
-	-	-	-	-	0 1	-	-	**IIC mix speaker1** Bypass Mix
-	-	-	-	0 1	-	-	-	**Mix gain speaker1** 0dB (-6dB/-6dB mix) 6dB (0dB/0dB mix)
-	-	0 0 1	0 1 x	-	-	-	-	**Auto mix detection input** Mix left channel Mix right channel Mix mono-sum
-	x	-	-	-	-	-	-	**Not used**
0 1	-	-	-	-	-	-	-	**Soft-step action** act wait

Table 26. DC-detector/speaker-limiter (25)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	0 0 1 1	0 1 0 1	**Spike rejection time** Disable 11 µs 22 µs 33 µs
-	-	-	-	0 0 1 1	0 1 0 1	-	-	**Zero-comparator Window size** ±120mV ±90mV ±60mV ±30mV
-	-	-	0 1	-	-	-	-	**DC-detector fast charge** On Off
-	0 0 1 1	0 1 0 1	-	-	-	-	-	**Speaker-limiter threshold** 1.5Vpp 3Vpp 4Vpp Off
x	-	-	-	-	-	-	-	**Not used**

Table 27. Spectrum analyzer (26)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Spectrum analyzer source selector** Main path Speaker0
-	-	-	-	-	-	0 1	-	**Run/Stop** Run Stop
-	-	-	-	-	0 1	-	-	**Reset mode** SARST-pin triggered reset Auto-reset mode
-	-	-	-	0 1	-	-	-	**Spectrum analyzer filter quality factor** 3.5 1.75
-	-	0 0 1 1	0 1 0 1	-	-	-	-	**Spectrum analyzer in-gain** 0dB 2dB 4dB 6dB
x	x	-	-	-	-	-	-	**Not used**

Table 28. Test I (27)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-		**Audio processor testing mode**
							0	Off
							1	On
								Test multiplexer (1)
		0	0	0	0	0		SSCLK
		0	0	0	0	1		SMCLK1
		0	0	0	1	0		SMCLK2
-	-	0	0	0	1	1	-	VDDd
		0	0	1	0	0		VDDa
		0	0	1	0	1		Clock200k
		0	0	1	1	0		SDCLK
		0	0	1	1	1		REQ_TEST
								SA / Auto-mix test multiplexer (1)
		0	1	0	0	0		Spec.Anal. AAF
		0	1	0	0	1		Spec.Anal. BPF1
		0	1	0	1	0		Spec.Anal. BPF2
-	-	0	1	0	1	1	-	Spec.Anal. BPF3
		0	1	1	0	0		Auto-mix Rectifier output
		0	1	1	0	1		Auto-mix attach clock
		0	1	1	1	0		Auto-mix release clock
		0	1	1	1	1		Auto-mix Vth
								DCO test multiplexer (1)
		1	0	0	0	0		Vthp Comp. Left
		1	0	0	0	1		Vthn Comp. Left
		1	0	0	1	0		Vthp Comp. Right
-	-	1	0	0	1	1	-	Vthn Comp. Right
		1	0	1	0	0		Vthp reference
		1	0	1	0	1		Vthn reference
		1	0	1	1	0		IntZeroErr
		1	0	1	1	1		Vref
								Auto-mix rectifier bypass (1)
-	0	-	-	-	-	-	-	On
	1							Off
x	-	-	-	-	-	-	-	**Not used**

1. The control bit needs both I²C test mode on & sub-address test mode on.

Table 29. Test II (28)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	0 0 1 1	0 1 0 1	**Manual set busy signal** (1) Auto Auto 0 1
-	-	-	-	-	-	0 0 1 1	0 1 0 1	**Request for clock generator** (1) Allow Allow Stopped Stopped
-	-	-	-	-	0 1	-	-	**Clock source** (2) External Internal (200kHz)
-	-	-	-	0 1	-	-	-	**Oscillator clock** (2), (3) 400kHz 800kHz
-	-	-	0 1	-	-	-	-	**Clock fast mode**(2) On Off
-	-	0 1	-	-	-	-	-	**Soft-step curve** (2) S-Curve (soft step time 7.5ms/15ms) Linear Curve (soft step time 5ms/10ms)
x	x	-	-	-	-	-	-	**Not used**

1. The control bit needs sub-address test mode on.
2. The control bit does not depend on test mode.
3. Oscillator clock frequency is not suggested to change, the change will influence auto mix attach time.

Table 30. Test III (29)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	**Test architecture** (1) Normal Split
-	-	-	-	-	-	0 1	-	**Attenuators gain clock control** (2) On Off
-	-	-	-	-	0 1	-	-	**Enable clock for speaker volume** On Off
-	-	-	-	0 1	-	-	-	**Enable clock for volume** On Off
-	-	-	0 1	-	-	-	-	**Enable clock for treble & bass** On Off
-	-	0 1	-	-	-	-	-	**Enable clock for loudness & middle** On Off
x	x	-	-	-	-	-	-	**Not used**

1. The control bit needs sub-address test mode on.
2. The control bit does not depend on test mode.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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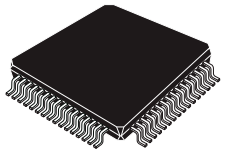
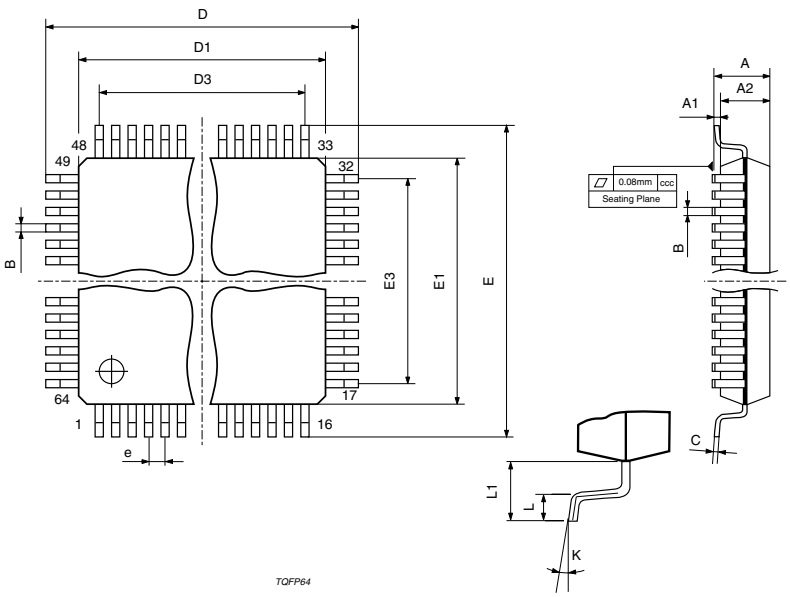
Figure 27. LFQP64 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0106
C	0.09		0.20	0.0035		0.0079
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0° (min.), 3.5° (min.), 7°(max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DAT A



LQFP64 (10 x 10 x 1.4mm)



GAPGPS00365

7 Revision history

Table 31. Document revision history

Date	Revision	Changes
05-Dec-2012	1	Initial release.
15-May-2013	2	Updated: *Table 5: Electrical characteristics*; *Section 4.12: Spectrum analyzer on page 29*.
16-Sept-2013	3	Updated Disclaimer

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