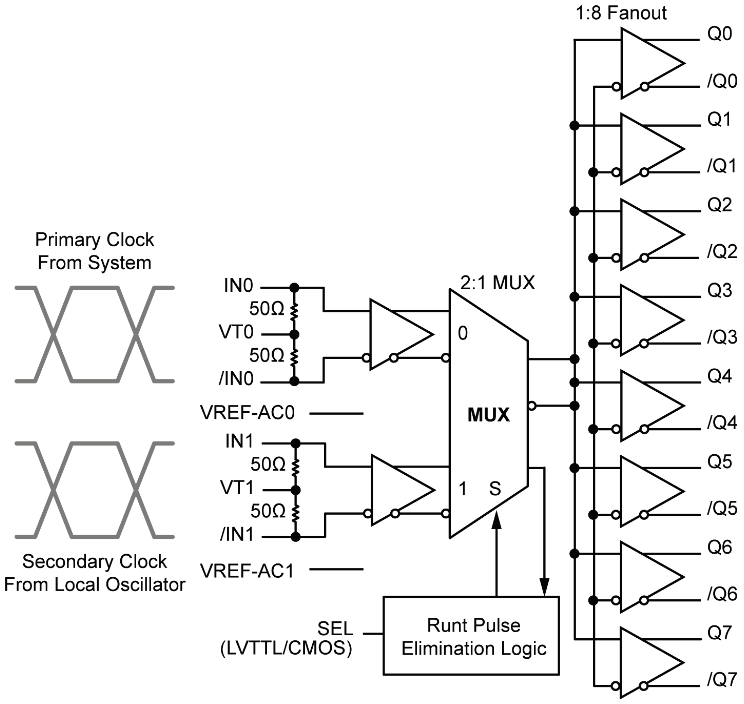
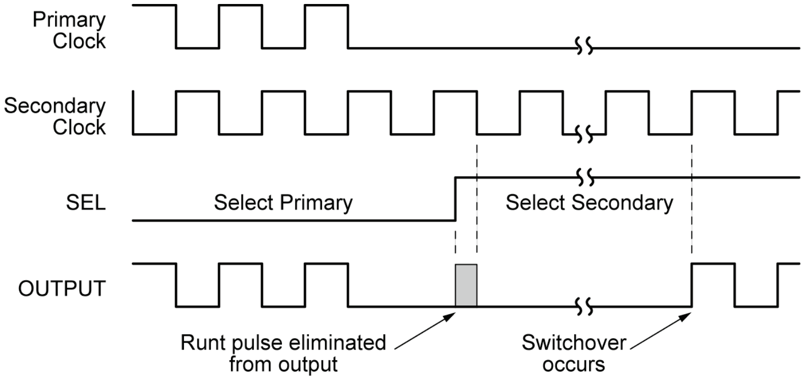
Typical Application





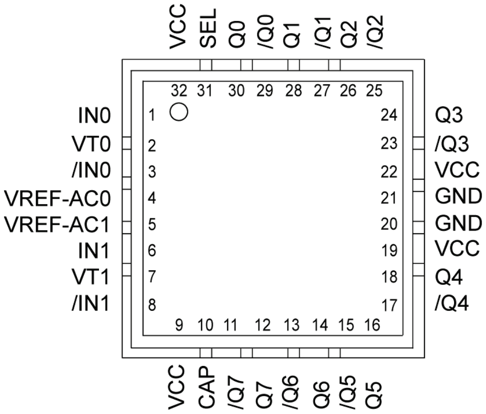
Ordering Information[1]

Part Number	**Package Type**	**Operating Range**	**Package Marking**	**Lead Finish**
SY89838UMG	QFN-32	Industrial	SY89838U with bar line Pb-Free indicator	NiPdAu Pb-Free
SY89838UMGTR(2)	QFN-32	Industrial	SY89838U with bar line Pb-Free indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = +25°C, DC Electrical only.
2. Tape and Reel.

Pin Configuration



32-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
1, 3, 6, 8	IN0, /IN0, IN1, /IN1	Differential Inputs: These input pairs are the differential signal inputs to the device. These inputs accept AC or DC-coupled signals as small as 100mV (200mV$_{PP}$). Each pin of a pair internally terminates to a VT pin through 50Ω. Please refer to the "Input Interface Applications" section for more details.
2, 7	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT0 and VT1 pins provide a center-tap to a termination network for maximum interface flexibility. See the "Input Interface Applications" section for more details.
31	SEL	This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. Input threshold is V$_{CC}$/2.
9, 19, 22, 32	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to VCC pins as possible.
30, 28, 26, 24, 18, 16, 14, 12, 29, 27, 25, 23, 17, 15, 13, 11	Q0 – Q7, /Q0 – /Q7	Differential Outputs: These LVDS output pairs are a logic function of the IN0, IN1, and SEL inputs. Please refer to the truth table below for details. Unused output pairs must be terminated with 100Ω across the pair.
20, 21	GND, Exposed Pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.
10	CAP	Power-On Reset (POR) Initialization capacitor. When using the multiplexer with RPE capability, this pin is tied to a capacitor to VCC. The purpose is to ensure the internal RPE logic starts up in a known state. See "Power-On Rest (POR) Description" section for more details regarding capacitor selection. If this pin is tied directly to VCC, the RPE function will be disabled and the multiplexer will function as a normal multiplexer. The CAP pin should never be left open.
4, 5	VREF-AC0 VREF-AC1	Reference Voltage: These outputs bias to V$_{CC}$–1.2V. They are used for AC-coupling inputs (IN, /IN). Connect VREF_AC directly to the VT pin. Bypass with 0.01µF low ESR capacitor to VCC. See "Input Interface Applications" section. Maximum sink/source current is ±1.5mA.

Truth Table

Inputs					Outputs	
IN0	**/IN0**	**IN1**	**/IN1**	**SEL**	**Q**	**/Q**
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

Absolute Maximum Ratings(1)

Supply Voltage (V_{CC}) ....-0.5V to +4.0V
Input Voltage (V_{IN}) .... -0.5V to V_{CC}
Input Current
  Source or sink current on IN, /IN............. ±50mA
Termination Current
  Source or sink current on V_T .... ±100mA
V_{REF-AC} Source or sink current .... ±2mA
Lead Temperature (soldering, 20 sec.) ....+260°C
Storage Temperature (T_s)..................–65°C to 150°C

Operating Ratings(2)

Supply Voltage (V_{CC}).................. +2.375V to +2.625V
Ambient Temperature (T_A) .... –40°C to +85°C
Package Thermal Resistance(3)
QFN (θ_{JA})
  Still-Air .... 35°C/W
QFN (ψ_{JB})
  Junction-to-Board .... 16°C/W

DC Electrical Characteristics(4)

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		250	350	mA
R_{IN}	Input Resistance (IN-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input High Voltage (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH}–0.2	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a. Note 5	0.2		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN-/IN|	See Figure 1b.	0.4			V
V_{IN_FSI}	Input Voltage Threshold that Triggers FSI			30	100	mV
V_{T_IN}	IN-to-V_T (IN, /IN)				1.8	V
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} values are determined for a 4-layer board in still air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IN} (max) is specified when V_T is floating.

LVDS Outputs DC Electrical Characteristics(6)

V_{CC} = +2.5V ±5%; T_A = –40°C to + 85°C; R_L = 100Ω across output pair, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing (Q, /Q)	See Figure 1a and 4a	250	325		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing |Q - /Q|	See Figure 1b	500	650		mV
V_{OCM}	Output Common Mode Voltage	See Figure 4b	1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage	See Figure 4b	–50		+50	mV

LVTTL/CMOS DC Electrical Characteristics(6)

V_{CC} = +2.5V ±5%; T_A = –40°C to + 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current		–300			µA

Note:

1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics(6)

V_{CC} = +2.5V ±5%; T_A = –40°C to +85°C, RPE enabled, Input t_r/t_f ≤ 600ps (20% to 80%), R_L = 100Ω, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	RPE enabled	1.5	2.0		GHz
t_{pd}	Differential Propagation Delay IN-to-Q	V_{IN} ≥ 250mV, Note 7	500	700	950	ps
	SEL-to-Q	RPE enabled, see Timing Diagram			17	Cycles
	SEL-to-Q	RPE disabled (V_{IN} = $V_{CC}/2$)			1000	ps
t_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			115		fs/°C
t_{skew}	Output-to-Output Skew	Note 8		20	40	ps
	Part-to-Part Skew	Note 9			200	ps
t_{Jitter}	RMS Phase Jitter	Output = 622MHz Integration range: 12kHz – 20MHz		150		fs
	Crosstalk-Induced Jitter	Note 10			0.7	ps_{RMS}
t_R, t_F	Output Rise/Fall Time (20% to 80%)	At full output swing.	40	80	150	ps

Notes:

6. High-frequency AC-parameters are guaranteed by design and characterization.
7. Propagation delay is a function of rise and fall time at IN. See “Typical Operating Characteristics” for more details.
8. Output-to-output skew is measured between two different outputs under identical transitions.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
10. Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

Functional Description

RPE MUX and Fail-Safe Input

The SY89838U is optimized for clock switchover applications where switching from one clock to another clock without runt pulses (short cycles) is required. It features two unique circuits:

Runt-Pulse Eliminator (RPE) Circuit:

The RPE MUX provides a “glitchless” switchover between two clocks and prevents any runt pulses from occurring during the switchover transition. The design of both clock inputs is identical (i.e., the switchover sequence and protection is symmetrical for both input pair, IN0 or IN1. Thus, either input pair may be defined as the primary input). If not required, the RPE function can be permanently disabled to allow the switchover between inputs to occur immediately. If the CAP pin is tied directly to V_{CC}, the RPE function will be disabled and the multiplexer will function as a normal multiplexer.

Fail-Safe Input (FSI) Circuit:

The FSI function provides protection against a selected input pair that drops below the minimum amplitude requirement. If the selected input pair drops sufficiently below the 100mV minimum single-ended input amplitude limit (V_{IN}), or 200mV differentially (V_{DIFF_IN}), the output will latch to the last valid clock state.

RPE and FSI Functionality

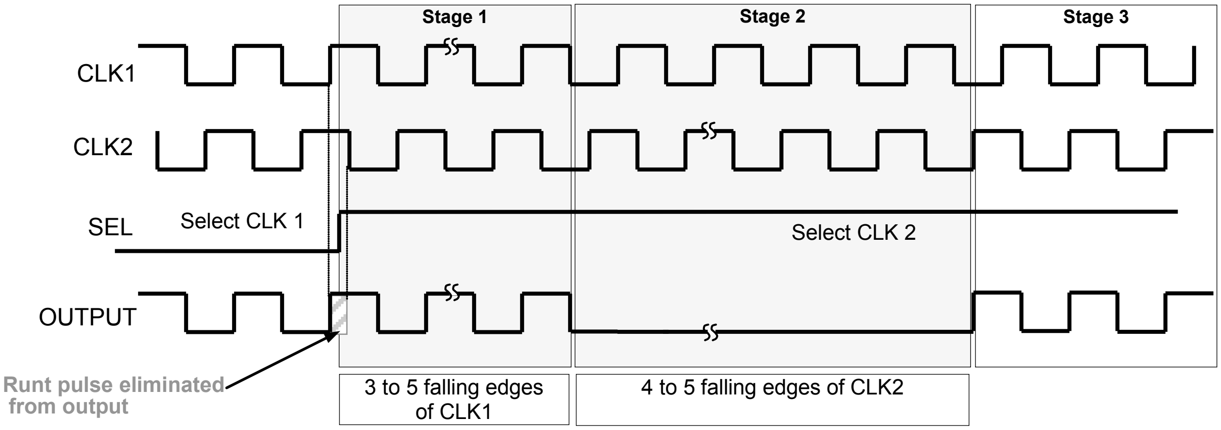
The basic operation of the RPE MUX and FSI functionality is described with the following four case descriptions. All descriptions are related to the true inputs and outputs. The primary (or selected) clock is called CLK1; the secondary (or alternate) clock is called CLK2. Due to the totally asynchronous relation of the IN and SEL signals and an additional internal protection against metastability, the number of pulses required for the operations described in cases 1-4 can vary within certain limits. Refer to “Timing Diagrams” for more detailed information.

Case #1 Two Normal Clocks and RPE Enabled

In this case the frequency difference between the two running clocks IN0 and IN1 must not be greater than 1.5:1. For example, if the IN0 clock is 500MHz, the IN1 clock must be within the range of 334MHz to 750MHz.

If the SEL input changes state to select the alternate clock, the switchover from CLK1 to CLK2 will occur in three stages.

- Stage 1: The output will continue to follow CLK1 for a limited number of pulses.
- Stage 2: The output will remain LOW for a limited number of pulses of CLK2.
- Stage 3: The output follows CLK2.

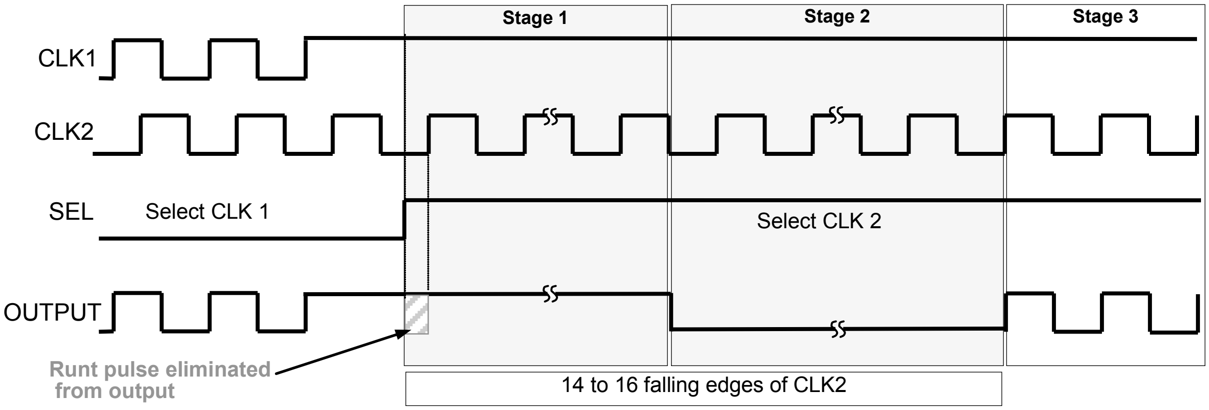


Case #2 Input Clock Failure: Switching from a selected clock stuck HIGH to a valid clock (RPE enabled)

If CLK1 fails HIGH before the RPE MUX selects CLK2 (using the SEL pin), the switchover will occur in three stages.

- Stage 1: The output will remain HIGH for a limited number of pulses of CLK2.
- Stage 2: The output will switch to LOW and then remain LOW for a limited number of falling edges of CLK2.

1. Stage 3: The output will follow CLK2.

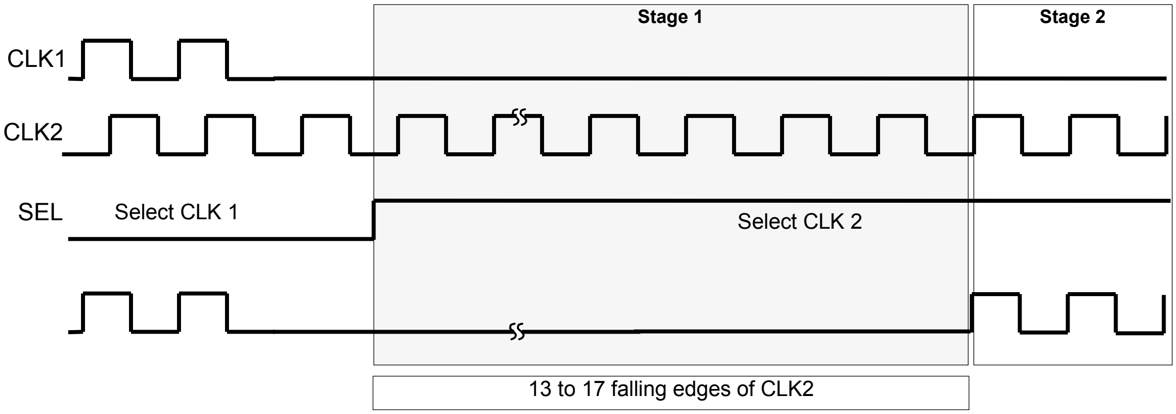


Note: Output shows extended clock cycle during switchover. Pulse width for both high and low of this cycle will always be greater than 50% of the CLK2 period.

Case #3 Input Clock Failure: Switching from a selected clock stuck Low to a valid clock (RPE enabled)

If CLK1 fails LOW before the RPE MUX selects CLK2 (using the SEL pin), the switchover will occur in two stages.

- Stage 1: The output will remain LOW for a limited number of falling edges of CLK2.
- Stage 2: The output will follow CLK2.

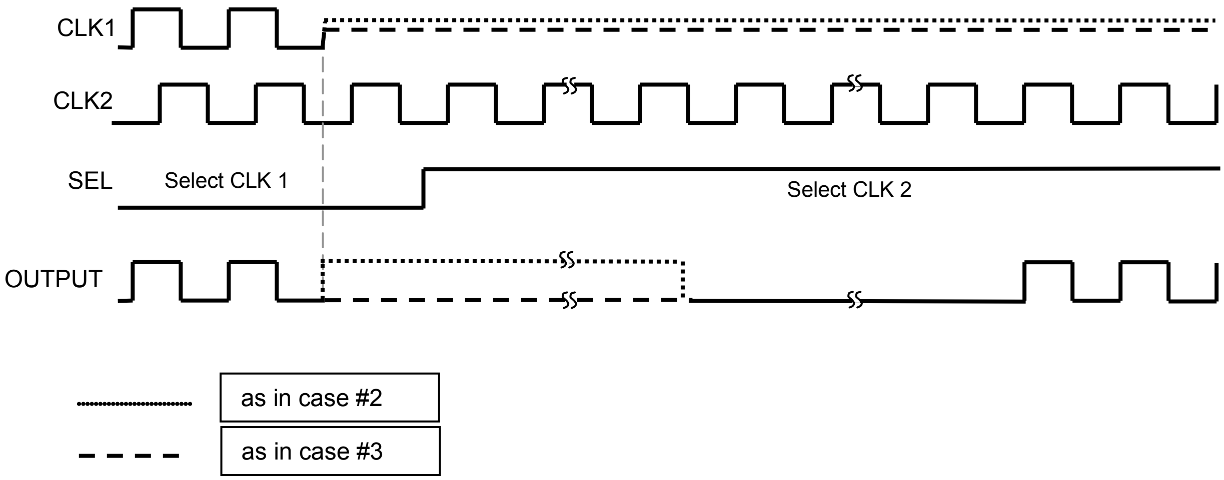


Case #4 Input Clock Failure: Switching from the selected clock input stuck in an undetermined state to a valid clock input (RPE enabled)

If CLK1 fails to an undetermined state (e.g., amplitude falls below the 100mV (V_{IN}) minimum single-ended input limit, or 200mV differentially) before the RPE MUX selects CLK2 (using the SEL pin), the switchover to the valid clock CLK2 will occur either following Case #2 or Case #3, depending on the last valid state at the CLK1.

If the selected input clock fails to a floating, static, or extremely low signal swing, including 0mV, the FSI function will eliminate any metastable condition and guarantee a stable output signal. No ringing and no undetermined state will occur at the output under these conditions.

Please note that the FSI function will not prevent duty cycle distortions or runt pulses in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to "Typical Operating Characteristics" for more detailed information.



Power-On Reset (POR) Description

The SY89838U includes an internal power-on reset (POR) function to ensure the RPE logic starts-up in a known logic state once the power-supply voltage is stable. An external capacitor connected between V_{CC} and the CAP pin (pin 10) controls the delay for the power-on reset function.

Calculation of the required capacitor value is based on the time the system power supply needs to power up to a minimum of 2.3V. The time constant for the internal power-on-reset must be greater than the time required for the power supply to ramp up to a minimum of 2.3V.

The following formula describes this relationship:

$$C(\mu F) \geq \frac{t_{dPS}(ms)}{12(ms/\mu F)}$$

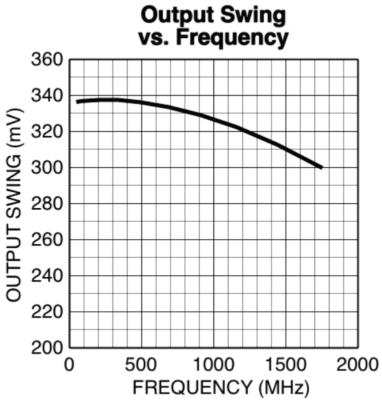
As an example, if the time required for the system power supply to power up past 2.3V is 12ms, the required capacitor value on pin 10 would be:

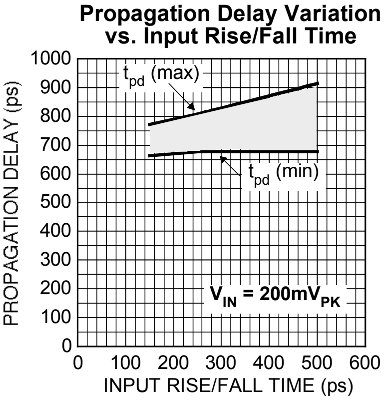
$$C(\mu F) \geq \frac{12ms}{12(ms/\mu F)}$$

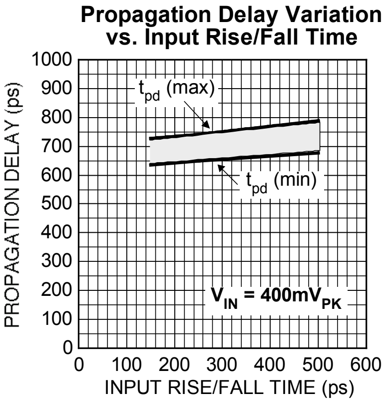
$$C(\mu F) \geq 1\mu F$$

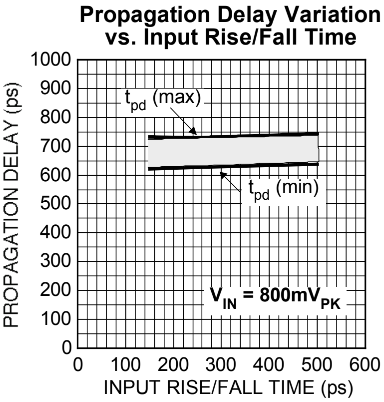
Typical Operating Characteristics

V_{CC} = 2.5V, GND = 0V, $V_{IN} \geq 250mV_{pk}$, $t_r/t_f \leq 300ps$, $R_L = 100\Omega$ across output pair; T_A = 25°C, unless otherwise stated.









Singled-Ended and Differential Swings

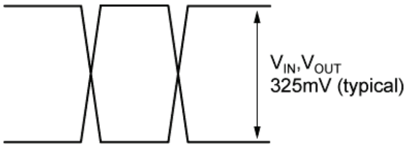


Figure 1a. Singled-Ended Voltage Swing

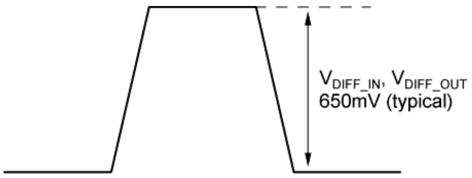


Figure1b. Differential Voltage Swing

Input Stage

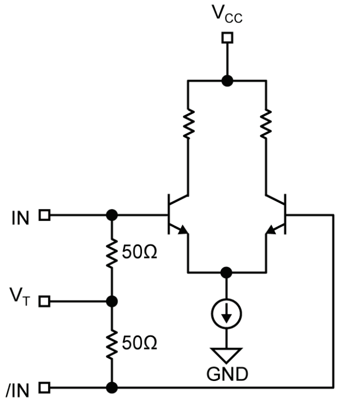
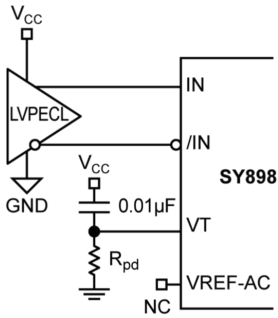


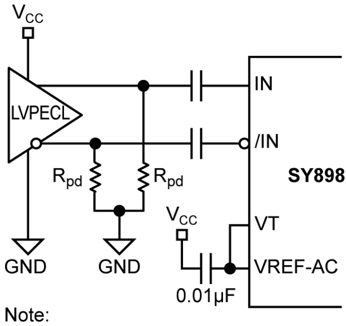
Figure 2. Simplified Differential Input Stage

Input Interface Applications



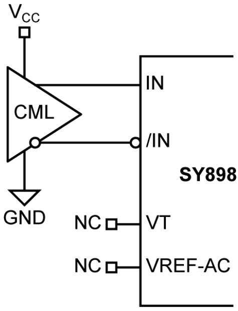
Note:
For 3.3V, R_{pd} = 50Ω.
For 2.5V, R_{pd} = 19Ω.

Figure 3a. LVPECL Interface (DC-Coupled)



Note:
For 3.3V, R_{pd} = 100Ω.
For 2.5V, R_{pd} = 50Ω.

Figure 3b. LVPECL Interface (AC-coupled)



option: may connect V_T to V_{CC}

Figure 3c. CML Interface (DC-Coupled)

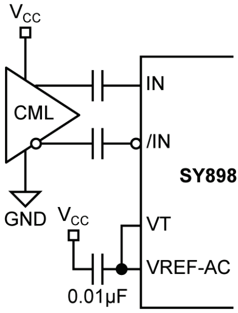


Figure 3d. CML Interface (AC-Coupled)

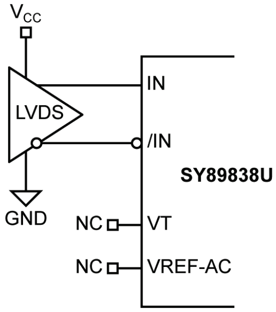


Figure 3e. LVDS Interface (DC-Coupled)

LVDS Output Interface Applications

LVDS specifies a small swing of 325mV typical, on a nominal 1.2V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

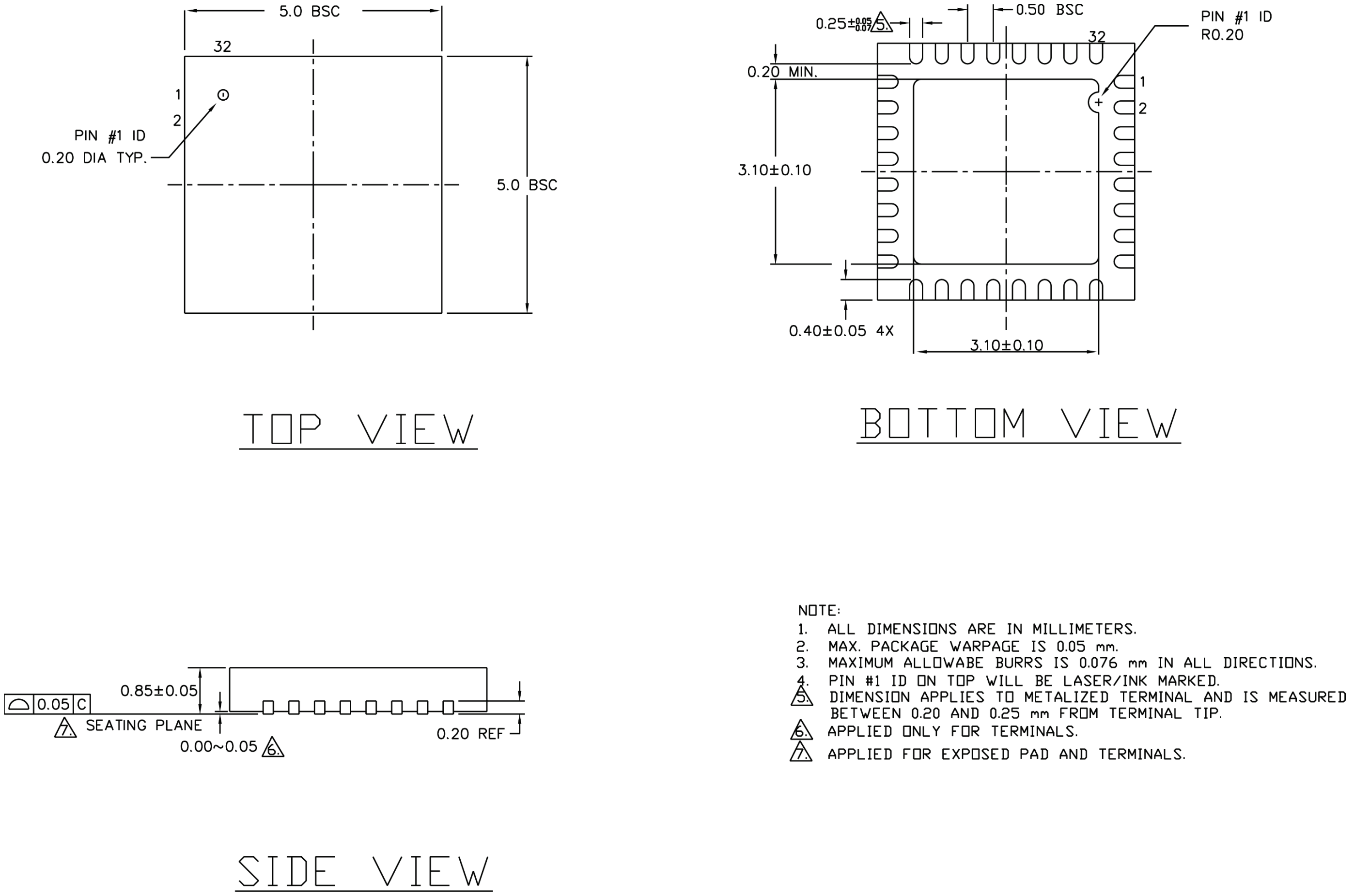
Figure 4a. LVDS Differential Measurement

Figure 4b. LVDS Common Mode Measurement

Related Product and Support Documentation

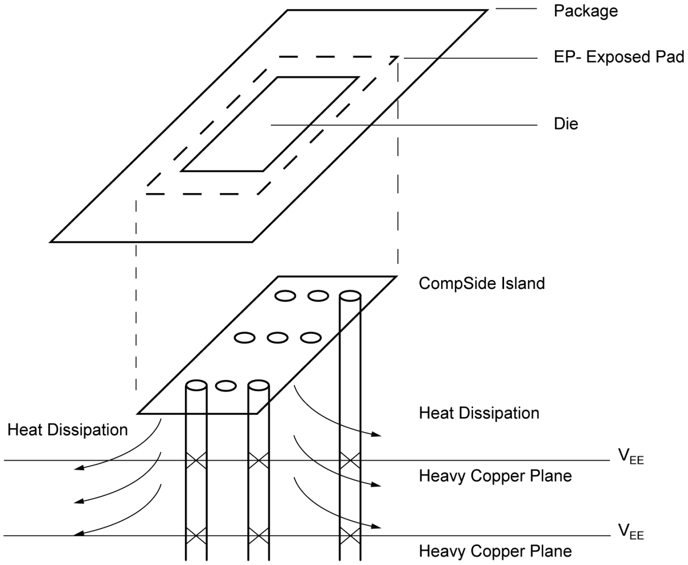
Part Number	Function	Data Sheet Link
SY89837U	Presision 1:8 LVPECL Fanout Buffer with 2:1 Runt Pulse Eliminator Input Mux	www.micrel.com/_PDF/HBW/SY89837u.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Package Information



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

32-Pin (5mm x 5mm) QFN



PCB Thermal Consideration for 32-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.