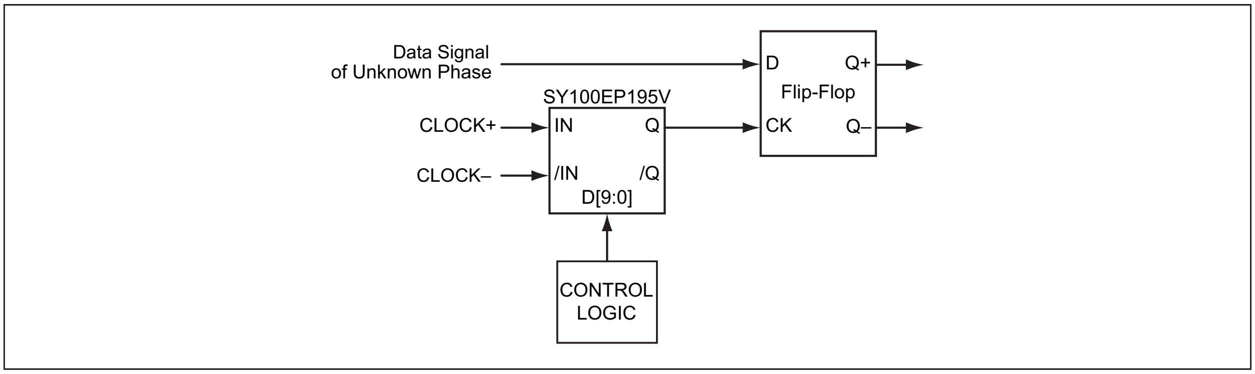
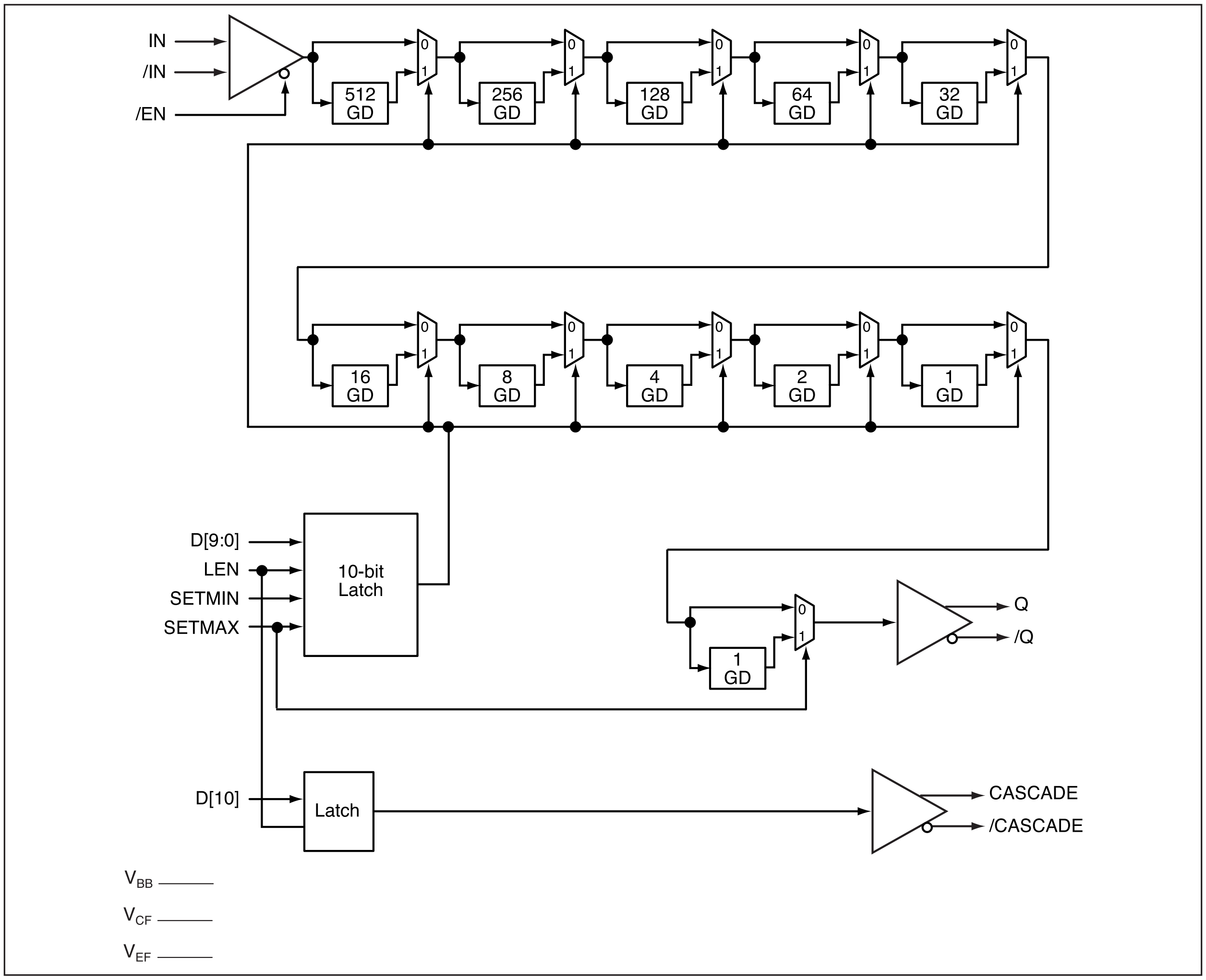
Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) PECL Mode (V_{EE} = 0V) .... –0.5V to +6.0V
Supply Voltage (V_{EE}) NECL Mode (V_{CC} = 0V) .... +0.5V to –6.0V
Any Input Voltage (V_{IN})
PECL Mode .... –0.5V to V_{CC} + 0.5V
NECL Mode .... +0.5V to V_{EE} – 0.5V
ECL Output Current (I_{OUT})
Continuous .... 50 mA
Surge .... 100 mA
I_{BB} Sink/Source Current .... ±0.5 mA
ESD Rating (Note 1) .... >1.5 kV

Operating Ratings ‡

Supply Voltage (V_{CC}) PECL Mode (V_{EE} = 0V) .... +3.0V to +5.5V
Supply Voltage (V_{EE}) NECL Mode (V_{CC} = 0V) .... –3.0V to –5.5V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions recommended.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = –40°C to +85°C, unless otherwise stated.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply Voltage (PECL)	V_{CC}	3.0	3.3	3.6	V	—
		4.5	5.0	5.5		
Power Supply Voltage (NECL)	V_{EE}	–3.6	–3.3	–3.0	V	—
		–5.5	–5.0	–4.5		
Power Supply Current (Note 1)	I_{EE}	—	150	175	mA	No load, over supply voltage

Note 1: Required 500 lfpm air flow when using +5V or –5V power supply.

LVPECL DC ELECTRICAL CHARACTERISTICS (100KEP)

Electrical Characteristics: V_{CC} = 3.3V, V_{EE} = 0V; T_A = –40°C to +85°C. (Note 1, Note 2)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output High Voltage	V_{OH}	2155	2280	2405	mV	Figure 7-1, All loading with 50Ω to V_{CC} – 2V
Output Low Voltage	V_{OL}	1355	1480	1605	mV	Figure 7-1, All loading with 50Ω to V_{CC} – 2V
PECL Input High Voltage	V_{IH}	2075	—	2420	mV	Figure 7-3, Figure 7-4
CMOS Input High Voltage		1815	—	—		
TTL Input High Voltage		2000	—	—		
PECL Input Low Voltage	V_{IL}	1355	—	1675	mV	Figure 7-3, Figure 7-4
CMOS Input Low Voltage		—	—	1485		
TTL Input Low Voltage		—	—	800		
Output Voltage Reference	V_{BB}	1775	1875	1975	mV	—
Input Select Voltage	V_{CF}	1610	1720	1825	mV	—
Mode Connection	V_{EF}	1900	2000	2100	mV	—
Input High Voltage Common Mode Range (Note 3)	V_{IHCMR}	2.0	—	3.3	V	Figure 7-6
Input High Current	I_{IH}	—	—	150	µA	—
Input Low Current	I_{IL}	0.5	—	—	µA	IN
		–150	—	—		/IN

Note 1: Device is guaranteed to meet the DC specifications shown in the table after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of ≥500 lfpm is maintained.

2: Input and output parameters vary 1:1 with V_{CC}.

3: V_{IHCMR} maximum varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

PECL DC ELECTRICAL CHARACTERISTICS (100KEP)

Electrical Characteristics: V_{CC} = 5.0V, V_{EE} = 0V; T_A = –40°C to +85°C. (Note 1, Note 2)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	3855	3980	4105	mV	Figure 7-1, All loading with 50Ω to V_{CC} – 2V
Output Low Voltage	V_{OL}	3055	3180	3305	mV	Figure 7-1, All loading with 50Ω to V_{CC} – 2V
PECL Input High Voltage	V_{IH}	3775	—	4120	mV	Figure 7-3, Figure 7-4
CMOS Input High Voltage		2750	—	—		
TTL Input High Voltage		2000	—	—		
PECL Input Low Voltage	V_{IL}	3055	—	3375	mV	Figure 7-3, Figure 7-4
CMOS Input Low Voltage		—	—	2250		
TTL Input Low Voltage		—	—	800		
Output Voltage Reference	V_{BB}	3475	3575	3675	mV	—
Input High Voltage Common Mode Range (Note 3)	V_{IHCMR}	2.0	—	5.0	V	Figure 7-6
Input High Current	I_{IH}	—	—	150	µA	—
Input Low Current	I_{IL}	0.5	—	—	µA	IN
		–150	—	—		/IN

Note 1: Device is guaranteed to meet the DC specifications shown in the table after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of ≥500 lfpm is maintained.

2: Input and output parameters vary 1:1 with V_{CC}.

3: V_{IHCMR} maximum varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NECL DC ELECTRICAL CHARACTERISTICS (100KEP)

Electrical Characteristics: V_{CC} = 0V, V_{EE} = –5.5V to –3.0V; T_A = –40°C to +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	–1145	–1020	–895	mV	Figure 7-2, All loading with 50Ω to V_{CC} – 2V
Output Low Voltage	V_{OL}	–1945	–1820	–1695	mV	Figure 7-2, All loading with 50Ω to V_{CC} – 2V
Input High Voltage NECL	V_{IH}	–1225	—	–880	mV	Figure 7-5
Input Low Voltage NECL	V_{IL}	–1945	—	–1625	mV	Figure 7-5
Output Voltage Reference	V_{BB}	–1525	–1425	–1325	mV	—
Input High Voltage Common Mode Range ()	V_{IHCMR}	V_{EE} + 2.0	—	0.0	V	Figure 7-7
Input High Current	I_{IH}	—	—	150	µA	—
Input Low Current	I_{IL}	0.5	—	—	µA	IN
		–150	—	—		/IN

Note 1: Device is guaranteed to meet the DC specifications shown in the table after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of ≥500 lfpm is maintained.

2: V_{IHCMR} minimum varies 1:1 with V_{EE}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.0 to 5.5V, V_{EE} = 0V or V_{CC} = 0V, V_{EE} = –3.0 to –5.5V; T_A = –40°C to +85°C. (Note 1, Note 2)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Frequency	f_{MAX}	1.6	—	—	GHz	Note 3
Propagation Delay, IN-to-Q; D[0-9] = 0	t_{PD}	1650	2000	2450	ps	T_A = –40°C
		1800	2070	2600		T_A = +25°C
		1950	2150	2750		T_A = +85°C
Propagation Delay, IN-to-Q; D[0-9] = 1023		9500	10551	13500	ps	T_A = –40°C
		9800	10756	14000		T_A = +25°C
		10600	11226	15800		T_A = +85°C
Propagation Delay, /EN-to-Q; D[0-9] = 0		1600	2150	2600	ps	T_A = –40°C
		1800	2300	2800		T_A = +25°C
		2000	2430	3000		T_A = +85°C
Propagation Delay, D10 to CASCADE		300	400	500	ps	T_A = –40°C
		325	410	550		T_A = +25°C
		325	430	625		T_A = +85°C
Programmable Range	t_{RANGE}	7850	8551	—	ps	$t_{PD(MAX)} – t_{PD(MIN)}$, T_A = –40°C
		8000	8686	—		$t_{PD(MAX)} – t_{PD(MIN)}$, T_A = +25°C
		8650	9076	—		$t_{PD(MAX)} – t_{PD(MIN)}$, T_A = +85°C
Step Delay, D0 High Note 4 applies to all Step Delay entries.	Δt	—	9	—	ps	T_A = –40°C
		—	10	—		T_A = +25°C
		—	10	—		T_A = +85°C
Step Delay, D1 High		—	25	—	ps	T_A = –40°C
		—	26	—		T_A = +25°C
		—	27	—		T_A = +85°C
Step Delay, D2 High		—	42	—	ps	T_A = –40°C
		—	42	—		T_A = +25°C
		—	43	—		T_A = +85°C
Step Delay, D3 High		—	75	—	ps	T_A = –40°C
		—	80	—		T_A = +25°C
		—	81	—		T_A = +85°C
Step Delay, D4 High		—	142	—	ps	T_A = –40°C
		—	143	—		T_A = +25°C
		—	150	—		T_A = +85°C
Step Delay, D5 High		—	296	—	ps	T_A = –40°C
		—	300	—		T_A = +25°C
		—	310	—		T_A = +85°C
Step Delay, D6 High		—	532	—	ps	T_A = –40°C
		—	540	—		T_A = +25°C
		—	565	—		T_A = +85°C
Step Delay, D7 High		—	1080	—	ps	T_A = –40°C
		—	1095	—		T_A = +25°C
		—	1140	—		T_A = +85°C

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{CC} = 3.0 to 5.5V, V_{EE} = 0V or V_{CC} = 0V, V_{EE} = –3.0 to –5.5V; T_A = –40°C to +85°C. (Note 1, Note 2)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Step Delay, D8 High	Δt	—	2100	—	ps	T_A = –40°C
		—	2150	—		T_A = +25°C
		—	2250	—		T_A = +85°C
Step Delay, D9 High		—	4250	—	ps	T_A = –40°C
		—	4300	—		T_A = +25°C
		—	4500	—		T_A = +85°C
Duty Cycle Skew, $t_{PHL} – t_{PLH}$	t_{SKEW}	—	25	—	ps	T_A = +25°C, Note 5
Setup Time, D-to-LEN	t_S	200	0	—	ps	—
Setup Time, D-to-IN (Note 6)		300	140	—	ps	T_A = –40°C
		300	160	—		T_A = +25°C
		300	180	—		T_A = +85°C
Setup Time, /EN-to-IN (Note 7)		300	150	—	ps	T_A = –40°C
		300	170	—		T_A = +25°C
		300	180	—		T_A = +85°C
Hold Time, LEN-to-D	t_H	200	60	—	ps	T_A = –40°C
		200	100	—		T_A = +25°C
		200	80	—		T_A = +85°C
Hold Time, IN-to-/EN (Note 8)		400	250	—	ps	T_A = –40°C
		400	280	—		T_A = +25°C
		400	300	—		T_A = +85°C
Release Time, /EN-to-IN (Note 9)	t_R	—	500	—	ps	T_A = +25°C
Release Time, SETMAX-to-LEN		400	200	—	ps	T_A = –40°C
		400	250	—		T_A = +25°C
		400	300	—		T_A = +85°C
Release Time, SETMIN-to-LEN		350	275	—	ps	T_A = –40°C
		350	200	—		T_A = +25°C
		350	335	—		T_A = +85°C

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{CC} = 3.0 to 5.5V, V_{EE} = 0V or V_{CC} = 0V, V_{EE} = –3.0 to –5.5V; T_A = –40°C to +85°C. (Note 1, Note 2)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Cycle-to-Cycle Jitter	t_{JIT}	—	0.2	<1	ps_{RMS}	Note 10
Input Voltage Swing (Differential)	V_{PP}	150	800	1200	mV	—
Output Rise/Fall Time, 20% to 80% (Q)	t_r/t_f	—	—	150	ps	T_A = –40°C
		—	—	150		T_A = +25°C
		—	—	175		T_A = +85°C
Output Rise/Fall Time, 20% to 80% (CASCADE)		—	180	250	ps	T_A = –40°C
		—	210	300		T_A = +25°C
		—	230	325		T_A = +85°C

Note 1: AC characteristics are guaranteed by design and characterization.

2: Measured using 750 mV source, 50% duty cycle clock source, R_L = 50Ω to V_{CC} – 2V.

3: Refer to Typical Operating Characteristics section for output swing performance.

4: The delays of the individual bits are cumulative.

5: Duty cycle skew guaranteed only for differential operation measured from the crosspoint of the input edge to the crosspoint of the corresponding output edge.

6: Setup time defines the amount of time prior to an edge on IN, /IN that the D[0:9] bits must be set to guarantee the new delay will occur for that edge.

7: Setup time is the minimum that /EN must be asserted prior to the next transition of IN, /IN to prevent an output response greater than ±75 mV to that IN, /IN transition.

8: Hold time is the minimum time that /EN must remain asserted after a negative-going IN or a positive-going /IN to prevent an output response greater than ±75 mV to that IN, /IN transition.

9: Release time is the minimum time that /EN must be deasserted prior to the next IN, /IN transition to ensure an output response that meets the specified IN-to-Q propagation delay and transition times.

10: This is the amount of generated jitter added to an otherwise jitter-free clock signal, going from IN, /IN-to-Q, /Q.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20s
Package Thermal Resistances						
32-lead TQFP (Still-Air)	θ_{JA}	—	50	—	°C/W	—
32-lead TQFP (500 lfpm)	θ_{JA}	—	42	—	°C/W	—
32-lead TQFP	θ_{JC}	—	20	—	°C/W	—

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

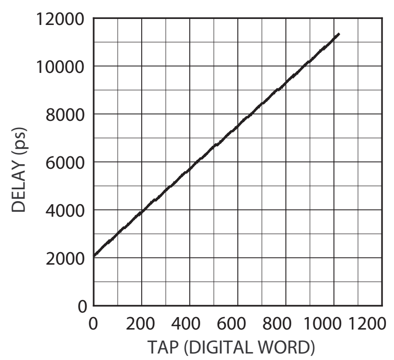


FIGURE 2-1: *Delay vs. Tap.*

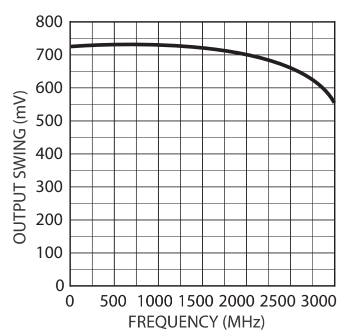


FIGURE 2-2: *Q, /Q Output Swing vs. Frequency.*

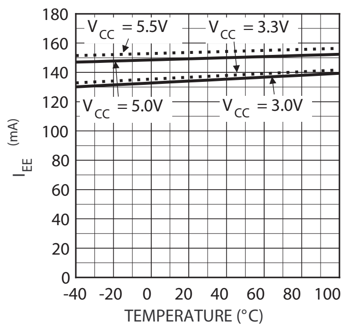


FIGURE 2-3: *Supply Current vs. Temperature.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
23, 25, 26, 27, 29, 30, 31, 32, 1, 2	D[0:9]	CMOS, ECL, or TTL Select Inputs: These digital control signals adjust the amount of delay from IN-to-Q. Please refer to the AC Electrical Characteristics and Table 5-1 for delay values. Figure 8-4 through Figure 8-8 show how to interface these inputs to various logic family standards. These inputs default to logic low when left unconnected. Bit 0 is the least significant bit, and bit 9 is the most significant bit
3	D[10]	CMOS, ECL, or TTL Select Input: This input latches just like D[0:9] does. It drives the CASCADE, /CASCADE differential pair. Use only when cascading two or more SY100EP195V to extend the range of delays required.
4, 5	IN, /IN	ECL Input: This is the signal to be delayed. If this input pair is left unconnected, this is equivalent to a logic low input.
6	VBB	Voltage Output: When using a single-ended logic source for IN and /IN, connect the unused input of the differential pair to this pin. This pin can also re-bias AC-coupled inputs to IN and /IN. When used, de-couple this pin to V_{CC} through an 0.01 µF capacitor. Limit current sinking or sourcing to 0.5 mA or less.
7	VEF	Voltage Output: Connect this pin to VCF when the D inputs are ECL. Refer to the Digital Control Logic Standard section of the Functional Description to interface the D inputs to CMOS or TTL.
8	VCF	Voltage Input: The voltage at this pin sets the logic transition threshold for the D inputs.
9, 24, 28	VEE	Most Negative Supply: Supply ground for PECL systems.
10	LEN	ECL Control Input: When logic low, the D inputs flow through. Any changes to the D inputs reflect in the delay between IN, /IN and Q, /Q. When logic high, the logic values at D are latched, and these latched bits determine the delay.
11	SETMIN	ECL Control Input: When logic high, the contents of the D register are reset. This sets the delay to the minimum possible, equivalent to D[0:9] being set to 0000000000. When logic low, the value of the D register, or the logic value of SETMAX determines the delay from IN, /IN to Q, /Q. This input defaults to logic low when left unconnected.
12	SETMAX	ECL Control Input: When logic high and SETMIN is logic low, the contents of the D register are set high, and the delay is set to one step greater than the maximum possible with D[0:9] set to 1111111111. When logic low, the value of the D register, or the logic value of SETMIN determines the delay from IN, /IN to Q, /Q. This input defaults to logic low when left unconnected.
13, 18, 19, 22	VCC	Most Positive Supply: Supply ground for NECL systems. Bypass to V_{EE} with 0.1 µF and 0.01 µF low-ESR capacitors.
15, 14	CASCADE, /CASCADE	100K ECL Outputs: These outputs are used when cascading two or more SY100EP195V to extend the delay range required.
16	/EN	ECL Control Input: When set active low, Q, /Q are a delayed version of IN, /IN. When set inactive high, IN, /IN are gated such that Q, /Q become a differential logic low. This input defaults to logic low when left unconnected.
21, 20	Q, /Q	100K ECL Outputs: This signal pair is the delayed version of IN, /IN.
17	NC	No Connect: Leave this pin unconnected.

4.0 FUNCTIONAL DESCRIPTION

SY100EP195V is a programmable delay line, varying the delay of a PECL or NECL input signal by any amount between about 2.1 ns and 10.8 ns. A 10-bit digital control register affords delay steps of approximately 10 ps.

SY100EP195V implements the delay using a multiplexer chain and a set of fixed delay elements. Under digital control, various subsets of the delay elements are included in the signal chain. To simplify interfacing, the 10-bit digital delay control word interfaces to PECL, CMOS, or TTL interface standards.

Because multiplexers must appear in the delay path, SY100EP195V has a minimum delay of about 2.1 ns. Delays below this value are not possible. In addition, when cascading multiple SY100EP195V to extend the delay range, the minimum delay is about 2.1 ns multiplied by the number of SY100EP195V in cascade. An eleventh control bit, D[10], along with the CASCADE and /CASCADE outputs and the SETMIN and SETMAX inputs, simplifies the task of cascading.

4.1 Signal Path Logic Standard

The signal path, from IN, /IN to Q, /Q, interfaces to PECL, LVPECL, or NECL signals, as shown in Table 4-6. The choice of signal path logic standard may limit possible choices for the delay control inputs, D.

4.2 Input Enable

The /EN input gates the signal at IN, /IN. When disabled, the input is effectively gated out, just as if a logic low was being provided to SY100EP195V.

TABLE 4-1: /EN TRUTH TABLE

/EN	Value at Q, /Q
L	IN, /IN Delayed
H	Logic Low Delayed

4.3 Digital Control Latch

SY100EP195V can capture the digital delay control word into its internal 11-bit latch, 10 bits for D[0:9], and an extra bit for the D[10] cascade control. The LEN input controls the action of this latch, as per Table 4-2.

Note that the LEN input is always PECL, LVPECL, or NECL, the same as the IN, /IN signal pair. The 11-bit delay control word, however, may also be CMOS or TTL.

TABLE 4-2: LEN TRUTH TABLE

LEN	Latch Action
L	Pass Through D[0:10]
H	Latch D[0:10]

The nominal delay value is based on the binary value in D[0:9], where D[0] is the least significant bit, and D[9] is the most significant bit.

4.4 Digital Control Logic Standard

When used in systems where VEE connects to ground, SY100EP195V may interface either to PECL, CMOS, or TTL on its D[0:10] inputs. To this end, the VCF pin sets the threshold at which the D inputs switch between logic low and logic high.

As shown in Table 4-3, connecting VCF to VEF sets the threshold to PECL (if V_{CC} is 5V) or LVPECL (if V_{CC} is 3.3V). Leaving VCF and VEF open yields a threshold suitable for detecting CMOS output logic levels. Leaving VEF open and connecting VCF to a 1.5V source allows the D inputs to accept TTL signals.

TABLE 4-3: DIGITAL CONTROL STANDARD TRUTH TABLE

Logic Standard	VCF Connection
ECL, PECL	VEF
CMOS	No Connect
TTL	1.5V Source

If a 1.5V source is not available, connecting VCF to VEE through an appropriate resistor will bias VCF at about 1.5V. The value of this resistor depends on the V_{CC} supply, as indicated in Table 4-4.

TABLE 4-4: RESISTOR VALUES FOR TTL INPUT

V_{CC}	Resistor Value
3.3V	1.5 kΩ
5.0V	500Ω

4.5 Cascade Logic

SY100EP195V is designed to ease cascading multiple devices in order to achieve a greater delay range. The SETMIN and SETMAX pins accomplish this, as set out in the applications section below. SETMIN and SETMAX override the delay by changing the value in the D latch register. Table 4-5 lists the action of these pins.

TABLE 4-5: SETMIN & SETMAX ACTION

SETMIN	SETMAX	Nominal Delay (ps)
L	L	As per D Latch
L	H	2100 + 8686
H	L	2100
H	H	Not Allowed

TABLE 4-6: SIGNAL PATH LOGIC STANDARD

Logic	V_{CC}	V_{EE}	Delay Control Input Choices
PECL	+4.5V to +5.5V	0V	PECL, CMOS, TTL
LVPECL	+3.0V to +3.6V	0V	LVPECL, CMOS, TTL
NECL	0V	–3.0V to –5.5V	NECL

5.0 APPLICATION INFORMATION

For best performance, use good high frequency layout techniques, filter V_{CC} supplies, and keep ground connections short. Use multiple vias where possible. Also, use controlled impedance transmission lines to interface with the SY100EP195V data inputs and outputs.

5.1 V_{BB} Supply

The VBB pin is an internally generated supply, and is available for use only by the SY100EP195V. When unused, this pin should be left unconnected. The two common uses for VBB are to handle a single-ended PECL input, and to re-bias inputs for AC-coupling applications.

If IN, /IN is driven by a single-ended output, VBB is used to bias the unused input. Please refer to Figure 8-1. The PECL signal driving SY100EP195V may optionally be inverted in this case.

When the signal is AC-coupled, VBB is used, as shown in Figure 8-3, to re-bias IN, /IN. This ensures that SY100EP195V inputs are within its acceptable common mode range.

In all cases, VBB current sinking our sourcing must be limited to 0.5 mA or less.

5.2 Setting D Input Logic Thresholds

In all designs where the SY100EP195V V_{EE} supply is at zero volts, the D inputs may accommodate CMOS and TTL level signals, as well as PECL or LVPECL. Figure 8-4 through Figure 8-8 show how to connect VCF and VEF for all possible cases.

5.3 Cascading

Two or more SY100EP195V may be cascaded, in order to extend the range of delays permitted. Each additional SY100EP195V adds about 2100 ps to the minimum delay, and adds another 8686 ps to the delay range.

Internal cascade circuitry has been included in the SY100EP195V. Using this internal circuitry, SY100EP195V may be cascaded without any external gating.

Examples of cascading 2, 3, or 4 SY100EP195V appear in Figure 5-1, Figure 5-2, and Figure 5-3. Table 5-1 lists the nominal delay for all the cases that appear in those figures.

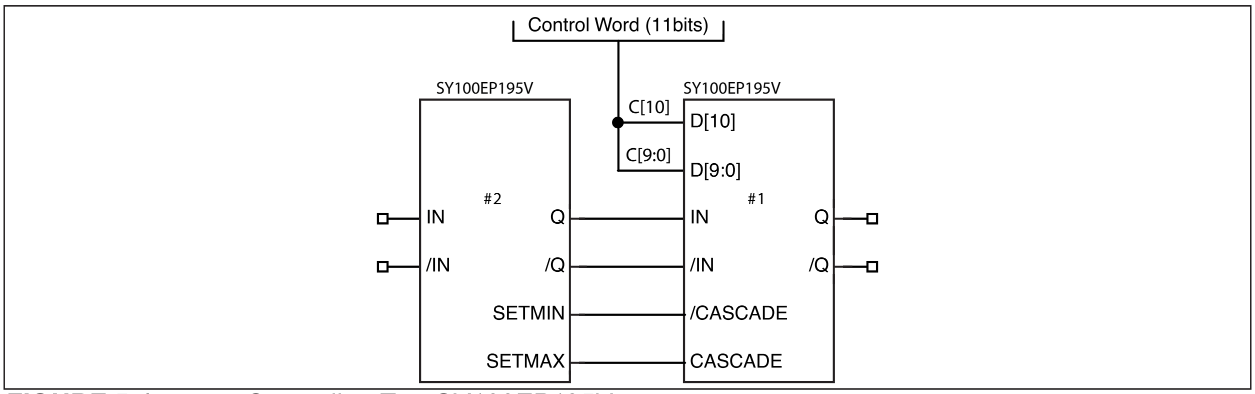


FIGURE 5-1: *Cascading Two SY100EP195V.*

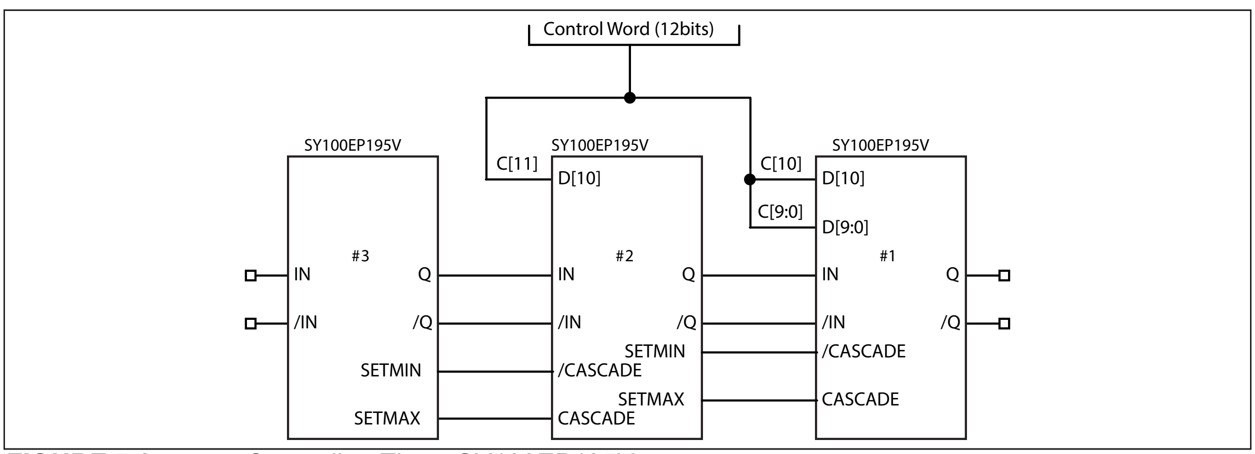


FIGURE 5-2: *Cascading Three SY100EP195V.*

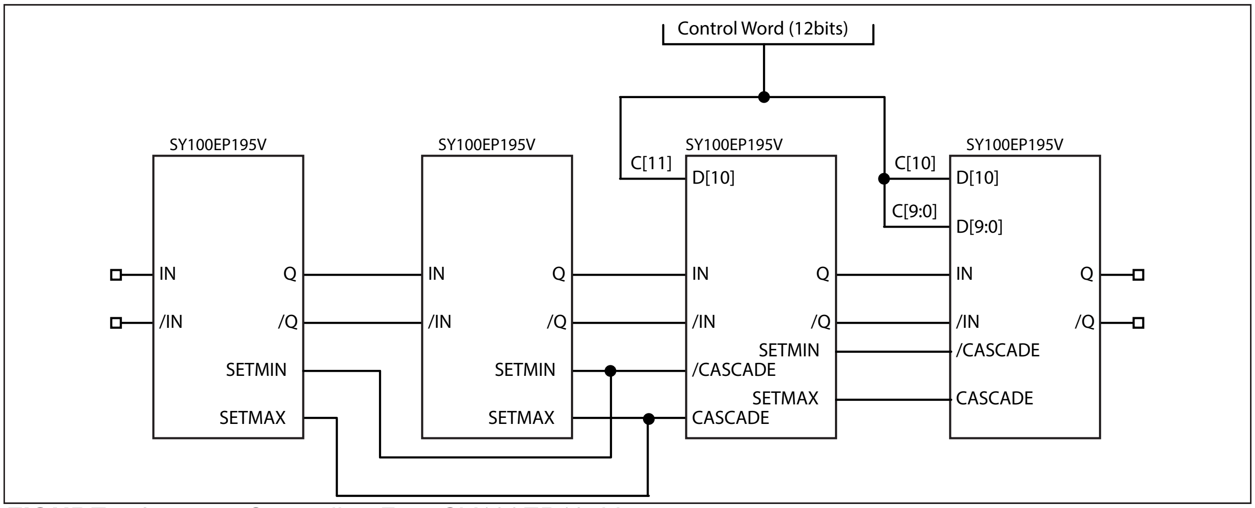


FIGURE 5-3: *Cascading Four SY100EP195V.*

TABLE 5-1: NOMINAL DELAY VALUES FOR CASCADED SY100EP195V

Control Inputs			Nominal Delay (ps)			
D[11]	**D[10]**	**D[9:0]**	**One Chip**	**Two Chips**	**Three Chips**	**Four Chips**
0	0	0000000000	2070	4140	6210	8280
0	0	0000000001	2080	4150	6220	8290
0	0	0000000010	2096	4166	6236	8306
0	0	0000000100	2112	4182	6252	8322
0	0	0000001000	2150	4220	6290	8360
0	0	0000010000	2213	4283	6353	8423
0	0	0000100000	2370	4440	6510	8580
0	0	0001000000	2610	4680	6750	8820
0	0	0010000000	3165	5235	7305	9375
0	0	0100000000	4220	6290	8360	10430
0	0	1000000000	6370	8440	10510	12580
0	0	1111111111	10756	12826	14896	16966
0	1	0000000000	—	12836	14906	16976
0	1	0000000001	—	12846	14916	16986
0	1	0000000010	—	12862	14932	17002
0	1	0000000100	—	12878	14948	17018
0	1	0000001000	—	12916	14986	17056
0	1	0000010000	—	12979	15049	17119
0	1	0000100000	—	13136	15206	17276
0	1	0001000000	—	13376	15446	17516
0	1	0010000000	—	13931	16001	18071
0	1	0100000000	—	14986	17056	19126
0	1	1000000000	—	17136	19206	21276
0	1	1111111111	—	21522	23592	25662
1	0	0000000000	—	—	14906	25672
1	0	0000000001	—	—	14916	25682
1	0	0000000010	—	—	14932	25698
1	0	0000000100	—	—	14948	25714

TABLE 5-1: NOMINAL DELAY VALUES FOR CASCADED SY100EP195V (CONTINUED)

Control Inputs			Nominal Delay (ps)			
D[11]	**D[10]**	**D[9:0]**	**One Chip**	**Two Chips**	**Three Chips**	**Four Chips**
1	0	0000001000	—	—	14986	25752
1	0	0000010000	—	—	15049	25815
1	0	0000100000	—	—	15206	25972
1	0	0001000000	—	—	15446	26212
1	0	0010000000	—	—	16001	26767
1	0	0100000000	—	—	17056	27822
1	0	1000000000	—	—	19206	29972
1	0	1111111111	—	—	23592	34358
1	1	0000000000	—	—	23602	34368
1	1	0000000001	—	—	23612	34378
1	1	0000000010	—	—	23628	34394
1	1	0000000100	—	—	23644	34410
1	1	0000001000	—	—	23682	34448
1	1	0000010000	—	—	23745	34511
1	1	0000100000	—	—	23902	34668
1	1	0001000000	—	—	24142	34908
1	1	0010000000	—	—	24797	35563
1	1	0100000000	—	—	25752	36518
1	1	1000000000	—	—	27902	38668
1	1	1111111111	—	—	32288	43054

6.0 INPUT AND OUTPUT STRUCTURES

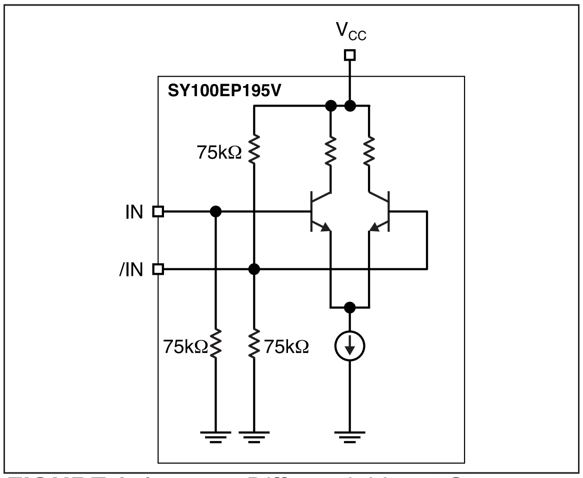


FIGURE 6-1: *Differential Input Structure.*

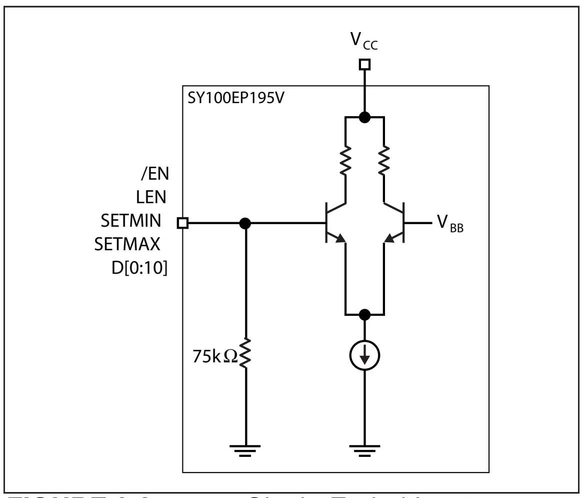


FIGURE 6-2: *Single-Ended Input Structure.*

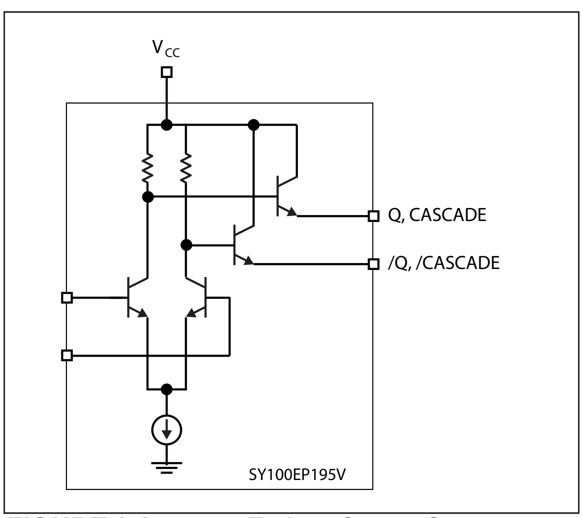


FIGURE 6-3: *Emitter Output Structure.*

7.0 INPUT AND OUTPUT LEVELS

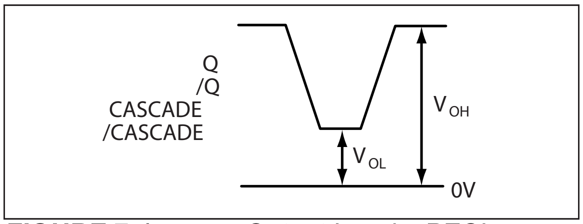


FIGURE 7-1: *Output Levels, PECL, LVPECL.*

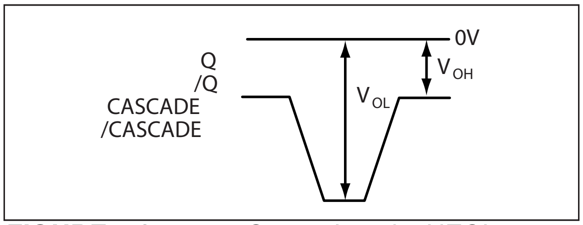


FIGURE 7-2: *Output Levels, NECL.*

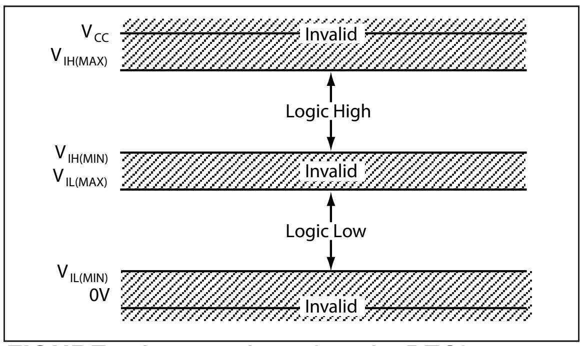


FIGURE 7-3: *Input Levels, PECL.*

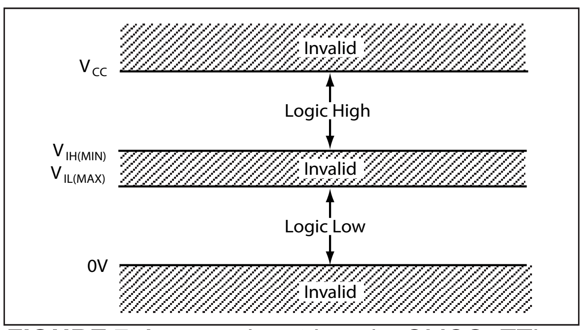


FIGURE 7-4: *Input Levels, CMOS, TTL.*

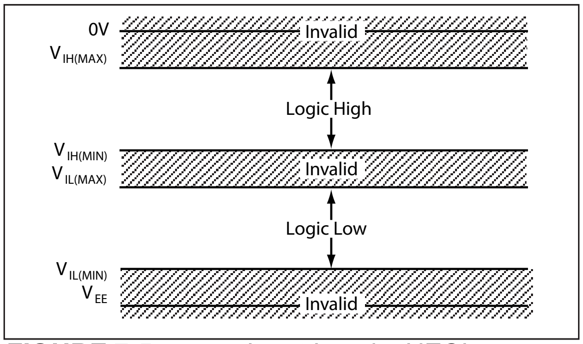


FIGURE 7-5: *Input Levels, NECL.*

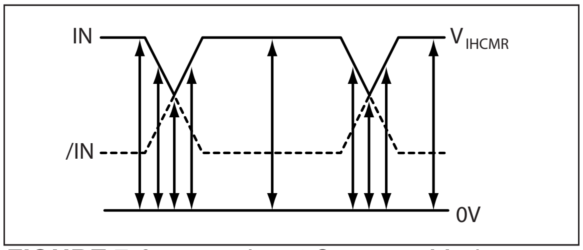


FIGURE 7-6: *Input Common Mode, PECL, LVPECL.*

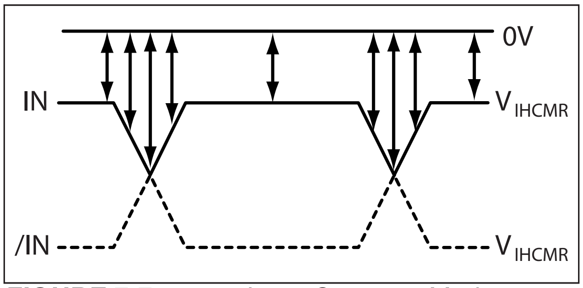


FIGURE 7-7: *Input Common Mode, NECL.*

8.0 INPUT INTERFACE APPLICATIONS

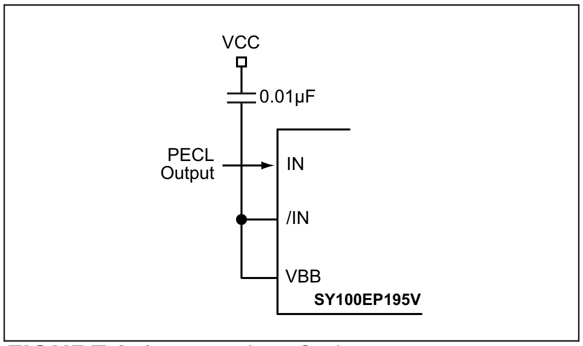


FIGURE 8-1: Interfacing to a Single-Ended PECL Signal.

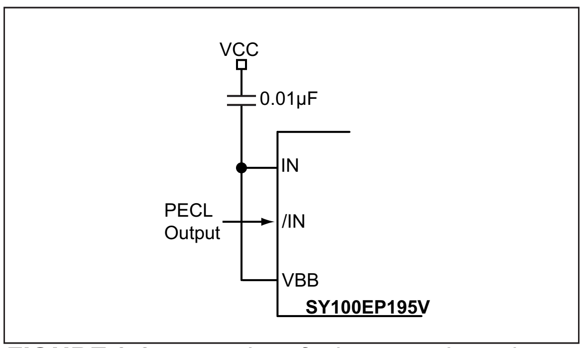


FIGURE 8-2: Interfacing to an Inverting Single-Ended PECL Signal.

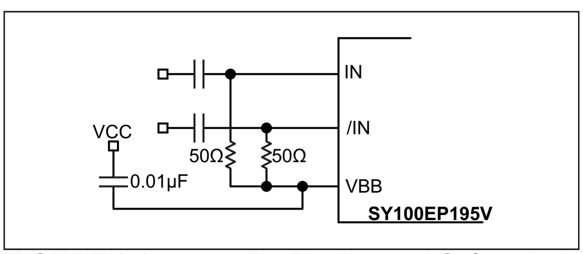


FIGURE 8-3: Re-Biasing an AC-Coupled Signal.

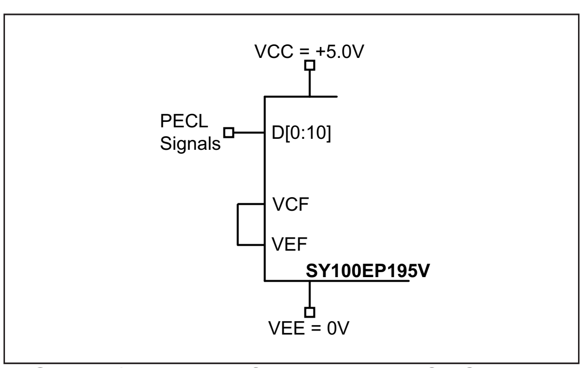


FIGURE 8-4: Connecting PECL Signals to the D Inputs.

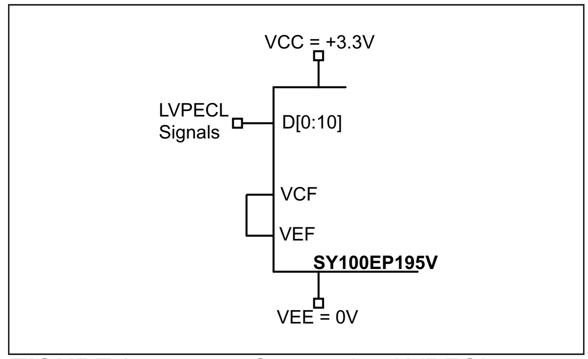


FIGURE 8-5: Connecting LVPECL Signals to the D Inputs.

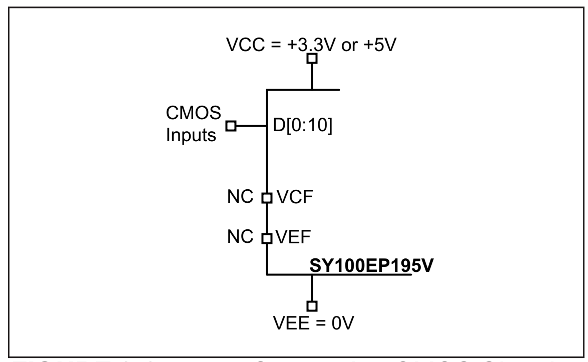


FIGURE 8-6: Connecting CMOS Signals to the D Inputs.

Note: V_{CF} and V_{EF} are not connected.

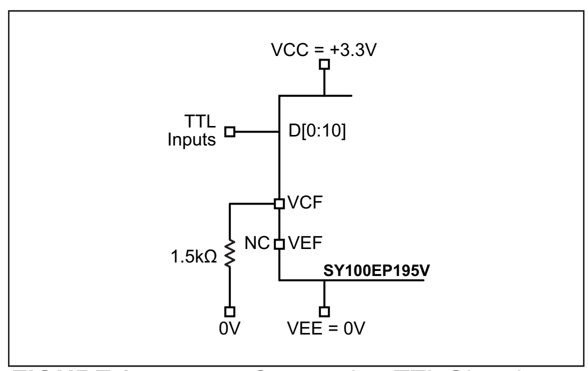


FIGURE 8-7: Connecting TTL Signals to the D Inputs with V_{CC} = 3.3V.

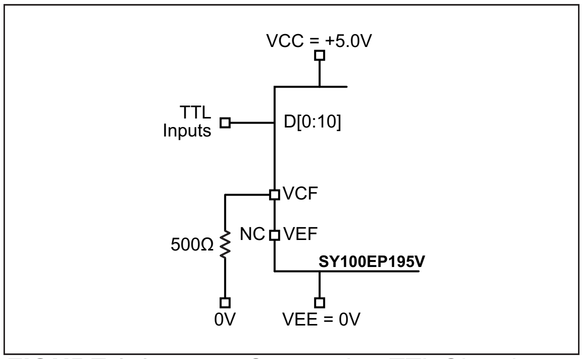


FIGURE 8-8: *Connecting TTL Signals to the D Inputs with V_{CC} = 5.0V.*

9.0 OUTPUT PECL TERMINATION

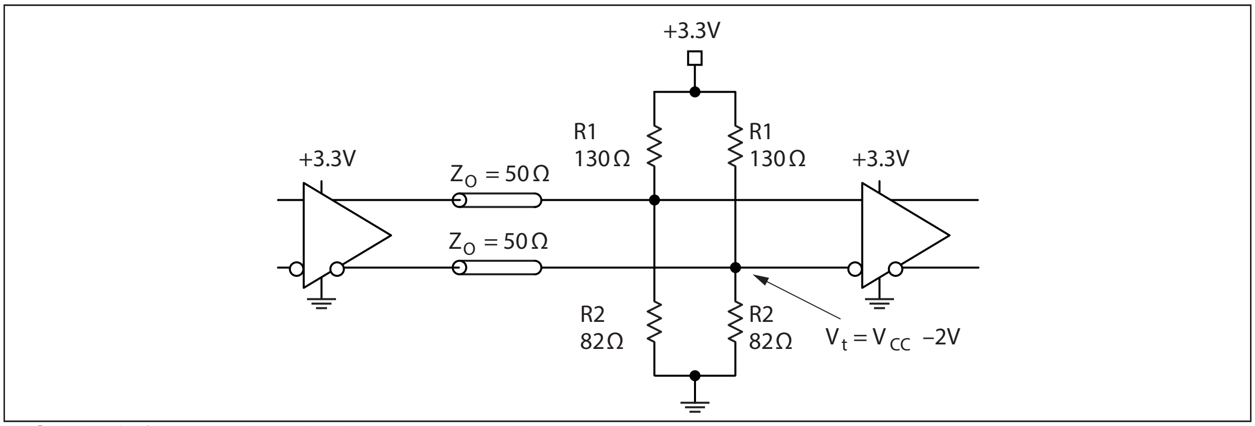


FIGURE 9-1: Parallel Termination – Thevenin Equivalent.

Note: For +5.0V systems: R1 = 82Ω, R2 = 130Ω.

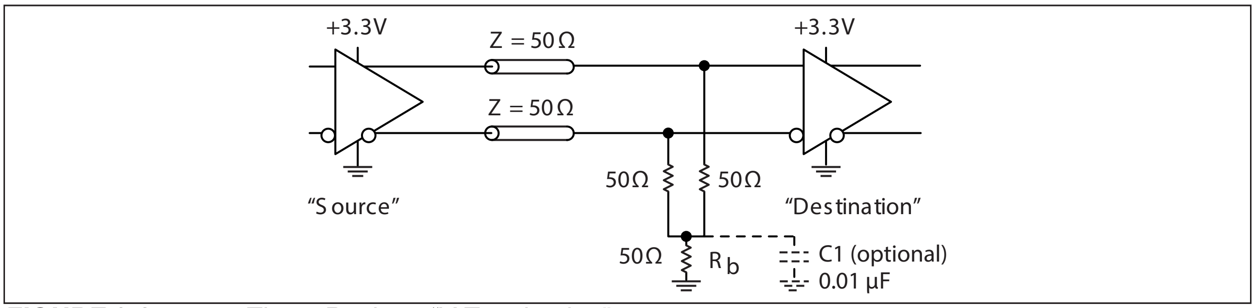


FIGURE 9-2: Three-Resistor "Y-Termination".

Note: Power-saving alternative to Thevenin termination.

Note: Place termination resistors as close to destination inputs as possible.

Note: R_b resistor set the DC bias voltage, equal to V_T. For +3.3V systems, R_b = 46Ω to 50Ω. For +5V systems, R_b = 110Ω.

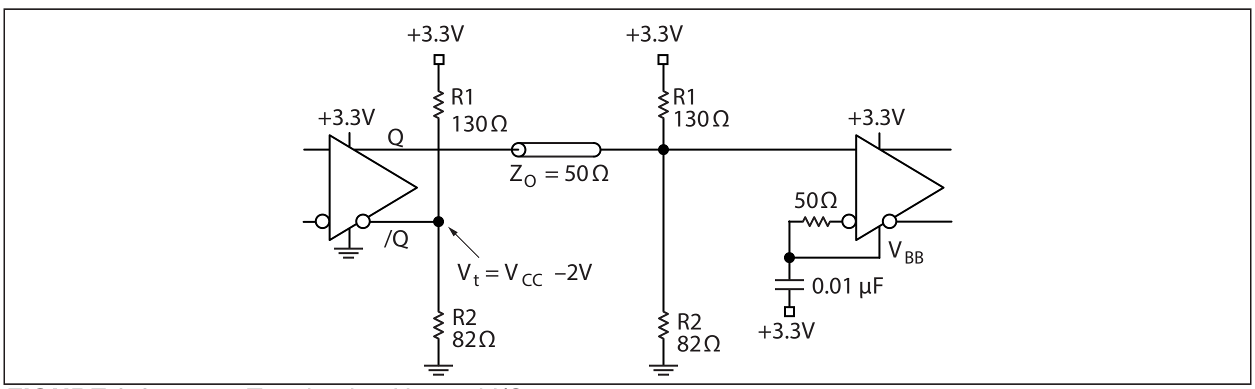


FIGURE 9-3: Terminating Unused I/O.

Note: Unused output (/Q) must be terminated to balance the output.

Note: Microchip's differential I/O logic devices include a V_{BB} reference pin.

Note: Connect unused input through 50Ω to V_{BB}. Bypass with a 0.01 µF capacitor to V_{CC}, not GND, because PECL is referenced to V_{CC}.

10.0 PACKAGING INFORMATION

10.1 Package Marking Information

32-Lead TQFP*

```
● XXXXXX-
XXXXXXXXXXX
WWNNN
```

Example

```
● MICREL-
100EP195VTG
36971
```

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

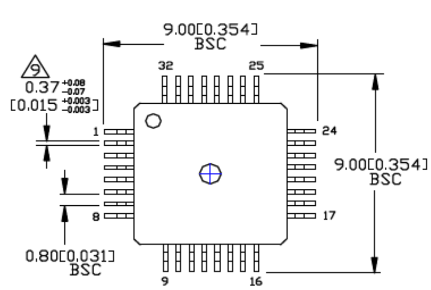
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

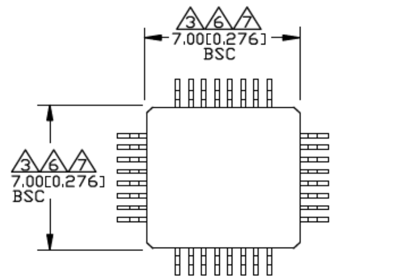
32-Lead TQFP Package Outline and Recommended Land Pattern

TITLE
32 LEAD TQFP 7X7 mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

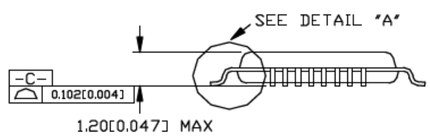
DRAWING #	TQFP7X7-32LD-PL-1	**UNIT**	MM [INCH]



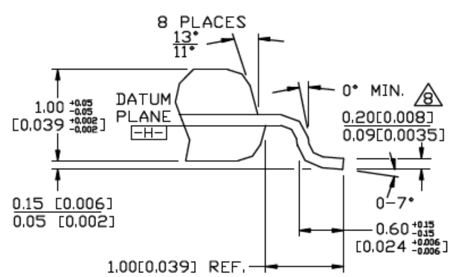
TOP VIEW



BOTTOM VIEW

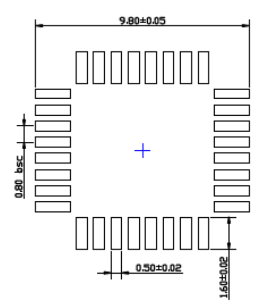


SIDE VIEW



DETAIL "A"

NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
8. DIMENSION INCLUDES LEAD FINISH.



RECOMMENDED LAND PATTERN

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2019)

- Converted Micrel document SY100EP195V to Microchip data sheet DS20006194A.
- Minor text changes throughout.
- Recalculated value updates to AC Electrical Characteristics and Table 5-1.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	XX
Device	Voltage Option	Package	Temperature	Media Type

Device:	SY100EP195:	3.3V/5V 1.6 GHz Programmable Delay
Voltage Option:	V =	3.3V to 5.5V
Package:	T =	32-Lead 7 mm x 7 mm TQFP
Temperature:	G =	–40°C to +85°C
Special Processing:	Blank = TR =	250/Tray 1,000/Reel

Examples:

a) SY100EP195VTG: SY100EP195, 3.3V to 5V Voltage Option, 32-Lead TQFP, –40°C to +85°C Temp. Range, 250/Tray

b) SY100EP195VTG-TR: SY100EP195, 3.3V to 5V Voltage Option, 32-Lead TQFP, –40°C to +85°C Temp. Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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