Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	68	A
I_D	Drain current (continuous) at T_C = 100 °C	43	A
I_{DM} (1)	Drain current (pulsed)	272	A
P_{TOT}	Total dissipation at T_C = 25 °C	450	W
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	10	A
E_{AS}	Single pulse avalanche energy (starting T_j=25°C, I_D= 10 A; V_{DD}=50 V)	1500	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)Pulse width limited by safe operating area

(2)I_{SD} ≤ 68 A, di/dt = 400 A/µs, $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V

(3)V_{DS} ≤ 480 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.28	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	50	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 600 V			1	µA
		V_{GS} = 0, V_{DS} = 600 V, T_C=125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ±25 V			±10	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 34 A		0.030	0.040	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	5200	-	pF
C_{oss}	Output capacitance		-	250	-	pF
C_{rss}	Reverse transfer capacitance		-	5	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	395	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0 A	-	3.3	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 68 A, V_{GS} = 10 V (see *Figure 15: "Gate charge test circuit"*)	-	118	-	nC
Q_{gs}	Gate-source charge		-	25	-	nC
Q_{gd}	Gate-drain charge		-	47	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 34 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Switching times test circuit for resistive load"* and *Figure 19: "Switching time waveform"*)	-	30	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off-delay time		-	150	-	ns
t_f	Fall time		-	9	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		68	A
I_{SDM}(1)	Source-drain current (pulsed)		-		272	A
V_{SD}(2)	Forward on voltage	I_{SD} = 68 A, V_{GS} = 0	-	0.98	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 68 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 18: "Unclamped inductive waveform"*)	-	520		ns
Q_{rr}	Reverse recovery charge		-	12		µC
I_{RRM}	Reverse recovery current		-	45		A
t_{rr}	Reverse recovery time	I_{SD} = 68 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 18: "Unclamped inductive waveform"*)	-	680		ns
Q_{rr}	Reverse recovery charge		-	18		µC
I_{RRM}	Reverse recovery current		-	50		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curve)

Figure 2: Safe operating area

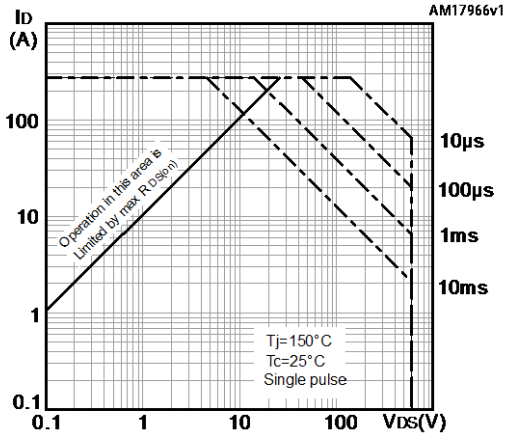


Figure 3: Thermal impedance

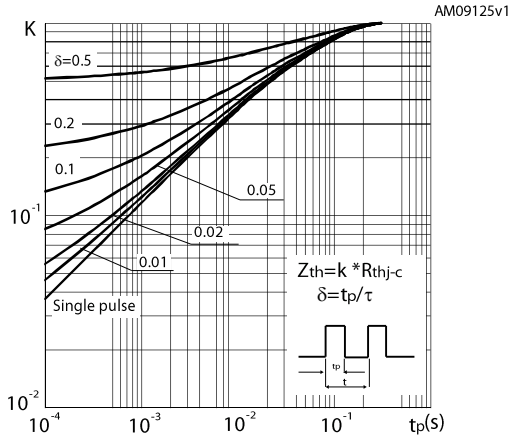


Figure 4: Output characteristics

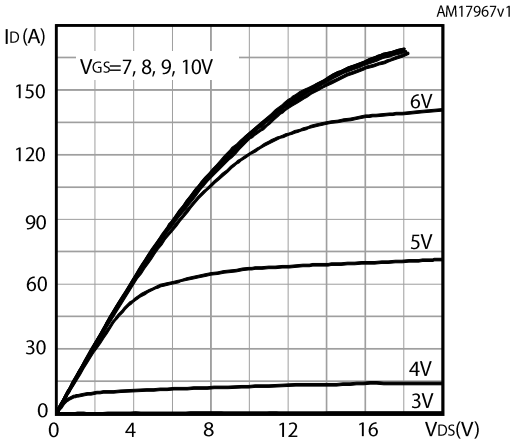


Figure 5: Tranfer characteristics

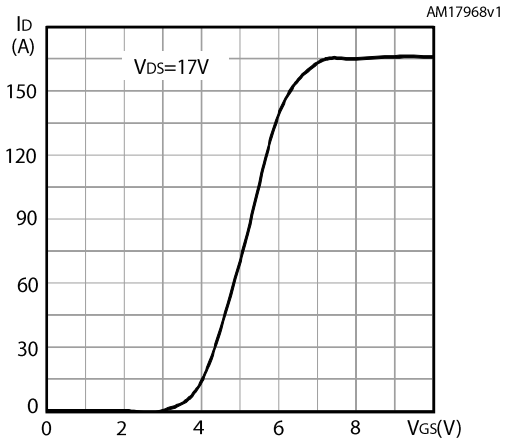


Figure 6: Gate charge vs gate-source voltage

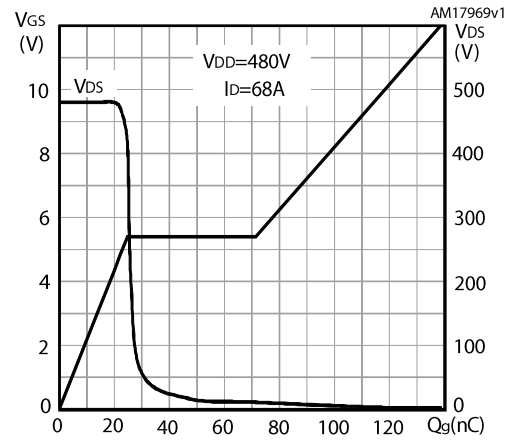


Figure 7: Static drain-source on-resistance

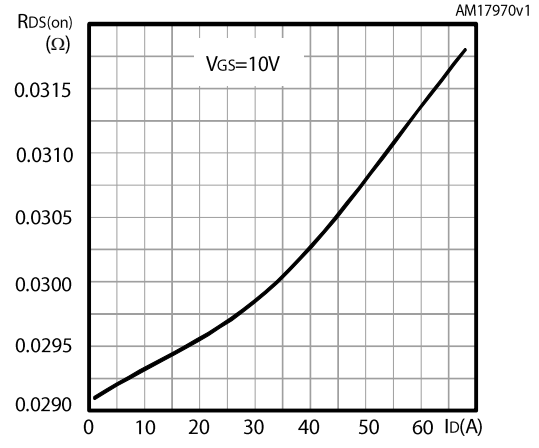


Figure 8: Capacitance variations

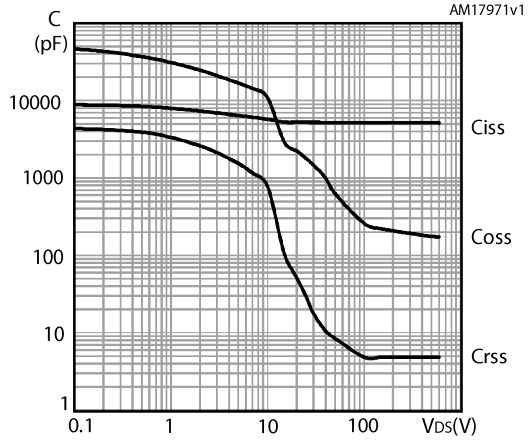


Figure 9: Output capacitance stored energy

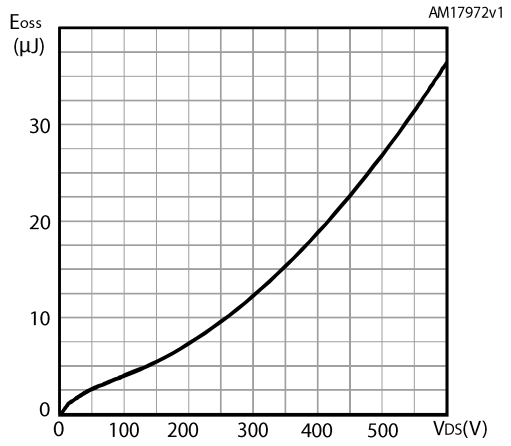


Figure 10: Normalized gate threshold voltage vs temperature

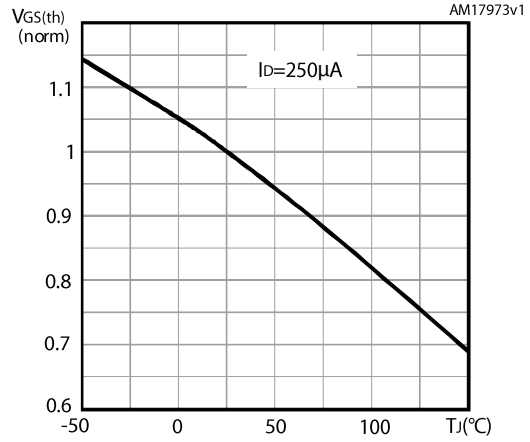


Figure 11: Normalized on-resistance vs temperature

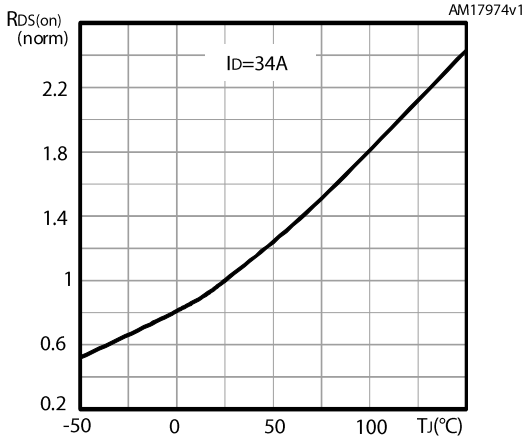


Figure 12: Normalized $V_{(BR)DSS}$ vs temperature

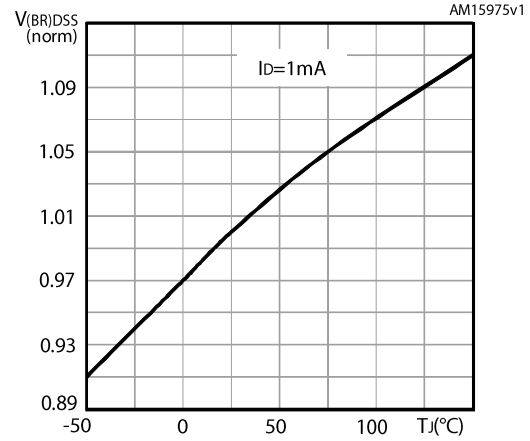
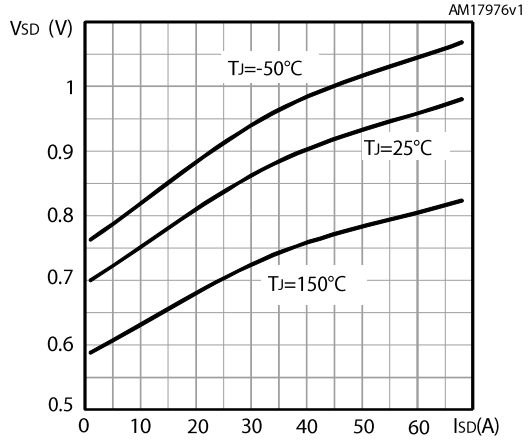


Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Switching times test circuit for resistive load

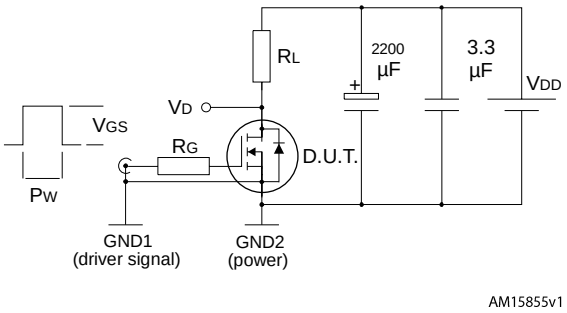


Figure 15: Gate charge test circuit

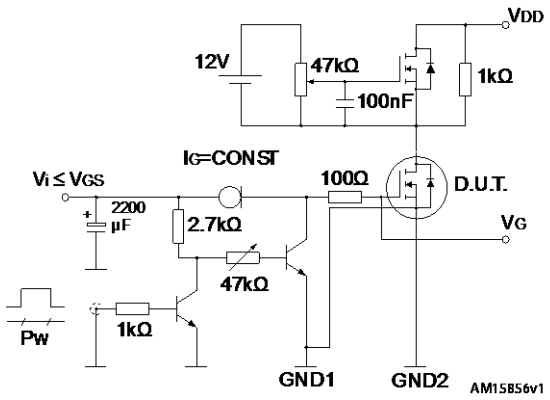


Figure 16: Test circuit for inductive load switching and diode recovery times

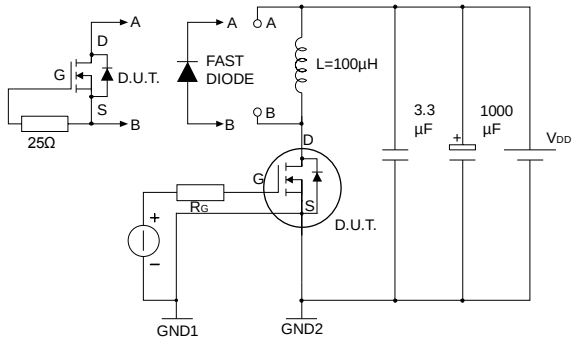


Figure 17: Unclamped inductive load test circuit

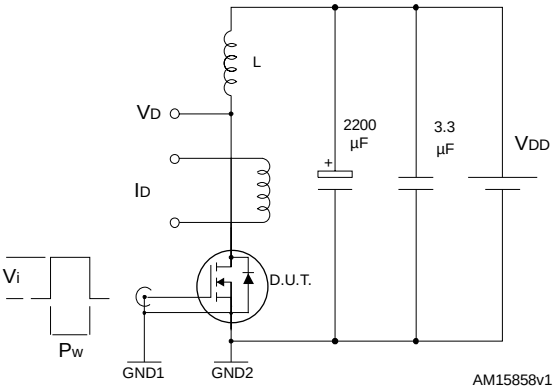


Figure 18: Unclamped inductive waveform

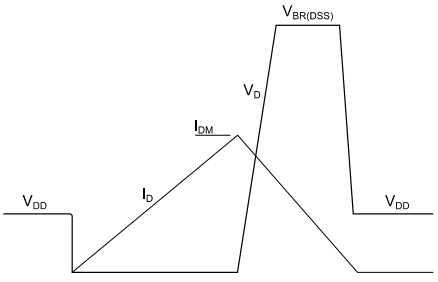
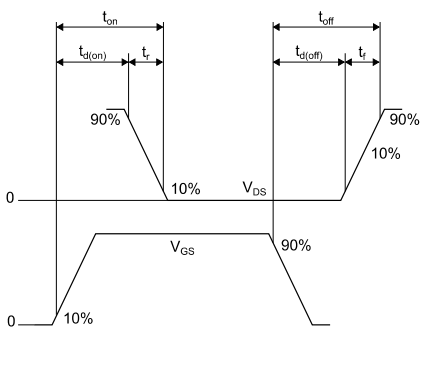


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO247-4 package information

Figure 20: TO247-4 package outline

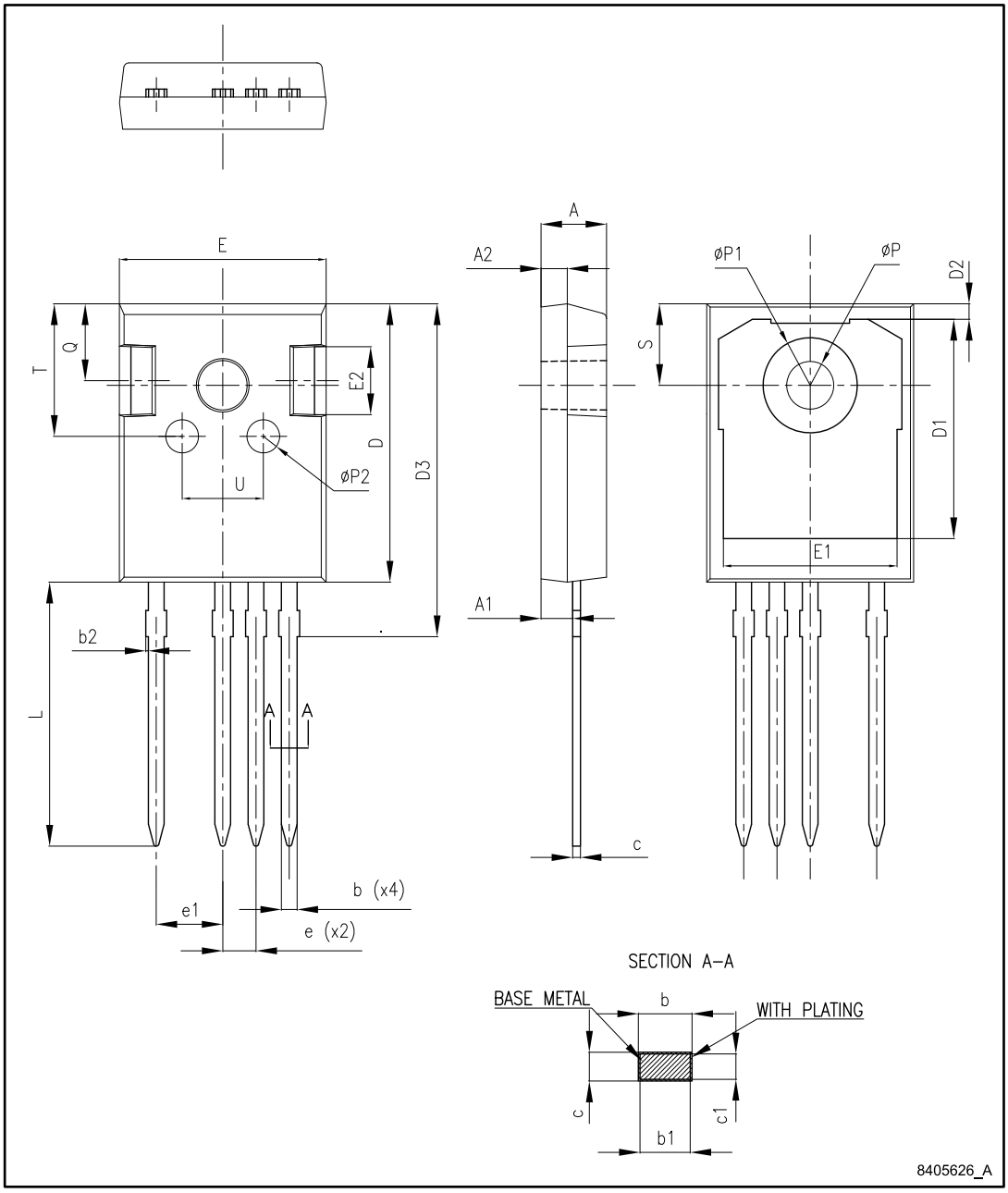


Table 8: TO247-4 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.29
b1	1.15	1.20	1.25
b2	0		0.20
c	0.59		0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1			7.40
P2	2.40	2.50	2.60
Q	5.60		6.00
S		6.15	
T	9.80		10.20
U	6.00		6.40

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
26-Sep-2016	1	Initial release.

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