Si4812BDY

Vishay Siliconix

Devenuetev	1	ICATIONS T _J = 25 °C, unless oth	-	1	Mari	Line / t	
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	1					1	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1		3	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zero Gate Voltage Drain Current (MOSFET and Schottky)		$V_{DS} = 30 V, V_{GS} = 0 V$		0.004	0.100	mA	
	I _{DSS}	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 100 ^{\circ}\text{C}$		0.7	10		
		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 125 \text{ °C}$		3.0	20		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
Drain-Source On-State Resistance ^a	Б	V _{GS} = 10 V, I _D = 9.5 A 0.013		0.016	0		
	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 7.7 \text{ A}$		0.0165	0.021	Ω	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 9.5 \text{ A}$		45		S	
Schottky Diode Forward Voltage ^a	V	I _S = 1.0 A, V _{GS} = 0 V		0.45	0.50	N	
	V _{SD}	I_{S} = 1.0 A, V_{GS} = 0 V, T_{J} = 125 °C		0.33	0.42	- V	
Dynamic ^b			-				
Total Gate Charge	Qg			8.5	13	nC	
Gate-Source Charge	Q _{gs}	V_{DS} = 15 V, V_{GS} = 5 V, I_{D} = 9.5 A		3			
Gate-Drain Charge	Q _{gd}			2.6			
Gate Resistance	Rg		0.3	0.7	1.1	Ω	
Turn-On Delay Time	t _{d(on)}			15	25		
Rise Time	t _r	V_{DD} = 15 V, R_L = 15 Ω		13	20	ns	
Turn-Off Delay Time	t _{d(off)}	$I_{D}\cong$ 1 A, V_{GEN} = 10 V, R_{g} = 6 Ω		20	30		
Fall Time	t _f			8	15		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.0 A, dl/dt = 100 A/μs		22	35		

Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

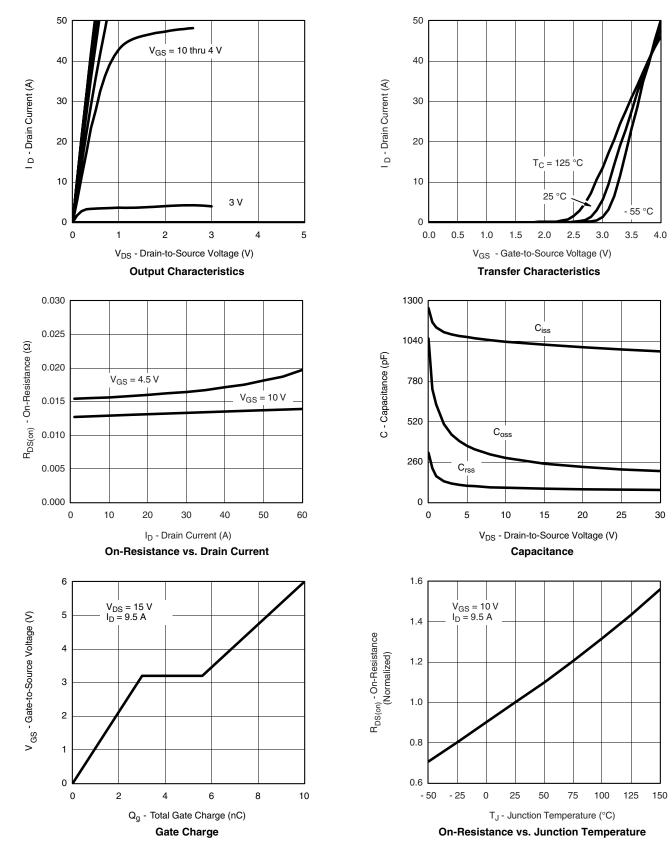




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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

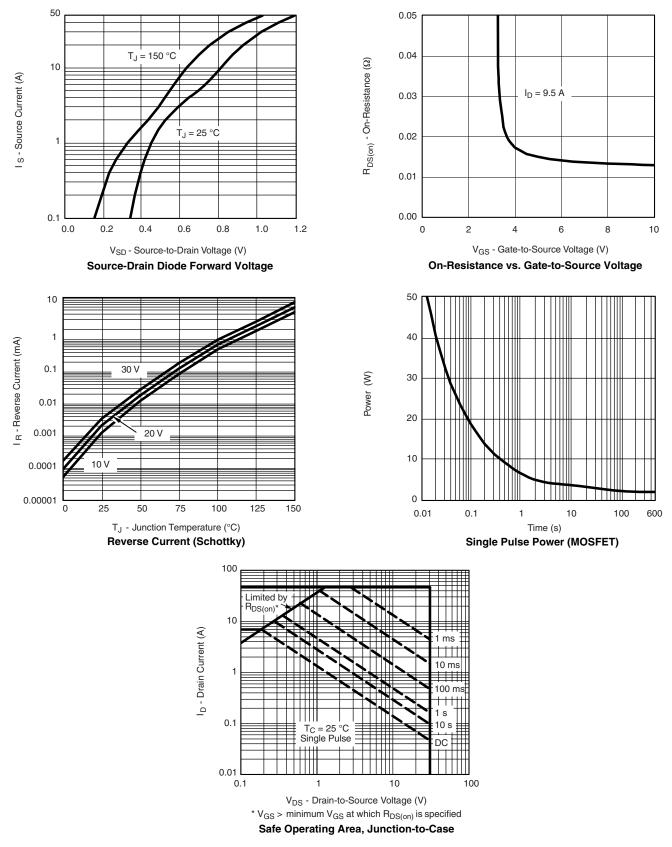


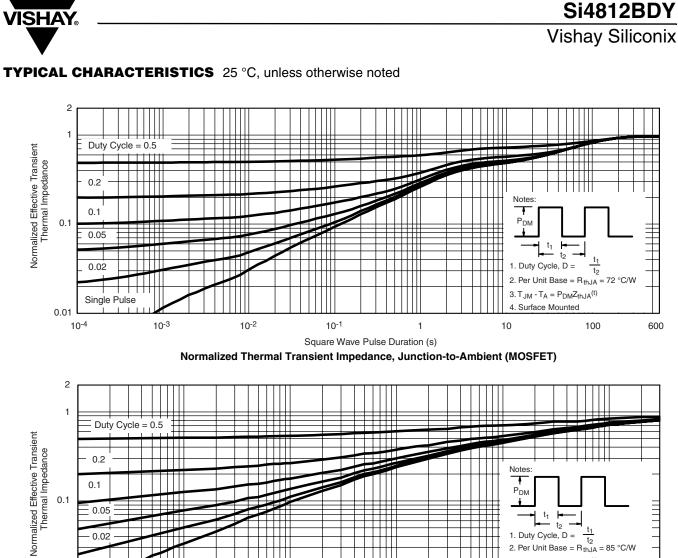
Document Number: 73038 S-83039-Rev. D, 29-Dec-08

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





t₁ t₂ t₁ 0.02 1. Duty Cycle, D = t2 2. Per Unit Base = R_{thJA} = 85 °C/W 3. T_{JM} - $T_A = P_{DM}Z_{thJA}^{(t)}$ Single Pulse 4. Surface Mounted 1 1 1 1 1 1 0.01 10⁻³ 10-4 10-2 10-1 1 10 Square Wave Pulse Duration (s)

Normalized Thermal Transient Impedance, Junction-to-Ambient (Schottky)

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73038.

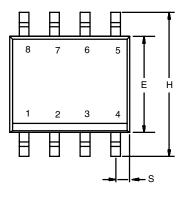
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Package Information

Vishay Siliconix

SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





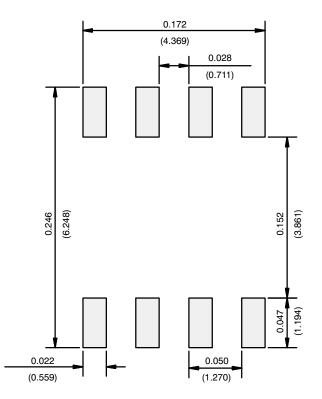
	MILLIM	IETERS	INCHES					
DIM	Min	Мах	Min	Max				
A	1.35	1.75	0.053	0.069				
A ₁	0.10	0.20	0.004	0.008				
В	0.35	0.51	0.014	0.020				
С	0.19	0.25	0.0075	0.010				
D	4.80	5.00	0.189	0.196				
E	3.80	4.00	0.150	0.157				
е	1.27 BSC		0.050 BSC					
н	5.80	6.20	0.228	0.244				
h	0.25	0.50	0.010	0.020				
L	0.50	0.93	0.020	0.037				
q	0°	8°	0°	8°				
S	0.44	0.64	0.018	0.026				
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498								

Application Note 826

Vishay Siliconix



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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