ABSOLUTE MAXIMUM RATINGS

Positive Supply (Pins 5, 17)	−0.5V dc to +18V dc
Negative Supply (Pins 6, 18)	+0.5V dc to −18V dc
Digital Input Voltages	
Address, Sample (Pins 8, 9, 20, 21)	−0.5V dc to +7V dc
Mux. Enable (Pins 7, 19)	−18V dc to +18V dc
Analog Input Voltage	±15V dc

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the full operating temperature range and power supply range unless otherwise specified. For test aspects, contact the factory.

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
ANALOG INPUTS				
Input Voltage Range	±10	–	–	V
Input Impedance	1M	–	–	Ohm
Input Capacitance	–	–	30	pf
Input Bias Current	–	–	1.5	μA
LOGIC INPUTS (TTL/CMOS)				
Logic 1 voltage	2.4	–	–	V
Logic 0 voltage	–	–	0.8	V
Logic 1 current	–	–	1	μA
Logic 0 current	–	–	1	μA
ANALOG OUTPUTS				
Direct Output (pins 1, 13)				
Output Voltage Range	±10	–	–	V
Output Current	10	–	–	mA
Output Impedance	–	1	2	Ohm
Mux. Output (pins 11, 23)				
Output Voltage Range	±10	–	–	V
Output Current	10	–	–	mA
Output Impedance	–	50	150	Ohms
OFF Output Leakage	–	–	1	μA
OFF Output Capacitance	–	–	20	pf
Output Switch Delay	–	–	500	nS
PERFORMANCE				
Gain (1)	–	+1	–	–
Gain Error (1)	–	–	±0.02	%
Gain Tempco	–	1	10	ppm/°C
Linearity Error (1)	–	–	0.003	% FSR
Linearity Tempco.	–	–	±1	ppm/°C
Initial Offset Voltage (2)	–	–	±1	mV
Offset Tempco., Hold Mode	–	20	50	μV/°C
Crosstalk, channel-to-channel	-90	–	–	dB
Offset Tempco. Tracking (A vs. B)	–	±10	±20	μV/°C
Gain Tracking (A vs. B)	–	–	±50	ppm
Gain Tracking Tempco.	–	–	±0.5	ppm/°C
PHYSICAL/ENVIRONMENTAL				
Thermal Resistance				
Junction-to-Case	–	0.015	–	°C/mW
Case-to-Ambient	–	0.035	–	°C/mW
Operating Temp. Range				
SHM-91MC	0 to +70 °C (ambient)			
SHM-91MM	-55 to +125 °C (ambient)			
Storage Temperature Range	-55 to +125 °C			
Package Type	24-pin hermetically sealed ceramic DIP			

T/H SWITCHING	MIN.	TYP.	MAX.	UNITS
Aperture Delay Time	–	15	–	nS
Aperture Uncertainty (Jitter)	–	300	1,000	pS
Offset Step (2)	–	–	±1	mV
Settling Time to ±2 mV	–	–	600	nS
HOLD MODE DYNAMICS				
Droop Rate: +25 °C	–	–	5	μV/μS
+85 °C	–	–	10	μV/μS
+125 °C	–	–	100	μV/μS
Feedthrough Rejection	-90	–	–	dB
HOLD-TO-TRACK DYNAMICS				
Acquisition Time				
10V Step to ±0.2 mV	–	–	2	μS
10V Step to ±1 mV	–	–	1.5	μS
POWER SUPPLY REQUIREMENTS				
Supply Voltage Range ±V	±14.5	±15	±15.5	V dc
Power Supply Rej. Ratio	-60	–	–	dB
Current Drains: ±15V dc	–	–	30	mA
-15V	–	–	30	mA
Power Dissipation	–	700	900	mW
TRACK MODE DYNAMICS				
Frequency Response				
Small Signal (−3dB)	–	–	1	Mhz
Slew Rate	–	45	–	V/μS

1. Specified at +25 °C.
2. Tested at ±25 °C with input source impedance of 50 ohms.

TECHNICAL NOTES

1. All ground pins (2, 12, 14, 24) should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder all four ground pins directly to it. The power supply pins (5, 6, 17, 18) should be bypassed to analog ground with .01 μF ceramic capacitors located as close to the pins as possible. In certain critical applications, additional bypass precautions using 0.1 or 1.0 μF tantalum capacitors are suggested.
2. A logic "1" on the sample pins (9, 21) will put this device in the sample mode. In this mode, the device acts as an unity gain amplifier and its output will track its input. A logic "0" on the sample pins (9, 21) will put the device in the hold mode, and the output will be held constant at the last input level present before the hold command was given.
3. Care should be taken when using the multiplexer output pins (11, 23) that the A $\overline{EN}$ (pin 7) and the B $\overline{EN}$ (pin 19) are not active (logic 0) at the same time. This condition could possibly damage the device.
4. The output of the SHM-91 should drive a high impedance receiver to minimize voltage divider losses. The receiver input impedance should be 100K ohms or greater when using the direct outputs from the amplifiers (pins 1 and 13). The receiver input impedance should be 2.5 M ohms or greater when using the multiplexer outputs (pins 11 and 23).
5. The SHM-91 should not be left in the hold mode for long periods of time. It should be left in the sample mode when long or indeterminate periods of time are involved. If left in the hold mode for several seconds, the output will continue to "droop" toward the power supply voltage. Eventually the output amplifier will saturate. The unit will require longer than the specified acquistion time to acquire a signal when the output amplifiers are saturated.
6. A Logic "1" on the A or B ADDR (Address) pins (8 and 20) will select channel 1A or 1B on the respective input mux. A Logic "0" will select 2A or 2B.