■ Block Diagrams

1. A/F type

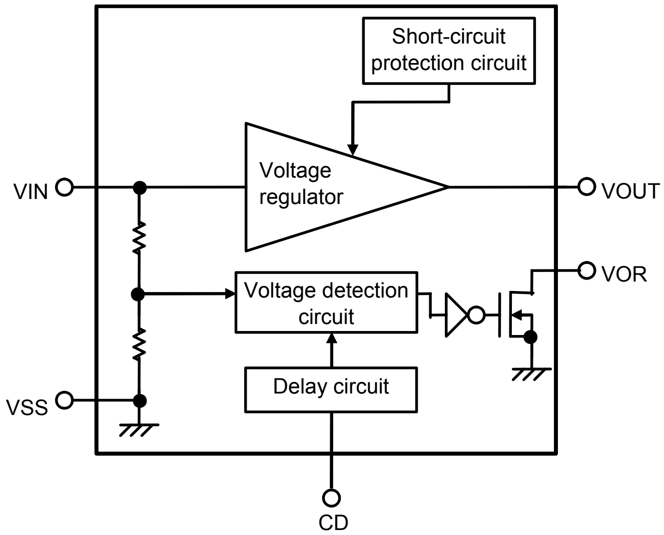


Figure 1

2. B type

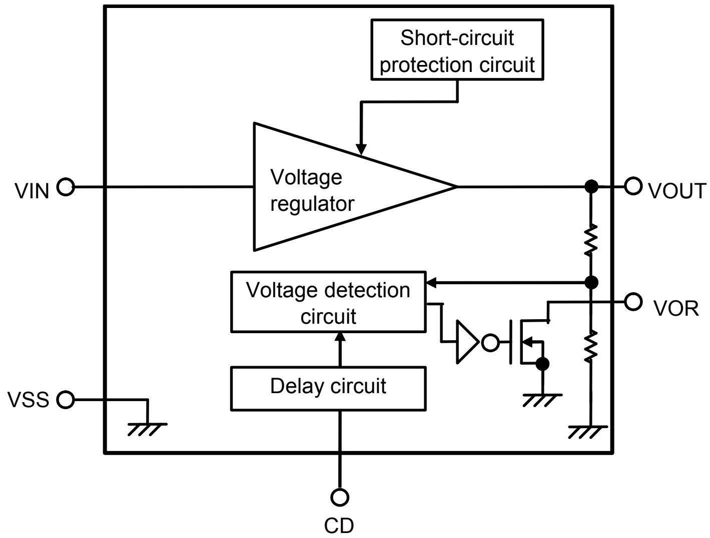


Figure 2

3. C type

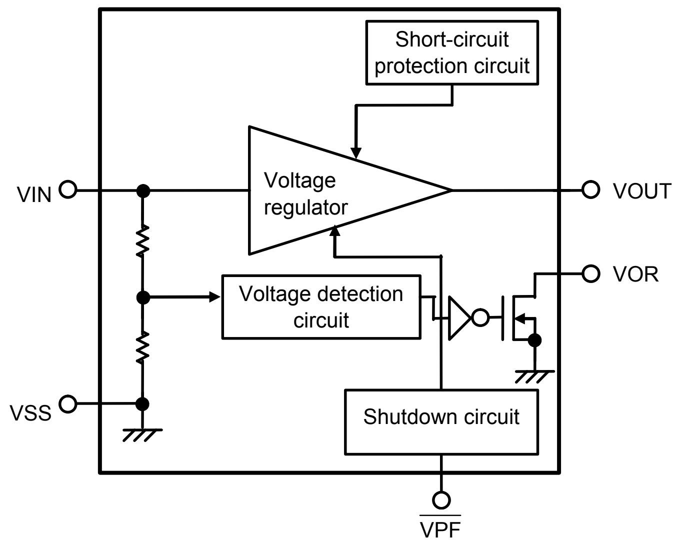


Figure 3

4. E type

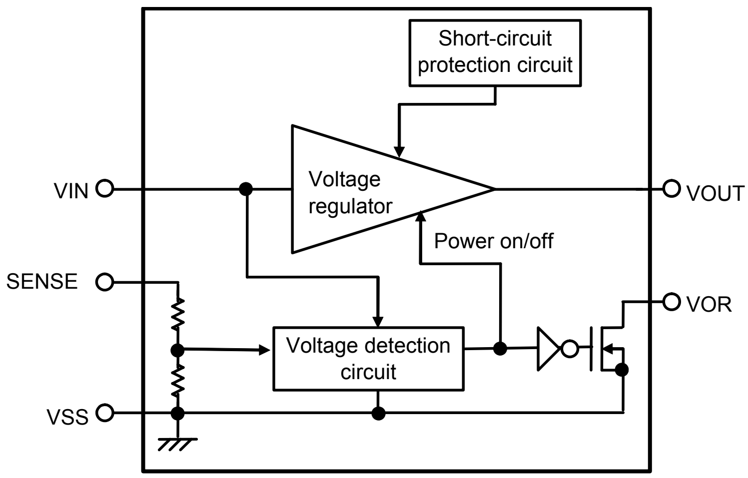


Figure 4

5. G type

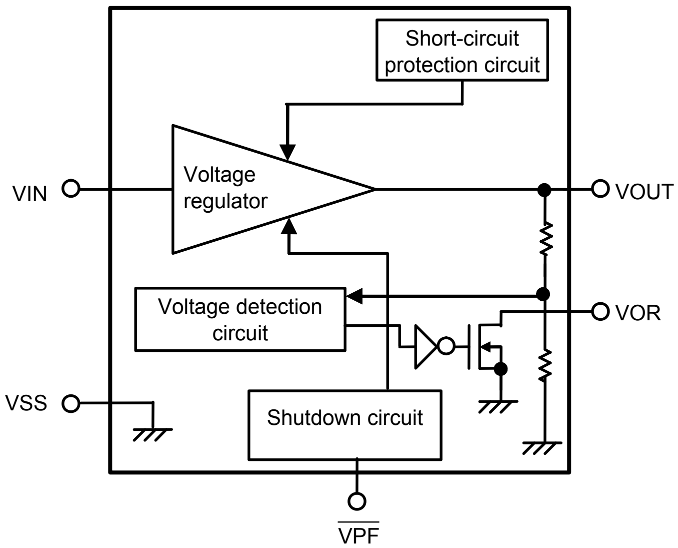


Figure 5

■ Product Name Structure

1. Function list

Table 1

Type name	Voltage detector (VD)	Detection voltage ($-V_{DET}$) accuracy [%]	Release voltage ($+V_{DET}$) accuracy [%]	Built-in delay circuit	Shutdown function	
					VR	VD
A type	Detects V_{IN}	±2.4	—	Yes	No	No
B type	Detects V_{OUT}	±2.4	—	Yes	No	No
C type	Detects V_{IN}	±2.4	—	No	Yes	No
E type	Detects V_{SENSE}	±2.4	—	No	Yes	No
F type	Detects V_{IN}	—	±1.1	Yes	No	No
G type	Detects V_{OUT}	±2.4	—	No	Yes	No

2. Product name selection guide

S-87 xx xx x UP - xxx T2 x

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
  - G: Lead-free (for details, please contact our sales office)
- IC direction in the tape sepecifications*1
- Product name (Abbreviation)*2
- Package name (Abbreviation)
  - UP: SOT-89-5
- Product type
  - A: Built-in delay circuit, V_{IN} detection ($-V_{DET}$ detection)
  - B: Built-in delay circuit, V_{OUT} detection
  - C: Built-in shudown circuit for regulator, V_{IN} detection
  - E: Built-in shudown circuit for regulator, V_{SENSE} detection
  - F: Built-in delay circuit, V_{IN} detection ($+V_{DET}$ detection)
  - G: Built-in shudown circuit for regulator, V_{OUT} detection
- Detection voltage of voltage detector
  - 21 to 94, A0, B0, B3 (Ex. When the detection voltage of voltage detector is 2.1 V, it is expressed as 21.*3)
- Output voltage of voltage regulator
  - 25 to 56 (Ex. When the output voltage of voltage regulator is

***1.** Refer to the tape specifications at the end of this document.
***2.** Refer to the **Table 2** to **Table 3** in the "**4. Product name list**".
***3.** A0 for 10.0 V, B0 for 11.0 V, B3 for 11.3 V.

3. Package

Package Name	Drawing Code		
	Package	Tape	Reel
SOT-89-5	UP005-A-P-SD	UP005-A-C-SD	UP005-A-R-SD

4. Product name list

Table 2 (1/2)

VR output voltage [V]	VD detection voltage [V]	S-87xxxxA Series	S-87xxxxB Series	S-87xxxxC Series
5.6	3.5	—	S-875635BUP-AGAT2x	—
5.2	9.4	—	—	S-875294CUP-AHCT2x
	7.1	—	—	S-875271CUP-AHAT2x
	5.5	—	—	S-875255CUP-AHBT2x
5.0	11.0	—	—	S-8750B0CUP-ACGT2x
	7.7	S-875077AUP-AAFT2x	—	S-875077CUP-ACFT2x
	6.1	—	—	S-875061CUP-ACHT2x
	4.5	S-875045AUP-AAAT2x	S-875045BUP-ABAT2x	S-875045CUP-ACAT2x
	4.3	S-875043AUP-AABT2x	S-875043BUP-ABBT2x	S-875043CUP-ACBT2x
	4.1	S-875041AUP-AACT2x	S-875041BUP-ABCT2x	S-875041CUP-ACCT2x
	3.9	S-875039AUP-AADT2x	S-875039BUP-ABDT2x	S-875039CUP-ACDT2x
	3.7	S-875037AUP-AAET2x	S-875037BUP-ABET2x	S-875037CUP-ACET2x
	3.4	—	S-875034BUP-ABFT2x	—
	2.9	—	S-875029BUP-ABHT2x	—
	2.1	—	S-875021BUP-ABGT2x	—
3.3	7.7	S-873377AUP-0AAT2x	—	—
	6.1	—	—	S-873361CUP-AOHT2x
	4.1	—	—	S-873341CUP-AOCT2x
	2.8	S-873328AUP-0ABT2x	—	—
	2.5	—	S-873325BUP-ALAT2x	—
3.0	6.9	—	—	S-873069CUP-AFFT2x
	5.9	—	—	S-873059CUP-AFGT2x
	2.5	S-873025AUP-ADAT2x	S-873025BUP-AEAT2x	S-873025CUP-AFAT2x
	2.4	S-873024AUP-ADBT2x	S-873024BUP-AEBT2x	S-873024CUP-AFBT2x
	2.3	S-873023AUP-ADCT2x	S-873023BUP-AECT2x	S-873023CUP-AFCT2x
	2.2	S-873022AUP-ADDT2x	S-873022BUP-AEDT2x	S-873022CUP-AFDT2x
	2.1	S-873021AUP-ADET2x	S-873021BUP-AEET2x	S-873021CUP-AFET2x
2.6	2.2	—	S-872622BUP-OLAT2x	—

Table 2 (2/2)

VR output voltage [V]	VD detection voltage [V]	S-87xxxxE Series	S-87xxxxG Series
5.0	11.0	S-8750B0EUP-AJIT2x	—
	8.7	S-875087EUP-AJGT2x	—
	7.7	S-875077EUP-AJFT2x	—
	6.1	S-875061EUP-AJHT2x	—
	4.2	—	S-875042GUP-ANCT2x
	3.7	—	S-875037GUP-ANET2x
	3.3	S-875033EUP-AJAT2x	—
	3.0	S-875030EUP-AJBT2x	—
3.3	11.0	S-8733B0EUP-APCT2x	—
	10.0	S-8733A0EUP-APFT2x	—
	8.2	S-873382EUP-APHT2x	—
	7.2	S-873372EUP-APET2x	—
	6.4	S-873364EUP-APGT2x	—
	4.8	S-873348EUP-APDT2x	—
	3.0	S-873330EUP-APBT2x	—
3.0	11.3	S-8730B3EUP-AMFT2x	—
	8.2	S-873082EUP-AMCT2x	—
	6.2	S-873062EUP-AMBT2x	—
	5.0	S-873050EUP-AMET2x	—
	4.2	S-873042EUP-AMDT2x	—
2.5	4.8	S-872548EUP-AZBT2x	—
	3.0	S-872530EUP-AZCT2x	—
	2.6	S-872526EUP-AZAT2x	—

Caution In the S-87xxxxB/S-87xxxxG Series, when the output voltage of the voltage regulator is close to the detection voltage of the voltage detector, the transient response of the voltage regulator may cause false detection. Please take transient response into account when deciding voltages.

Remark 1. x: G or U
2. Please select products of environmental code = U for Sn 100%, halogen-free products.

Table 3

VR output voltage [V]	VD release voltage [V]	S-87xxxxF Series
5.0	8.7	S-875087FUP-AKAT2x

Remark 1. x: G or U
2. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Pin Configuration

SOT-89-5
Top view

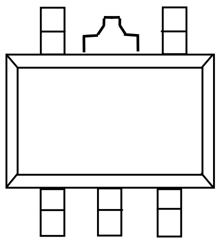


Figure 6

Table 4

Pin No.	Symbol	Description
1	VOUT	Voltage output pin of voltage regulator
2	VSS	Ground pin
3	CD (A/B/F type)	Connection pin of external capacitor for delay of voltage detector
	$\overline{\text{VPF}}$ (C/G type)	Input pin of shutdown circuit
	SENSE (E type)	Voltage monitoring pin of voltage detector
4	VOR	Output pin of voltage detector, Nch opendrain output
5	VIN	Positive power-supply

■ Absolute Maximum Ratings

Table 5

(Unless otherwise specified: Ta=25°C)

Item	Symbol	Absolute maximum rating	Unit
Input voltage[*1]	V_{IN}	V_{SS}−0.3 to V_{SS}+26	V
	V_{CD} (A/B/F type)	V_{SS}−0.3 to V_{IN}+0.3	
	$\overline{V_{PF}}$ (C/G type)	V_{SS}−0.3 to V_{SS}+26	
	V_{SENSE} (E type)		
Output voltage	V_{OUT}	V_{SS}−0.3 to V_{IN}+0.3	
Output voltage of voltage detector	V_{OR}	V_{SS}−0.3 to V_{SS}+26	
Power dissipation	P_D	500 (When not mounted on board)	mW
		1000[*2]	
Operating ambient temperature	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−40 to +125	

***1.** Even pulse (μs) noise exceeding the above input voltage (V_{SS}+26 V) may damage the IC. Observe the rated input voltage (V_{SS}+26 V).

***2.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

(1) When mounted on board **(2) When not mounted on board**

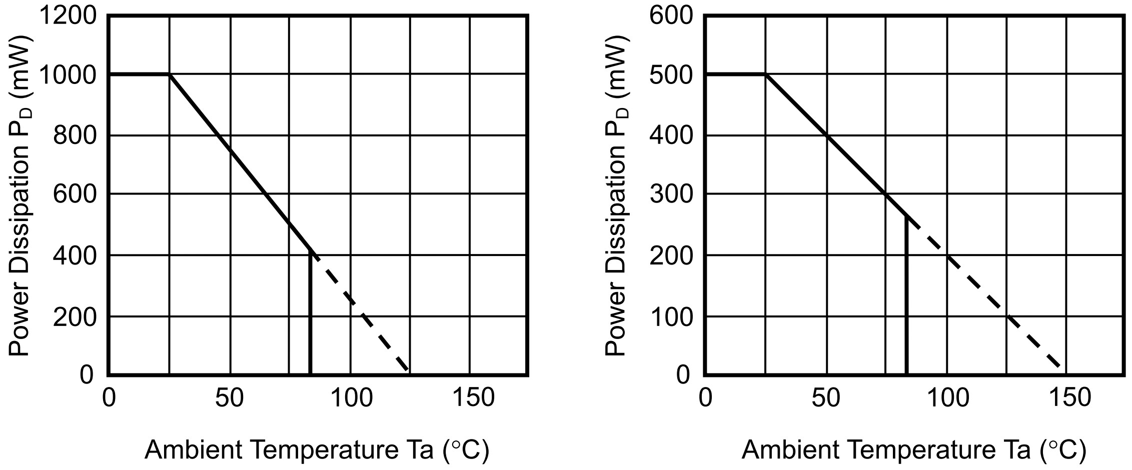


Figure 7 Power dissipation of package

■ Electrical Characteristics

1. S-8750xxA Series/S-8750xxB Series

Table 6

(Unless otherwise specified: Ta=25°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator								
Output voltage	V_{OUT}	V_{IN}=7 V, I_{OUT}=30 mA		4.88	5.00	5.12	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA		—	0.15	0.40	V	1
Line regulation	ΔV_{OUT1}	V_{IN}=6 to 24 V, I_{OUT}=30 mA		—	15	50	mV	1
Load regulation	ΔV_{OUT2}	V_{IN}=7 V, I_{OUT}=50 μA to 40 mA		—	15	50	mV	1
Input voltage	V_{IN}	—		—	—	24	V	1
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=7 V, I_{OUT}=30 mA, Ta=–40°C to +85°C		—	±0.38	±1.52	mV /°C	1
Voltage Detector								
Operating voltage	V_{opr}	—		1.3	—	24	V	2
Delay time[*1]	t_{pd}	C_D=4.7 nF		15	27	41	ms	3
Tempertue characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=–40°C to +85°C		—	±0.5	±2.0	mV /°C	2
Detection voltage	$-V_{DET}$	S-875045A/B		4.392	4.50	4.608	V	2
		S-875043A/B		4.196	4.30	4.404		
		S-875041A/B		4.001	4.10	4.199		
		S-875039A/B		3.806	3.90	3.994		
		S-875037A/B		3.611	3.70	3.789		
		S-875021B		2.049	2.10	2.151		
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V	V_{IN}=1.3 V	0.25	0.60	—	mA	4
			V_{IN}=2.4 V	1.50	2.60	—		
			V_{IN}=3.6 V	3.00	4.50	—		
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V, V_{IN}=10 V		—	—	0.1	μA	4
Hysteresis width	V_{HYS}	S-875045A/B		$-V_{DET}$ ×0.01	—	$-V_{DET}$ ×0.025	V	2
		S-875043A/B to S-875021A/B		$-V_{DET}$ ×0.03	—	$-V_{DET}$ ×0.08		
Total								
Current consumption[*2]	I_{SS}	V_{IN}=7 V, Unloaded		—	3	8	μA	5

***1.** t_{pd} (ms)=(3.18 min., 5.74 typ., 8.73 max.)×C_D (nF)
***2.** Excluding the charging current of C_D

2. S-8730xxA Series/S-8730xxB Series

Table 7

(Unless otherwise specified: Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator							
Output voltage	V_{OUT}	V_{IN}=5 V, I_{OUT}=30 mA	2.928	3.000	3.072	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA	—	0.45	0.70		
Line regulation	ΔV_{OUT1}	V_{IN}=4 to 24 V, I_{OUT}=30 mA	—	15	50	mV	
Load regulation	ΔV_{OUT2}	V_{IN}=5 V, I_{OUT}=50 μA to 40 mA	—	15	50		
Input voltage	V_{IN}	—	—	—	24	V	
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=5 V, I_{OUT}=30 mA, Ta=–40°C to +85°C	—	±0.23	±0.92	mV /°C	
Voltage Detector							
Operating voltage	V_{opr}	—	1.3	—	24	V	2
Delay time[*1]	t_{pd}	C_D=4.7 nF	15	27	41	ms	3
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=–40°C to +85°C	—	±0.3	±1.2	mV /°C	2
Detection voltage	$-V_{DET}$	S-873025A/B	2.440	2.500	2.560	V	
		S-873024A/B	2.342	2.400	2.458		
		S-873023A/B	2.244	2.300	2.356		
		S-873022A/B	2.147	2.200	2.253		
		S-873021A/B	2.049	2.100	2.151		
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V; V_{IN}=1.3 V Other than below	0.25	0.60	—	mA	4
		Nch, V_{DS}=0.5 V; V_{IN}=2.4 V S-873025A/B	1.50	2.60	—		
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V, V_{IN}=10 V	—	—	0.1	μA	
Hysteresis width	V_{HYS}	—	$-V_{DET}$ ×0.03	—	$-V_{DET}$ ×0.08	V	2
Total							
Current consumption[*2]	I_{SS}	V_{IN}=5 V, Unloaded	—	3	8	μA	5

***1.** t_{pd} (ms)=(3.18 min., 5.74 typ., 8.73 max.)×C_D (nF)
***2.** Excluding the charging current of C_D

3. S-875635B

Table 8

(Unless otherwise specified: Ta=25°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator								
Output voltage	V_{OUT}	V_{IN}=7.6 V, I_{OUT}=30 mA		5.465	5.60	5.735	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA		—	0.15	0.40		
Line regulation	ΔV_{OUT1}	V_{IN}=6.6 to 24 V, I_{OUT}=30 mA		—	15	50	mV	
Load regulation	ΔV_{OUT2}	V_{IN}=7.6 V, I_{OUT}=50 μA to 40 mA		—	15	50		
Input voltage	V_{IN}	—		—	—	24	V	
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=7.6 V, I_{OUT}=30 mA, Ta=–40°C to +85°C		—	±0.43	±1.72	mV /°C	
Voltage Detector								
Operating voltage	V_{opr}	—		1.3	—	24	V	2
Delay time[*1]	t_{pd}	C_D=4.7 nF		15	27	41	ms	3
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=–40°C to +85°C		—	±0.3	±1.2	mV /°C	2
Detection voltage	$-V_{DET}$	—		3.416	3.50	3.584	V	
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V	V_{IN}=1.3 V	0.25	0.60	—	mA	4
			V_{IN}=2.4 V	1.50	2.60	—		
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V, V_{IN}=10 V		—	—	0.1	μA	
Hysteresis width	V_{HYS}	—		$-V_{DET}$ ×0.03	—	$-V_{DET}$ ×0.08	V	2
Total								
Current consumption[*2]	I_{SS}	V_{IN}=7.6 V, Unloaded		—	4	8	μA	5

***1.** t_{pd} (ms)=(3.18 min., 5.74 typ., 8.73 max.)×C_D (nF)
***2.** Excluding the charging current of C_D

4. S-873325B

Table 9

(Unless otherwise specified: Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator							
Output voltage	V_{OUT}	V_{IN}=5.3 V, I_{OUT}=30 mA	3.220	3.300	3.380	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA	—	0.45	0.70		
Line regulation	ΔV_{OUT1}	V_{IN}=4.3 to 24 V, I_{OUT}=30 mA	—	15	50	mV	
Load regulation	ΔV_{OUT2}	V_{IN}=5.3 V, I_{OUT}=50 μA to 40 mA	—	15	50		
Input voltage	V_{IN}	—	—	—	24	V	
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=5.3 V, I_{OUT}=30 mA, Ta=−40°C to +85°C	—	±0.25	±1.00	mV/°C	
Voltage Detector							
Operating voltage	V_{opr}	—	1.3	—	24	V	2
Delay time[*1]	t_{pd}	C_D=4.7 nF	15	27	41	ms	3
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=−40°C to +85°C	—	±0.2	±0.8	mV/°C	2
Detection voltage	$-V_{DET}$	—	2.440	2.500	2.560	V	
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V, V_{IN}=1.3 V	0.25	0.60	—	mA	4
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V, V_{IN}=10 V	—	—	0.1	μA	
Hysteresis width	V_{HYS}	—	$-V_{DET}$ ×0.03	—	$-V_{DET}$ ×0.08	V	2
Total							
Current consumption[*2]	I_{SS}	V_{IN}=5.3 V, Unloaded	—	4	8	μA	5

***1.** t_{pd} (ms)=(3.18 min., 5.74 typ., 8.73 max.)×C_D (nF)
***2.** Excluding the charging current of C_D

5. S-8750xxC Series/S-875037G

Table 10 (1/2)

(Unless otherwise specified: Ta=25°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator								
Output voltage	V_{OUT}	V_{IN}=7 V, I_{OUT}=30 mA		4.88	5.00	5.12	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA		—	0.15	0.40		
Line regulation	ΔV_{OUT1}	V_{IN}=6 to 24 V, I_{OUT}=30 mA		—	15	50	mV	
Load regulation	ΔV_{OUT2}	V_{IN}=7 V, I_{OUT}=50 μA to 40 mA		—	15	50		
Input voltage	V_{IN}	—		—	—	24	V	
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=7 V, I_{OUT}=30 mA, Ta=–40°C to +85°C		—	±0.38	±1.52	mV /°C	
Shutdown output voltage	$V_{OUT/OFF}$	V_{IN}=7 V, $\overline{VPF}$ ="L", R_L=1 MΩ		—	—	0.1	V	6
Voltage Detector								
Operating voltage	V_{opr}	—		1.3	—	24	V	2
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=–40°C to +85°C	S-8750B0C	—	±0.8	±3.2	mV /°C	2
			S-875077C	—	±0.6	±2.4		
			S-875061C to S-875037C, S-875037G	—	±0.5	±2.0		
Detection voltage	$-V_{DET}$	S-8750B0C		10.736	11.00	11.264	V	
		S-875077C		7.515	7.70	7.885		
		S-875061C		5.953	6.10	6.247		
		S-875045C		4.392	4.50	4.608		
		S-875043C		4.196	4.30	4.404		
		S-875041C		4.001	4.10	4.199		
		S-875039C		3.806	3.90	3.994		
		S-875037C/S-875037G		3.611	3.70	3.789		
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V	V_{IN}=1.3 V	0.25	0.60	—	mA	4
			V_{IN}=2.4 V	1.50	2.60	—		
			V_{IN}=3.6 V	3.00	4.50	—		
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V	V_{IN}=10 V S-875077C to S-875037C, S-875037G	—	—	0.1	μA	
			V_{IN}=15 V S-8750B0C					
Hysteresis width	V_{HYS}	S-875045C		$-V_{DET}$ ×0.01	—	$-V_{DET}$ ×0.025	V	2
		S-8750B0C to S-875061C, S-875043C to S-875037C, S-875037G		$-V_{DET}$ ×0.03	—	$-V_{DET}$ ×0.08		

Table 10 (2/2)

(Unless otherwise specified: Ta=25°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Total								
Current consumption	I_{SS}	V_{IN}=7 V, Unloaded	S-8750B0C to S-875061C	—	4	8	μA	5
			S-875045C to S-875037C, S-875037G	—	3	8		
	I_{of}	$\overline{V_{PF}}$ ="L", Shutdown, V_{IN}=7 V		—	1.5	3.5		
Shutdown input voltage	V_{IL}	$\overline{V_{PF}}$ ="L", Shutdown, V_{IN}=7 V		—	—	0.4	V	6
	V_{IH}	$\overline{V_{PF}}$ ="H", Power on, V_{IN}=7 V		2.0	—	—		

6. S-8730xxC Series

Table 11

(Unless otherwise specified: Ta=25°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator								
Output voltage	V_{OUT}	V_{IN}=5 V, I_{OUT}=30 mA		2.928	3.000	3.072	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA		—	0.45	0.70		
Line regulation	ΔV_{OUT1}	V_{IN}=4 to 24 V, I_{OUT}=30 mA		—	15	50	mV	
Load regulation	ΔV_{OUT2}	V_{IN}=5 V, I_{OUT}=50 μA to 40 mA		—	15	50		
Input voltage	V_{IN}	—		—	—	24	V	
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=5 V, I_{OUT}=30 mA, Ta=−40°C to +85°C		—	±0.23	±0.92	mV /°C	
Shutdown output voltage	V_{OUTOFF}	V_{IN}=5V, $\overline{V_{PF}}$ ="L", R_L=1 MΩ		—	—	0.1	V	6
Voltage Detector								
Operating voltage	V_{opr}	—		1.3	—	24	V	2
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=−40°C to +85°C	S-873069C	—	±0.5	±2.0	mV /°C	
			S-873025C to S-873021C	—	±0.3	±1.2		
Detection voltage	$-V_{DET}$	S-873069C		6.734	6.900	7.066	V	
		S-873025C		2.440	2.500	2.560		
		S-873024C		2.342	2.400	2.458		
		S-873023C		2.244	2.300	2.356		
		S-873022C		2.147	2.200	2.253		
		S-873021C		2.049	2.100	2.151		
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V	V_{IN}=1.3 V Other than below	0.25	0.60	—	mA	4
			V_{IN}=2.4 V S-873069C, S-873025C	1.50	2.60	—		
			V_{IN}=3.6 V S-873069C	3.00	4.50	—		
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V, V_{IN}=10 V		—	—	0.1	μA	
Hysteresis width	V_{HYS}	—		$-V_{DET}$ ×0.03	—	$-V_{DET}$ ×0.08	V	2
Total								
Current consumption	I_{SS}	V_{IN}=5 V, Unloaded		—	3	8	μA	5
	I_{of}	$\overline{V_{PF}}$ ="L", Shutdown, V_{IN}=5 V		—	1.5	3.5		
Shutdown input voltage	V_{IL}	$\overline{V_{PF}}$ ="L", Shutdown, V_{IN}=5 V		—	—	0.4	V	6
	V_{IH}	$\overline{V_{PF}}$ ="H", Power on, V_{IN}=5 V		2.0	—	—		

7. S-875271C, S-875255C

Table 12

(Unless otherwise specified: Ta=25°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator								
Output voltage	V_{OUT}	V_{IN}=7.2 V, I_{OUT}=30 mA		5.075	5.20	5.325	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA		—	0.15	0.40		
Line regulation	ΔV_{OUT1}	V_{IN}=6.2 to 24 V, I_{OUT}=30 mA		—	15	50	mV	
Load regulation	ΔV_{OUT2}	V_{IN}=7.2 V, I_{OUT}=50 µA to 40 mA		—	15	50		
Input voltage	V_{IN}	—		—	—	24	V	
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=7.2 V, I_{OUT}=30 mA, Ta=−40°C to +85°C		—	±0.40	±1.60	mV /°C	
Shutdown output voltage	V_{OUTOFF}	V_{IN}=7.2V, $\overline{V_{PF}}$ ="L", R_L=1 MΩ		—	—	0.1	V	6
Voltage Detector								
Operating voltage	V_{opr}	—		1.3	—	24	V	2
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=−40°C to +85°C	S-875271C	—	±0.5	±2.0	mV /°C	
			S-875255C	—	±0.4	±1.6		
Detection voltage	$-V_{DET}$	S-875271C		6.929	7.10	7.271	V	
		S-875255C		5.368	5.50	5.632		
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V	V_{IN}=1.3V	0.25	0.60	—	mA	4
			V_{IN}=2.4V	1.50	2.60	—		
			V_{IN}=3.6V	3.00	4.50	—		
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V, V_{IN}=10 V		—	—	0.1	µA	
Hysteresis width	V_{HYS}	—		$-V_{DET}$ ×0.03	—	$-V_{DET}$ ×0.08	V	2
Total								
Current consumption	I_{SS}	V_{IN}=7.2 V, Unloaded		—	4	8	µA	5
	I_{of}	$\overline{V_{PF}}$ ="L", Shutdown, V_{IN}=7.2 V		—	1.5	3.5		
Shutdown input voltage	V_{IL}	$\overline{V_{PF}}$ ="L", Shutdown, V_{IN}=7.2 V		—	—	0.4	V	6
	V_{IH}	$\overline{V_{PF}}$ ="H", Power on, V_{IN}=7.2 V		2.0	—	—		

8. S-875294C

Table 13

(Unless otherwise specified: Ta=25°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator								
Output voltage	V_{OUT}	V_{IN}=14.4 V, I_{OUT}=30 mA		5.075	5.20	5.325	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA		—	0.15	0.40		
Line regulation	ΔV_{OUT1}	V_{IN}=6.2 to 24 V, I_{OUT}=30 mA		—	15	50	mV	
Load regulation	ΔV_{OUT2}	V_{IN}=14.4 V, I_{OUT}=50 μA to 40 mA		—	15	50		
Input voltage	V_{IN}	—		—	—	24	V	
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=14.4 V, I_{OUT}=30 mA, Ta=−40°C to +85°C		—	±0.40	±1.60	mV /°C	
Shutdown output voltage	V_{OUTOFF}	V_{IN}=14.4 V, $\overline{VPF}$ ="L", R_L=1 MΩ		—	—	0.1	V	6
Voltage Detector								
Operating voltage	V_{opr}	—		1.3	—	24	V	2
Temperature characteristic of $-V_{DET}$	$\frac{\Delta - V_{DET}}{\Delta Ta}$	Ta=−40°C to +85°C		—	±0.7	±2.8	mV /°C	
Detection voltage	$-V_{DET}$	—		9.174	9.40	9.626	V	
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V	V_{IN}=1.3 V	0.25	0.60	—	mA	4
			V_{IN}=2.4 V	1.50	2.60	—		
			V_{IN}=3.6 V	3.00	4.50	—		
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V, V_{IN}=10 V		—	—	0.1	μA	
Hysteresis width	V_{HYS}	—		$-V_{DET}$ ×0.03	—	$-V_{DET}$ ×0.08	V	2
Total								
Current consumption	I_{SS}	V_{IN}=14.4 V, Unloaded		—	4	9	μA	5
	I_{of}	$\overline{VPF}$ ="L", Shutdown,, V_{IN}=14.4 V		—	2.1	4.7		
Shutdown input voltage	V_{IL}	$\overline{VPF}$ ="L", Shutdown, V_{IN}=14.4 V		—	—	0.4	V	6
	V_{IH}	$\overline{VPF}$ ="H", Power on, V_{IN}=14.4 V		2.6	—	—		

9. S-873361C

Table 14

(Unless otherwise specified: Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator							
Output voltage	V_{OUT}	V_{IN}=5.3 V, I_{OUT}=30 mA	3.220	3.300	3.380	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA	—	0.45	0.70		
Line regulation	ΔV_{OUT1}	V_{IN}=4.3 to 24 V, I_{OUT}=30 mA	—	15	50	mV	
Load regulation	ΔV_{OUT2}	V_{IN}=5.3 V, I_{OUT}=50 μA to 40 mA	—	15	50		
Input voltage	V_{IN}	—	—	—	24	V	
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=5.3 V, I_{OUT}=30 mA, Ta=−40°C to +85°C	—	±0.25	±1.00	mV /°C	
Shutdown output voltage	V_{OUTOFF}	V_{IN}=5.3 V, $\overline{V_{PF}}$ ="L", R_L=1 MΩ	—	—	0.1	V	6
Voltage Detector							
Operating voltage	V_{opr}	—	1.3	—	24	V	2
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=−40°C to +85°C	—	±0.5	±2.0	mV /°C	
Detection voltage	$-V_{DET}$	—	5.953	6.100	6.247	V	
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V, V_{IN}=1.3 V	0.25	0.60	—	mA	4
		V_{IN}=2.4 V	1.50	2.60	—		
		V_{IN}=3.6 V	3.00	4.50	—		
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V, V_{IN}=10 V	—	—	0.1	μA	
Hysteresis width	V_{HYS}	—	$-V_{DET}$ ×0.03	—	$-V_{DET}$ ×0.08	V	2
Total							
Current consumption	I_{SS}	V_{IN}=5.3 V, Unloaded	—	4	8	μA	5
	I_{of}	$\overline{V_{PF}}$ ="L", Shutdown, V_{IN}=5.3 V	—	1.5	3.5		
Shutdown input voltage	V_{IL}	$\overline{V_{PF}}$ ="L", Shutdown, V_{IN}=5.3 V	—	—	0.4	V	6
	V_{IH}	$\overline{V_{PF}}$ ="H", Power on, V_{IN}=5.3 V	2.0	—	—		

10. S-8750xxE Series

Table 15

(Unless otherwise specified: Ta=25°C, Connect the SENSE pin to the VIN pin.)

<table>
<tr><th>Item</th><th>Symbol</th><th colspan="2">Condition</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th><th>Test circuit</th></tr>
<tr><td colspan="9">Voltage Regulator</td></tr>
<tr><td>Output voltage</td><td>V_{OUT}</td><td colspan="2">V_{IN}=7 V, I_{OUT}=30 mA, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V</td><td>4.88</td><td>5.00</td><td>5.12</td><td>V</td><td rowspan="6">1</td></tr>
<tr><td>I/O voltage difference</td><td>V_{dif}</td><td colspan="2">I_{OUT}=30 mA, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V</td><td>—</td><td>0.15</td><td>0.40</td><td rowspan="3">mV</td></tr>
<tr><td>Line regulation</td><td>ΔV_{OUT1}</td><td colspan="2">V_{IN}=6 to 24 V, I_{OUT}=30 mA, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V</td><td>—</td><td>15</td><td>50</td></tr>
<tr><td>Load regulation</td><td>ΔV_{OUT2}</td><td colspan="2">V_{IN}=7 V, I_{OUT}=50 μA to 40 mA, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V</td><td>—</td><td>15</td><td>50</td></tr>
<tr><td>Input voltage</td><td>V_{IN}</td><td colspan="2">—</td><td>—</td><td>—</td><td>24</td><td>V</td></tr>
<tr><td>Temperature coefficient of V_{OUT}</td><td>$\frac{\Delta V_{OUT}}{\Delta Ta}$</td><td colspan="2">$V_{IN}$=7 V, I_{OUT}=30 mA, Ta=−40°C to +85°C, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V</td><td>—</td><td>±0.38</td><td>±1.52</td><td>mV /°C</td></tr>
<tr><td>Output voltage during voltage detection</td><td>V_{OUTOFF}</td><td colspan="2">V_{IN}=$-V_{DET\ (Typ.)}$−1V, R_L=1 MΩ</td><td>—</td><td>—</td><td>0.1</td><td>V</td><td>6</td></tr>
<tr><td colspan="9">Voltage Detector</td></tr>
<tr><td>Operating voltage</td><td>V_{opr}</td><td colspan="2">—</td><td>1.3</td><td>—</td><td>24</td><td>V</td><td rowspan="4">2</td></tr>
<tr><td rowspan="2">Temperature characteristic of $-V_{DET}$</td><td rowspan="2">$\frac{\Delta -V_{DET}}{\Delta Ta}$</td><td rowspan="2">Ta=−40°C to +85°C</td><td>S-875077E</td><td>—</td><td>±0.6</td><td>±2.4</td><td rowspan="2">mV /°C</td></tr>
<tr><td>S-875061E</td><td></td><td>±0.5</td><td>±2.0</td></tr>
<tr><td rowspan="2">Detection voltage</td><td rowspan="2">$-V_{DET}$</td><td colspan="2">S-875077E</td><td>7.515</td><td>7.70</td><td>7.885</td><td rowspan="2">V</td></tr>
<tr><td colspan="2">S-875061E</td><td>5.953</td><td>6.10</td><td>6.247</td></tr>
<tr><td rowspan="3">Sink current</td><td rowspan="3">I_{DOUT}</td><td rowspan="3">Nch, V_{DS}=0.5 V</td><td>V_{IN}=1.3 V</td><td>0.25</td><td>0.60</td><td>—</td><td rowspan="3">mA</td><td rowspan="4">4</td></tr>
<tr><td>V_{IN}=2.4 V</td><td>1.50</td><td>2.60</td><td>—</td></tr>
<tr><td>V_{IN}=3.6 V</td><td>3.00</td><td>4.50</td><td>—</td></tr>
<tr><td>Leakage current</td><td>I_{LEAK}</td><td colspan="2">Nch, V_{DS}=24 V, V_{IN}=$-V_{DET\ (Typ.)}$ +2 V</td><td>—</td><td>—</td><td>0.1</td><td rowspan="3">μA</td></tr>
<tr><td rowspan="2">SENSE pin input current</td><td rowspan="2">I_{SENSE}</td><td rowspan="2">V_{IN}=7 V, V_{SENSE}=$-V_{DET\ (Typ.)}$ +2 V</td><td>S-875077E</td><td>—</td><td>0.6</td><td>1.7</td><td rowspan="2">7</td></tr>
<tr><td>S-875061E</td><td>—</td><td>0.7</td><td>1.8</td></tr>
<tr><td>Hysteresis width</td><td>V_{HYS}</td><td colspan="2">—</td><td>$-V_{DET}$ ×0.03</td><td>—</td><td>$-V_{DET}$ ×0.08</td><td>V</td><td>2</td></tr>
<tr><td colspan="9">Total</td></tr>
<tr><td rowspan="3">Current consumption</td><td rowspan="2">I_{SS}</td><td rowspan="2">V_{IN}=$-V_{DET\ (Typ.)}$+2 V, Unloaded</td><td>S-875077E</td><td>—</td><td>4</td><td>8</td><td rowspan="3">μA</td><td rowspan="3">5</td></tr>
<tr><td>S-875061E</td><td>—</td><td>4</td><td>9</td></tr>
<tr><td>I_{of}</td><td colspan="2">V_{IN}=$-V_{DET\ (Typ.)}$−1 V, Shutdown</td><td>—</td><td>1.5</td><td>3.5</td></tr>
</table>

11. S-8730xxE Series

Table 16

(Unless otherwise specified: Ta=25°C, Connect the SENSE pin to the VIN pin.)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator								
Output voltage	V_{OUT}	V_{IN}=5 V, I_{OUT}=30 mA, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V		2.928	3.000	3.072	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V		—	0.45	0.70		
Line regulation	ΔV_{OUT1}	V_{IN}=4 to 24 V, I_{OUT}=30 mA, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V		—	15	50	mV	
Load regulation	ΔV_{OUT2}	V_{IN}=5 V, I_{OUT}=50 μA to 40 mA, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V		—	15	50		
Input voltage	V_{IN}	—		—	—	24	V	
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=5 V, I_{OUT}=30 mA, Ta=−40°C to +85°C, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V		—	±0.23	±0.92	mV/°C	
Output voltage during voltage detection	V_{OUTOFF}	V_{IN}=$-V_{DET\ (Typ.)}$−1 V, R_L=1 MΩ		—	—	0.1	V	6
Voltage Detector								
Operating voltage	V_{opr}	—		1.3	—	24	V	2
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=−40°C to +85°C	S-873082E	—	±0.6	±2.4	mV/°C	
			S-873062E	—	±0.5	±2.0		
Detection voltage	$-V_{DET}$	S-873082E		8.003	8.200	8.397	V	
		S-873062E		6.051	6.200	6.349		
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V	V_{IN}=1.3 V	0.25	0.60	—	mA	4
			V_{IN}=2.4 V	1.50	2.60	—		
			V_{IN}=3.6 V	3.00	4.50	—		
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V, V_{IN}=$-V_{DET\ (Typ.)}$+2 V		—	—	0.1	μA	
SENSE pin input current	I_{SENSE}	V_{IN}=5 V, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V	S-873082E	—	0.6	1.7		7
			S-873062E	—	0.6	1.8		
Hysteresis width	V_{HYS}	—		$-V_{DET}$ ×0.03	—	$-V_{DET}$ ×0.08	V	2
Total								
Current consumption	I_{SS}	V_{IN}=$-V_{DET\ (Typ.)}$+2 V, Unloaded		—	4	8	μA	5
	I_{of}	V_{IN}=$-V_{DET\ (Typ.)}$−1 V, Shutdown		—	1.5	3.5		

12. S-873330E

Table 17

(Unless otherwise specified: Ta=25°C, Connect the SENSE pin to the VIN pin.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator							
Output voltage	V_{OUT}	V_{IN}=5.3 V, I_{OUT}=30 mA, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V	3.220	3.300	3.380	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V	—	0.45	0.70		
Line regulation	ΔV_{OUT1}	V_{IN}=4.3 to 24 V, I_{OUT}=30 mA, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V	—	15	50	mV	
Load regulation	ΔV_{OUT2}	V_{IN}=5.3 V, I_{OUT}=50 μA to 40 mA, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V	—	15	50		
Input voltage	V_{IN}	—	—	—	24	V	
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=5.3 V, I_{OUT}=30 mA, Ta=−40°C to +85°C, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V	—	±0.25	±1.00	mV/°C	
Output voltage during voltage detection	V_{OUTOFF}	V_{IN}=$-V_{DET\ (Typ.)}$−1 V, R_L=1 MΩ	—	—	0.1	V	6
Voltage Detector							
Operating voltage	V_{opr}	—	1.3	—	24	V	2
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=−40°C to +85°C	—	±0.2	±0.8	mV/°C	
Detection voltage	$-V_{DET}$	—	2.928	3.000	3.072	V	
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V, V_{IN}=1.3 V	0.25	0.60	—	mA	4
		Nch, V_{DS}=0.5 V, V_{IN}=2.4 V	1.50	2.60	—		
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V, V_{IN}=$-V_{DET\ (Typ.)}$+2 V	—	—	0.1	μA	
SENSE pin input current	I_{SENSE}	V_{IN}=5.3 V, V_{SENSE}=$-V_{DET\ (Typ.)}$+2 V	—	0.5	1.3		7
Hysteresis width	V_{HYS}	—	$-V_{DET}$ ×0.03	—	$-V_{DET}$ ×0.08	V	2
Total							
Current consumption	I_{SS}	V_{IN}=$-V_{DET\ (Typ.)}$+2 V, Unloaded	—	4	8	μA	5
	I_{of}	V_{IN}=$-V_{DET\ (Typ.)}$−1 V, Shutdown	—	1.5	3.5		

13. S-8725xxE Series

Table 18

(Unless otherwise specified: Ta=25°C, Connect the SENSE pin to the VIN pin.)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator								
Output voltage	V_{OUT}	V_{IN}=4.5 V, I_{OUT}=30 mA, V_{SENSE}=–$V_{DET\ (Typ.)}$+2 V		2.440	2.500	2.560	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA, V_{SENSE}=–$V_{DET\ (Typ.)}$+2 V		—	0.65	1.00		
Line regulation	ΔV_{OUT1}	V_{IN}=4.5 to 24 V, I_{OUT}=30 mA, V_{SENSE}=–$V_{DET\ (Typ.)}$+2 V		—	15	50	mV	
Load regulation	ΔV_{OUT2}	V_{IN}=4.5 V, I_{OUT}=50 μA to 40 mA, V_{SENSE}=–$V_{DET\ (Typ.)}$+2 V		—	15	50		
Input voltage	V_{IN}	—		—	—	24	V	
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=4.5 V, I_{OUT}=30 mA, Ta=–40°C to +85°C, V_{SENSE}=–$V_{DET\ (Typ.)}$+2 V		—	±0.23	±0.92	mV/°C	
Output voltage during voltage detection	V_{OUTOFF}	V_{IN}=–$V_{DET\ (Typ.)}$–1 V, R_L=1 MΩ		—	—	0.1	V	6
Voltage Detector								
Operating voltage	V_{opr}	—		1.3	—	24	V	2
Temperature characteristic of –V_{DET}	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=–40°C to +85°C	S-872548E	—	±0.5	±2.0	mV/°C	
			S-872530E to S-872526E	—	±0.2	±0.8		
Detection voltage	–V_{DET}	S-872548E		4.685	4.800	4.915	V	
		S-872530E		2.928	3.000	3.072		
		S-872526E		2.538	2.600	2.662		
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V	V_{IN}=1.3 V	0.25	0.60	—	mA	4
			V_{IN}=2.4 V	1.50	2.60	—		
			V_{IN}=3.6 V	3.00	4.50	—		
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V, V_{IN}=–$V_{DET\ (Typ.)}$+2 V		—	—	0.1	μA	
SENSE pin input current	I_{SENSE}	V_{IN}=4.5V, V_{SENSE}=–$V_{DET\ (Typ.)}$ +2 V	S-872548E to S-872526E	—	0.5	1.3		7
Hysteresis width	V_{HYS}	S-872548E to S-872530E		–V_{DET} ×0.03	—	–V_{DET} ×0.08	V	2
		S-872526E		–V_{DET} ×0.02	—	–V_{DET} ×0.05		
Total								
Current consumption	I_{SS}	V_{IN}=–$V_{DET\ (Typ.)}$+2 V, Unloaded		—	4	8	μA	5
	I_{of}	V_{IN}=–$V_{DET\ (Typ.)}$–1 V, Shutdown		—	1.5	3.5		

14. S-875087F

Table 19

(Unless otherwise specified: Ta=25°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Voltage Regulator								
Output voltage	V_{OUT}	V_{IN}=7 V, I_{OUT}=30 mA		4.88	5.00	5.12	V	1
I/O voltage difference	V_{dif}	I_{OUT}=30 mA		—	0.15	0.40		
Line regulation	ΔV_{OUT1}	V_{IN}=6 to 24 V, I_{OUT}=30 mA		—	15	50	mV	
Load regulation	ΔV_{OUT2}	V_{IN}=7 V, I_{OUT}=50 μA to 40 mA		—	15	50		
Input voltage	V_{IN}	—		—	—	24	V	
Temperature coefficient of V_{OUT}	$\frac{\Delta V_{OUT}}{\Delta Ta}$	V_{IN}=7 V, I_{OUT}=30 mA, Ta=−40°C to +85°C		—	±0.38	±1.52	mV /°C	
Voltage Detector								
Operating voltage	V_{opr}	—		1.3	—	24	V	2
Delay time[*1]	t_{pd}	C_D=4.7 nF		15	27	41	ms	3
Release voltage vs Temperature	$\frac{\Delta +V_{DET}}{\Delta Ta}$	Ta=−40°C to +85°C		—	±0.7	±2.8	mV /°C	2
Release voltage (Overcharge detection voltage)	$+V_{DET}$	—		8.600	8.700	8.800	V	
Sink current	I_{DOUT}	Nch, V_{DS}=0.5 V	V_{IN}=1.3 V	0.25	0.60	—	mA	4
			V_{IN}=2.4 V	1.50	2.60	—		
			V_{IN}=3.6 V	3.00	4.50	—		
Leakage current	I_{LEAK}	Nch, V_{DS}=24 V, V_{IN}=15 V		—	—	0.1	μA	
Hysteresis width	V_{HYS}	—		0.085	—	0.215	V	2
Total								
Current consumption[*2]	I_{SS}	V_{IN}=7 V, Unloaded		—	4	8	μA	5

***1.** t_{pd} (ms)=(3.18min., 5.74typ., 8.73max.)×C_D(nF)
***2.** Excluding the charging current of C_D.

■ Measurement Circuits

1.

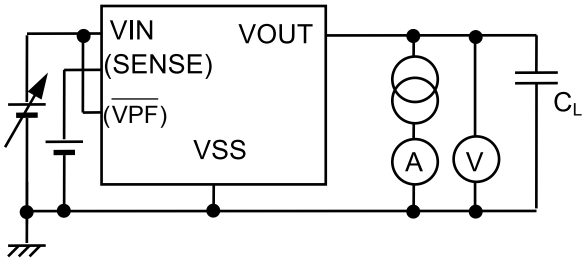


Figure 8

2.

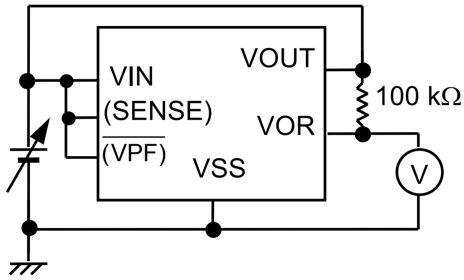


Figure 9

3.

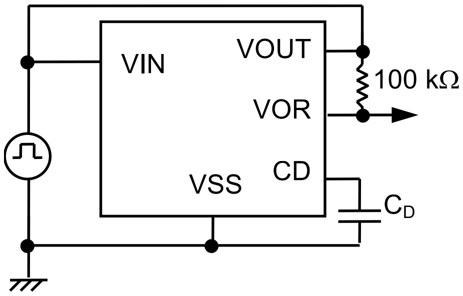


Figure 10

4.

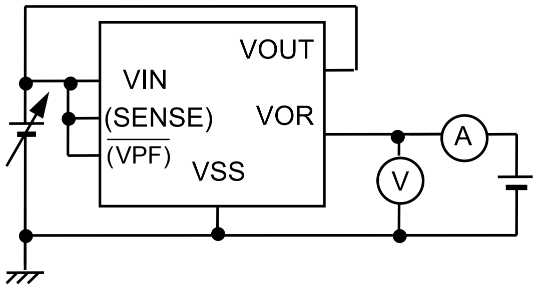


Figure 11

5.

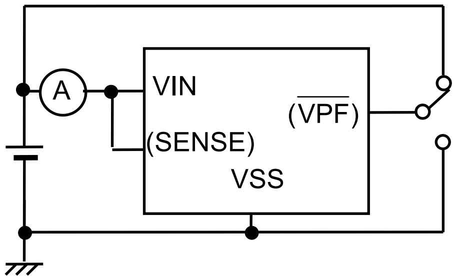


Figure 12

6.

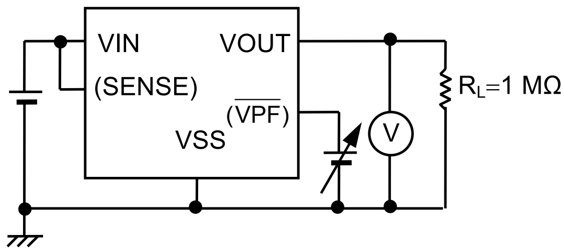


Figure 13

7.

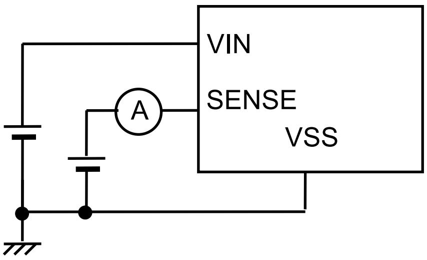
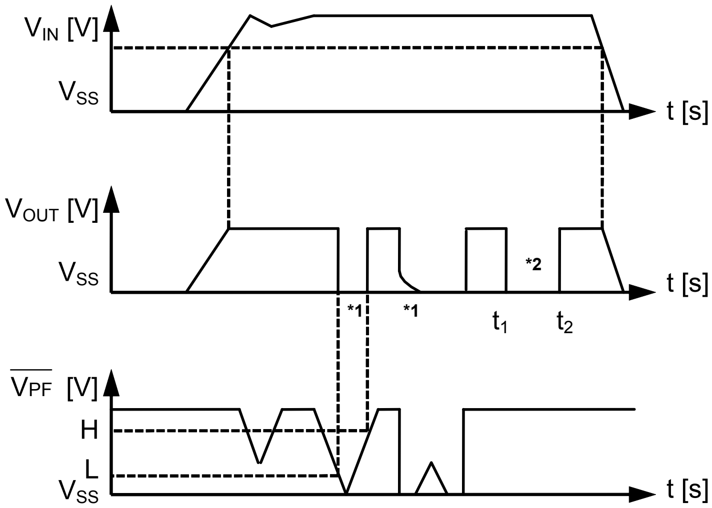


Figure 14

■ Operation Timing Charts

1. Voltage regulator (C/G type)

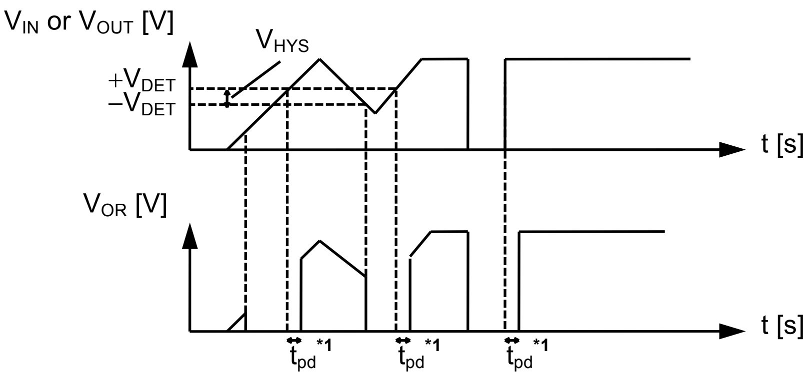


***1.** Indicates shutdown state. When the load current (I_{OUT}) is less than 1 μA, the output voltage (V_{OUT}) is not always V_{SS} level.

***2.** When the V_{OUT} is shorted at t_1, V_{OUT} becomes V_{SS} level. When the short of V_{OUT} is removed at t_2, V_{OUT} returns to normal output.

Figure 15

2. Voltage detector (A/B/F type)

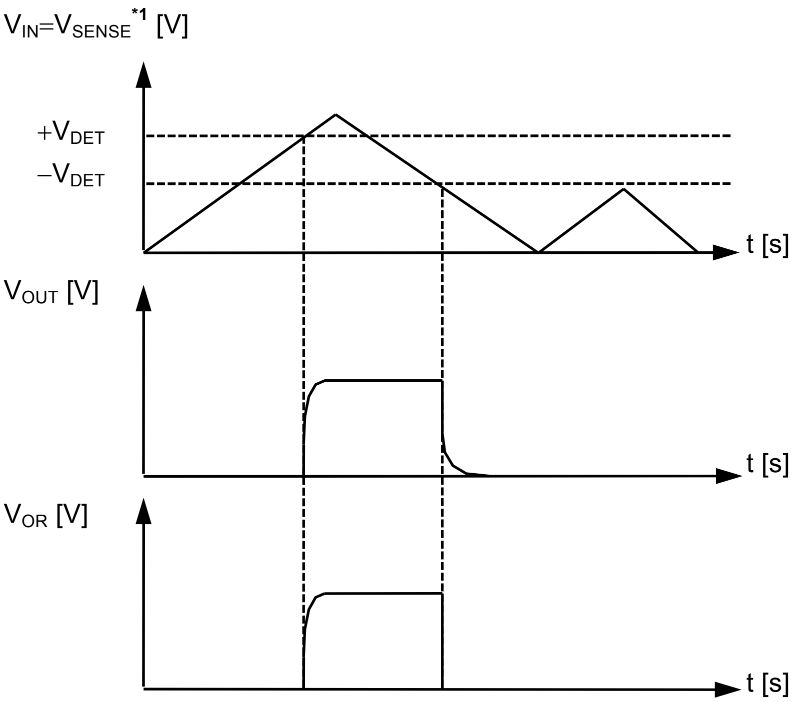


***1.** Output delay time (t_{pd}) of the voltage detector can be changed with an external capacitance value to CD pin. Delay circuit is not included in C/E/G type.

Remark Pull up V_{OR} through a resistor to V_{IN} or V_{OUT}.

Figure 16

3. When using the SENSE pin (E type)



***1.** The SENSE pin is connected to VIN pin.

Remark Pull up V_{OR} through a resistor to V_{OUT}.

Figure 17

■ Explanation of Terms

1. I/O voltage difference (V_{dif})

$V_{dif}=V_{IN1}-V_{OUT1}$

V_{OUT1}: Initial output voltage

V_{IN1}: Input voltage which generates an output voltage (V_{OUT2}) decreased by 5 % from V_{OUT1}

2. Load regulation (ΔV_{OUT2})

$\Delta V_{OUT2}=V_{OUT1}-V_{OUT2}$

V_{OUT1}: Output voltage when I_{OUT} is 50 μA

V_{OUT2}: Output voltage when I_{OUT} is 40 mA

3. Line regulation (ΔV_{OUT1})

$\Delta V_{OUT1}=V_{OUT1}-V_{OUT2}$

V_{OUT1}: Output voltage when V_{IN} is 24 V

V_{OUT2}: Output voltage when V_{IN} is (V_{OUT}+1) V

4. Hysteresis width (V_{HYS})

$V_{HYS}=(+V_{DET})-(-V_{DET})$

$+V_{DET}$: Release voltage

$-V_{DET}$: Detection voltage

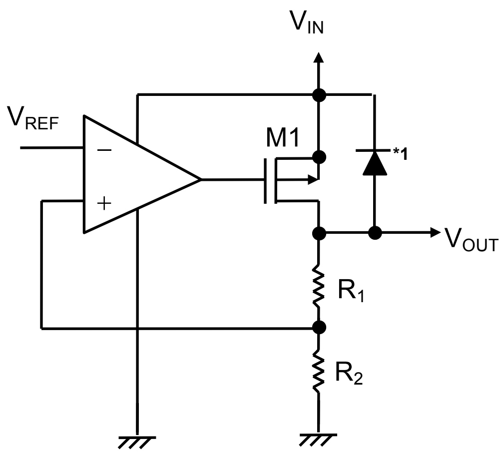
■ Operation

1. Reference voltage circuit

The reference voltage circuit operates all the time when the voltage is applied to VIN pin and is not affected by the $\overline{V_{PF}}$ signal.

2. Voltage regulator

Figure 18 shows the voltage regulator circuit. The S-87x Series has a Pch MOS transistor as the output control transistor.
Reverse current may break IC if V_{OUT} potential is higher than V_{IN}, because a parasitic diode is formed between V_{IN} and V_{OUT} due to the structure of the control transistor. Therefore, keep V_{OUT} lower than V_{IN}+0.3 V.
The output voltage of the voltage regulator can be selected as follows:
2.5 V to 5.8 V±2.4 % (0.1 V step)



***1.** Parasitic diode

Figure 18 Voltage regulator circuit

Caution For an application with a load current of less than 1 μA, the leakage current of the control transistor M1 increases the output voltage.

3. Short-circuit protection circuit

The S-87x Series has a built-in short-circuit protection circuit to protect the element from break caused by a large current in case of a short circuit. The output short current is internally limited to approx. 70 mA. Short-circuit protection circuit has three kinds characteristics according to input voltage (V_{IN}) as shown in **Figure 19 to 21**.

At 5 V Output:

(a) $V_{IN}/V_{OUT} \geq 2.0$ **(b) $1.5 \leq V_{IN}/V_{OUT} < 2.0$** **(c) $V_{IN}/V_{OUT} < 1.5$**

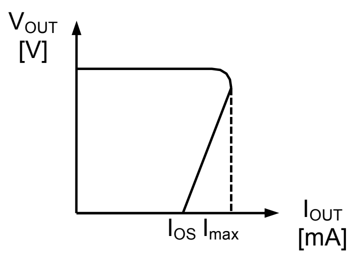


Figure 19

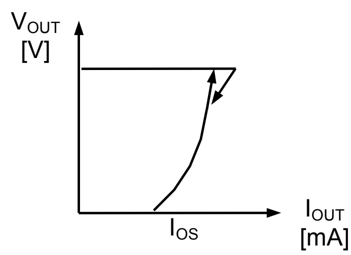


Figure 20

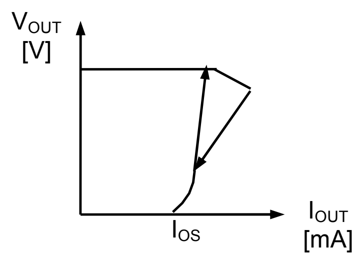


Figure 21

4. Delay circuit

The delay circuit outputs voltage detector output (V_{OR}) with delay after the voltage at V_{IN} pin has become release voltage ($+V_{DET}$) at the rising of VIN pin.

In **Figure 22**, when V_{cd} exceeds the reference voltage (V_{ref}), the output voltage pin detection voltage output (V_{OR}) changes from low to high level, providing delay output. When the voltage at VIN pin falls under the detection voltage ($-V_{DET}$), the N2 transistor turns ON, therefore the charge of the external capacitor (C_D) is rapidly discharged and the voltage detector output (V_{OR}) changes from high to low level without delay.

The external capacitor (C_D) is charged with constant current, and is practically independent of V_{IN} voltage. Its delay time (t_{pd}) is expressed by the following equation:

t_{pd} (ms)=Delay coefficient (3.18 min., 5.74 typ., 8.73 max.)$\times C_D$ (nF)

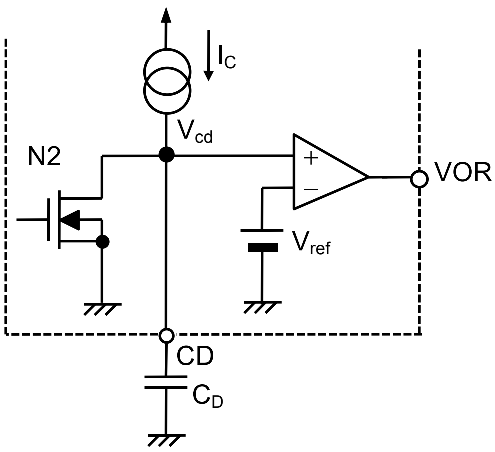


Figure 22

Caution 1. Unless an output delay is needed, keep CD pin open. Do not apply external voltage other than ground potential to CD pin, which may cause IC breakdown.

2. When designing your printed-circuit board layout, take care that no leakage current flows to the external capacitor (C_D), otherwise the correct delay time may not be obtained. Because the value of the constant current source (I_C) is only 195 nA, C_D to impedance is high.

5. Voltage detection circuit

The built-in voltage detection circuit (Nch opendrain type) is equivalent to our S-808 Series/S-809 Series voltage detectors. A pull-up resistor of about 100 kΩ is required for output. Since the comparator power of this circuit is supplied from VIN pin, this circuit operates while voltage is applied to VIN pin.
The detection voltage of the voltage detector can be selected as follows:

2.1 V to 11.3 V±2.4 % (0.1 V step)

In the F type, the release voltage ($+V_{DET}$) accuracy is ±1.1 %. So, it responds to the application for overcharge detection of lithium-ion battery packs.
In the E type, the input voltage monitoring pin of the voltage detector is externally connected as the SENSE pin. Because this pin is configured by a resistor only, temporary current such as a through-type current does not flow. Consequently even when resistor (R_{IN}) is inserted between input power supply and VIN pin, the input power voltage can be accurately monitored by connecting the SENSE pin to the input power supply. Also, when a drop in the SENSE pin input voltage is detected, the voltage detector generates a reset signal. At the same time, it powers off the voltage regulator.

Caution 1. As shown in Figure 23 to 25, when connecting V_{OR} output to $\overline{\text{VPF}}$ pin in the C type or connecting SENSE pin to VIN pin in the E type, the following phenomena occur if resistor (R_{IN}) is connected between input voltage and VIN pin. Be careful.

(1) At the time of voltage detection, the voltage regulator is shutdown and load current is cut. Therefore, VIN pin voltage increases by $\Delta V_{IN}=I_{IN}\times R_{IN}$, where the current flowing into R_{IN} is set to I_{IN}. Hence, if ΔV_{IN} exceeds hysterisis width (V_{HYS}), oscillation starts immediately after detection and continues. It is necessary to set ΔV_{IN} less than V_{HYS}.

(2) At the time of voltage release, the voltage regulator is powered on and load current flows. Therefore, if ΔV_{IN} exceeds hysterisis width (V_{HYS}), oscillation starts immediately after release and continues. It is necessary to set ΔV_{IN} less than V_{HYS}. Also at the time of voltage release, the rush current to charge output capacitor (C_{OUT}) flows. Hence, oscillation momentarily starts until the output of regulator (V_{OUT}) rises high enough even though ΔV_{IN} is set less than V_{HYS}. But Short-circuit protection circuit controls the rush current less than I_{MAX} on Figure 19 to 21. If this momentary oscillation is a problem in your applicaion, setting R_{IN} less than V_{HYS}/I_{MAX} prevents oscillation.

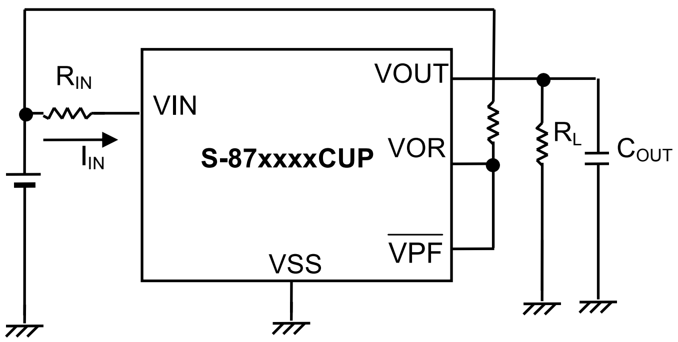


Figure 23 Attention connecting example 1

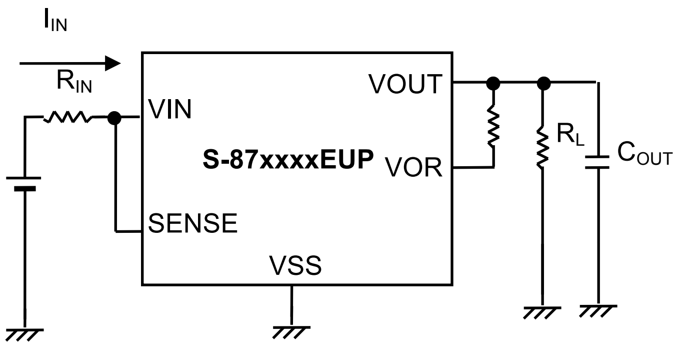


Figure 24 Attention connecting example 2

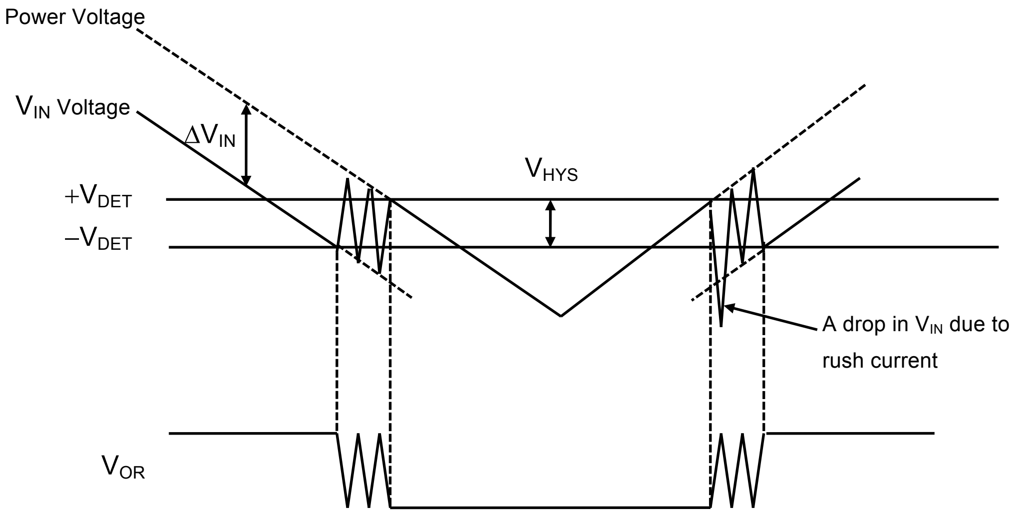


Figure 25 When $\Delta V_{IN} > V_{HYS}$

2. **In the E type, the minimum operating voltage becomes 2.0 V as V_{IN} voltage. If a drop in V_{IN} voltage occurs due to load current or rush current to be charged to the output capacitor when load current or the voltage regulator is powered on at the time of release, set V_{IN} to 2.0 V or more.**
3. **Also, in the E type, when sharply increasing only VIN pin voltage at 1 ms/V or less, with the SENSE pin fixed to $-V_{DET} \geq V_{SENSE} \geq -V_{DET} - 2$ V, a release pulse is output to the output pin of voltage detector. Be careful. In this case, this release pulse is removed by setting the time constant of VOR pin 20 ms or more with capacitance and pull-up resistance. In addition, when the voltage of SENSE pin is fixed to between the detection voltage and the release voltage at the detect condition, if sharply increasing only VIN pin voltage at 1 ms/V or less, the output of the detector turns to the release condition. If this action is a problem in your system, please connect SENSE pin to VIN pin.**

6. Shutdown circuit (C/E/G type)

When $\overline{\text{VPF}}$ pin goes low (0.4 V or less) in the C/G type or at the time of voltage detection in the E type current for the voltage regulator is shut down, the current consumption (excluding the current which flows through the pull-up resistor) lowers to 3.5 μA or less.
During shutdown, the M1 transistor in the voltage regulator shown in the **Figure 17** is off and VOUT pin is pulled down by R_1 and R_2, whose value (R_1+R_2) is 5 MΩ to 10 MΩ. Input current of $\overline{\text{VPF}}$ pin is 0.1 μA or less.

Caution 1. The output voltage may not become 0 V when the load which makes I_{OUT} under 1 μA is connected during shutdown.

2. DO NOT keep $\overline{\text{VPF}}$ pin floating state or medium potential (between low and high levels). Otherwise through-type current flows.

■ Transient Characteristics

An undershoot or an overshoot may occur in the output voltage of the voltage regulator if input voltage or load current fluctuates transiently. If an undershoot is large, the voltage detector operates to output reset signal in the B type in which the voltage detector detects the output voltage of the regulator. If an overshoot is large, the load circuit is adversely affected. Therefore it is important to determine the capacitor value so as to minimize undershoot and overshoot.

1. Line: Transient characteristics due to input voltage fluctuation

Input voltage fluctuation differs depending on the types of the signal applied: type 1 which is a rectangular wave between (V_{OUT}+1) V and 10 V, and type 2 which is a rectangular wave from 0 V to 10 V. (Refer to **Figure 26 to 27**) The ringing waveforms and parameter dependency of each type are described below. The measuring circuit is shown in **Figure 28** for reference.

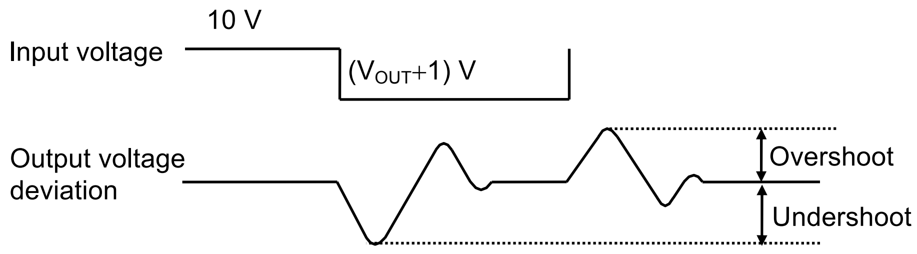
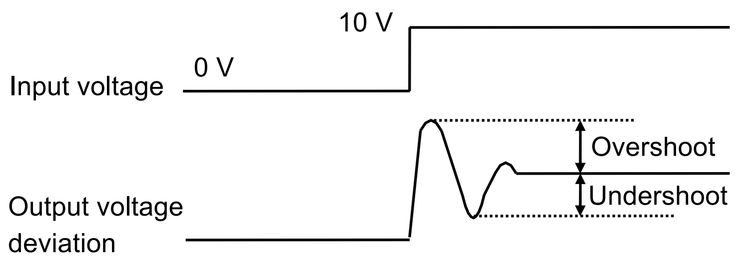
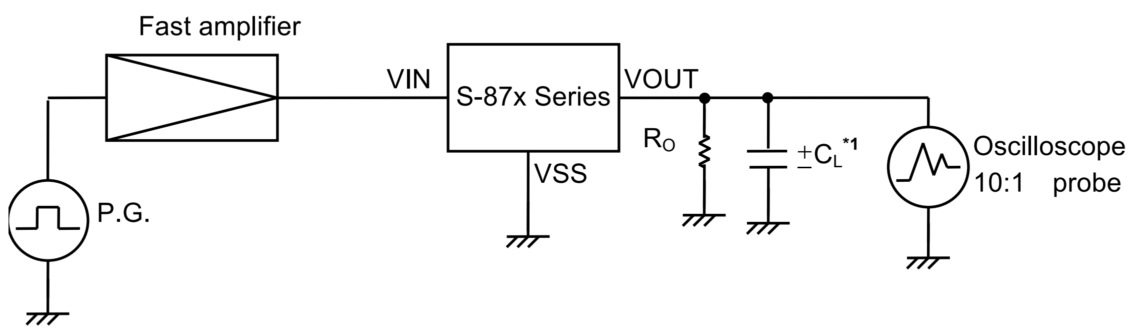


Figure 26 Rectangular wave between (V_{OUT}+1) V and 10 V (Type 1)



Remark Rise/fall time (time between 10 % and 90 %) is 1 μs.

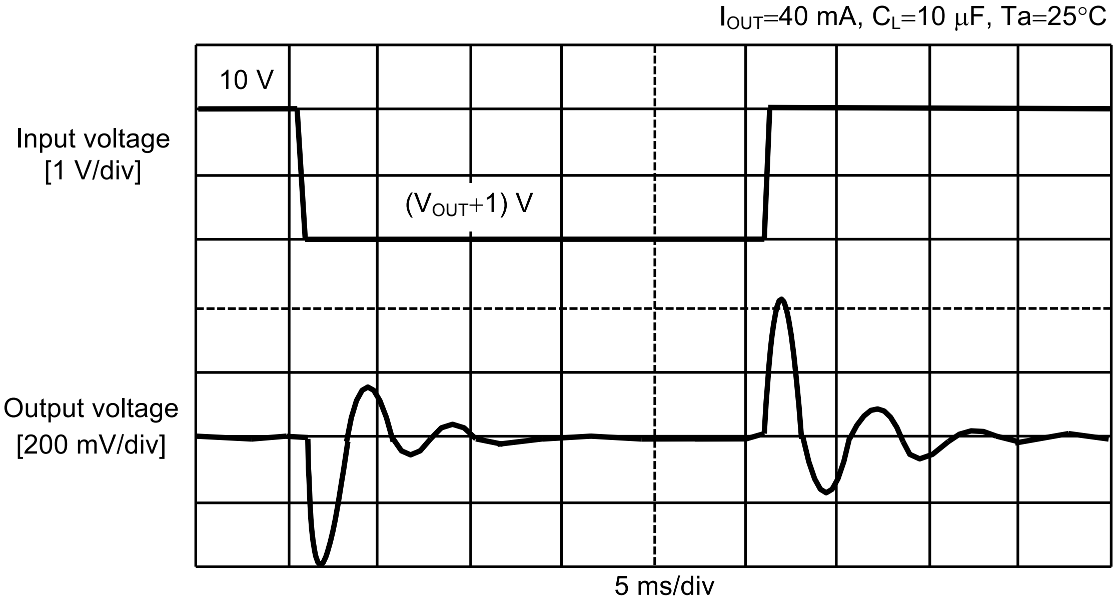
Figure 27 Rectangular wave from 0 V to 10 V (Type 2)



***1.** AL electrolytic capacitor

Figure 28 Measuring circuit

Type 1 (Rectangle wave between (V_{OUT}+1) V and 10 V)



Overshoot amount: 350 mV
Undershoot amount: 325 mV

Figure 29 Ringing waveform (Type 1)

Table 20 Parameter dependency (Type 1)

Series	Parameter	Conditions	Method to decrease overshoot	Method to decrease undershoot
S-8750xxx	Load current (I_{OUT})	10 to 60 mA, C_L=10 μF	Decrease	Decrease
	Load capacitance (C_L)	1 to 47 μF, I_{OUT}=40 mA	Increase	Increase
	Input fluctuation (ΔV_{IN}*1)	2 to 4 V	Decrease	Decrease
		4 to 18 V	Increase	Decrease
	Temperature (Ta)	–40 °C to +85 °C	Low temperature	Low temperature
S-8730xxx	Load current (I_{OUT})	10 to 60 mA, C_L=10 μF	Increase	Decrease
	Load capacitance (C_L)	1 to 47 μF, I_{OUT}=40 mA	Increase	Increase
	Input fluctuation (ΔV_{IN}*1)	4 to 20 V	Increase	Decrease
	Temperature (Ta)	–40 °C to +85 °C	Low temperature	Low temperature

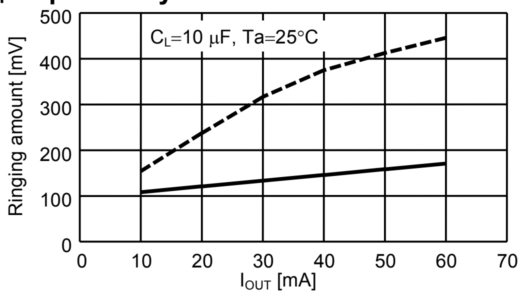
***1.** High voltage value – low voltage value

For reference, the following pages describe the ringing in V_{OUT} measured using the output load current (I_{OUT}), output load capacitance (C_L), input fluctuation width (ΔV_{IN}), and temperature (Ta) as parameters.

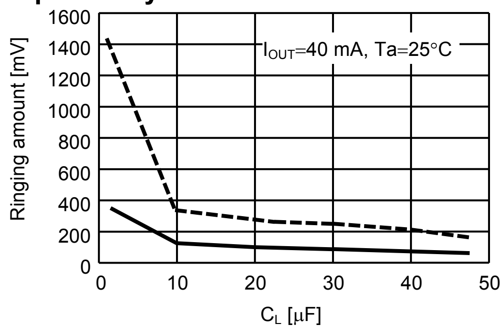
Reference Data: Type 1

S-8750xxx Series

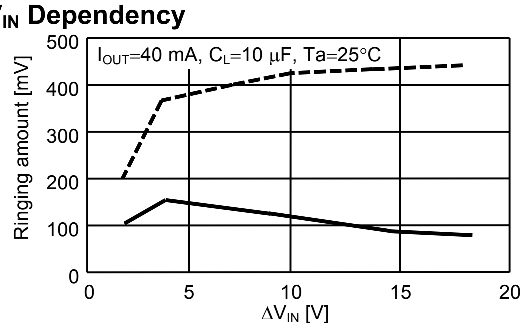
1. I_{OUT} Dependency



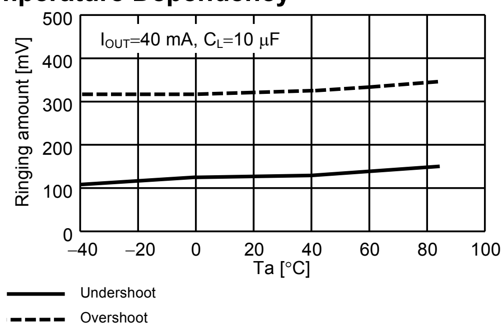
2. C_L Dependency



3. ΔV_{IN} Dependency



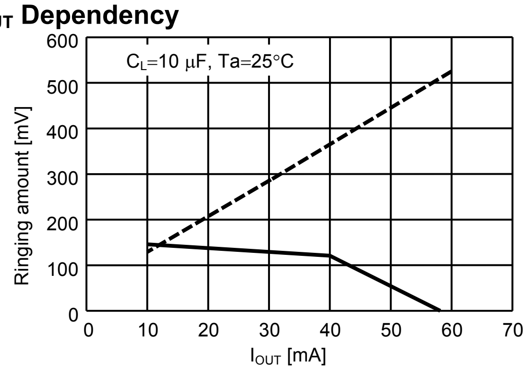
4. Temperature Dependency



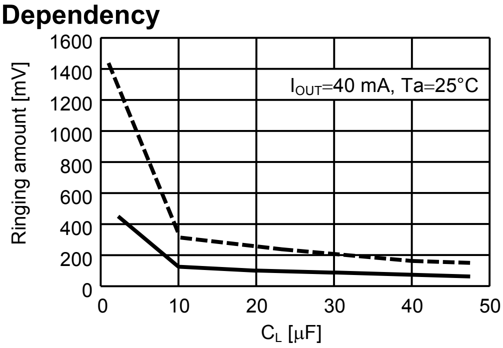
Remark The lower voltage is fixed at 6 V.

S-8730xxx Series

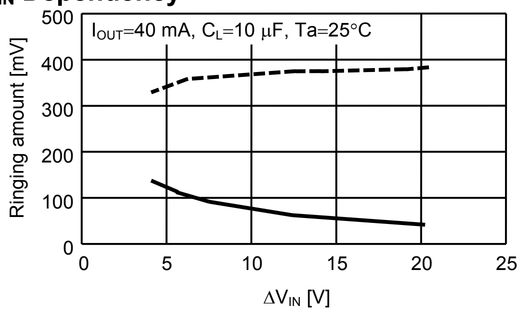
1. I_{OUT} Dependency



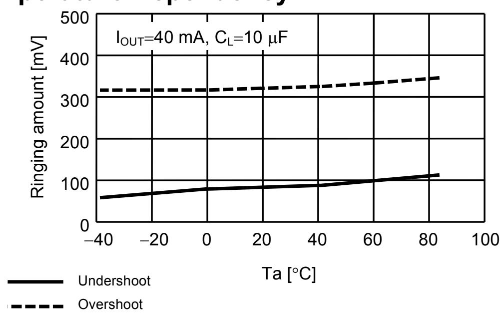
2. C_L Dependency



3. ΔV_{IN} Dependency

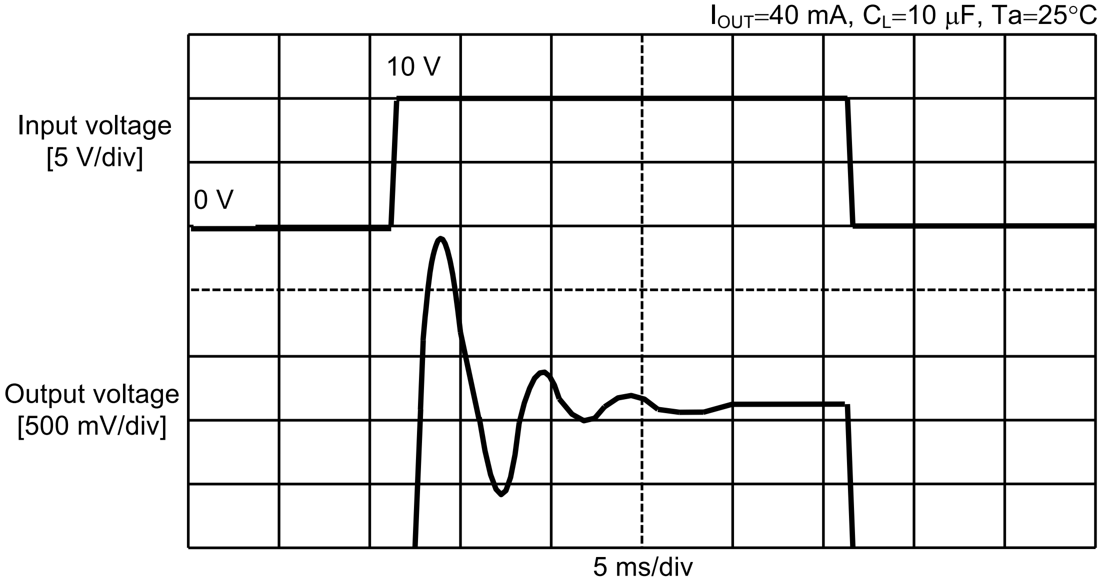


4. Temperature Dependency



Remark The lower voltage is fixed at 4 V.

Type 2 (Rectangle wave form 0 V to 10 V)



Overshoot amount: 1300 mV
Undershoot amount: 610 mV

Figure 30 Ringing waveform (Type 2)

Table 21 Parameter dependency (Type 2)

Series	Parameter	Conditions	Method to decrease overshoot	Method to decrease undershoot
S-8750xxx	Load current (I_{OUT})	10 to 60 mA, C_L=10 μF	Increase	Increase
	Load capacitance (C_L)	1 to 47 μF, I_{OUT}=40 mA	Decrease	Decrease
	Input fluctuation (ΔV_{IN}*1)	8 to 24 V	Increase	Increase
	Temperature (Ta)	−40 °C to +85 °C	Low temperature	Low temperature
S-8730xxx	Load current (I_{OUT})	10 to 60 mA, C_L=10 μF	Increase	Increase
	Load capacitance (C_L)	1 to 47 μF, I_{OUT}=40 mA	Decrease	Decrease
	Input fluctuation (ΔV_{IN}*1)	8 to 24 V	Increase	Increase
	Temperature (Ta)	−40 °C to +85 °C	Low temperature	Low temperature

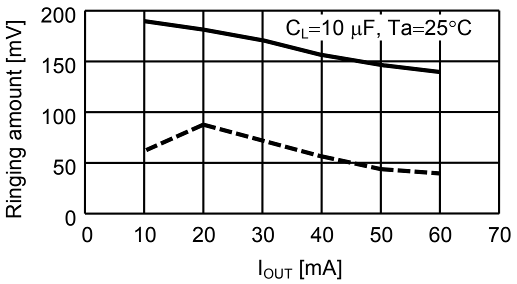
***1.** High voltage value – 0 V

For reference, the following pages describe the ringing in V_{OUT} measured using the output load current (I_{OUT}), output load capacitance (C_L), input fluctuation width (ΔV_{IN}), and temperature (Ta) as parameters.

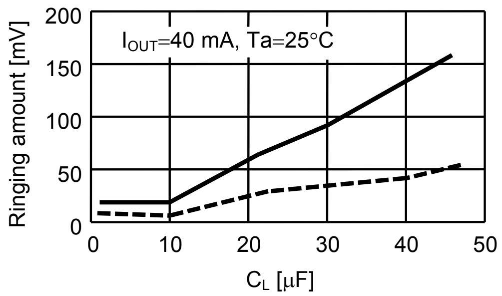
Reference Data: Type 2

S-8750xxx Series

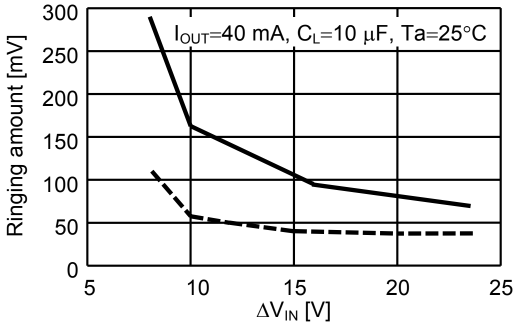
1. I_{OUT} Dependency



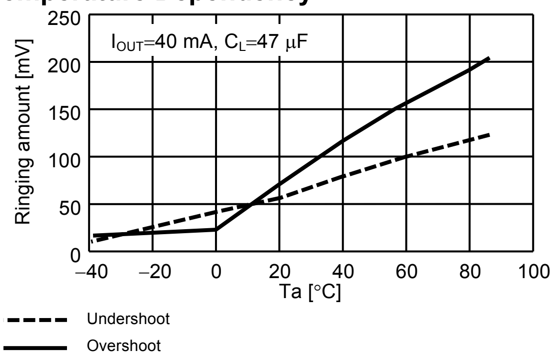
2. C_L Dependency



3. ΔV_{IN} Dependency



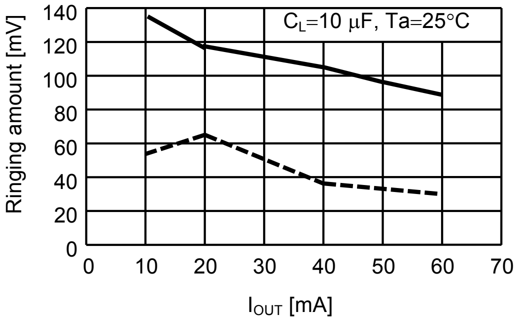
4. Temperature Dependency



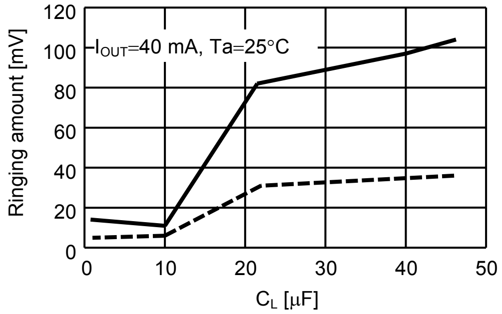
Remark The lower voltage is fixed at 0 V.

S-8730xxxSeries

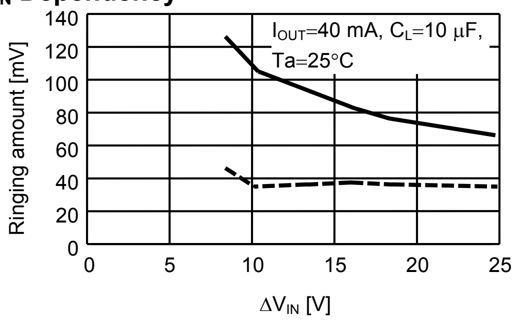
1. I_{OUT} Dependency



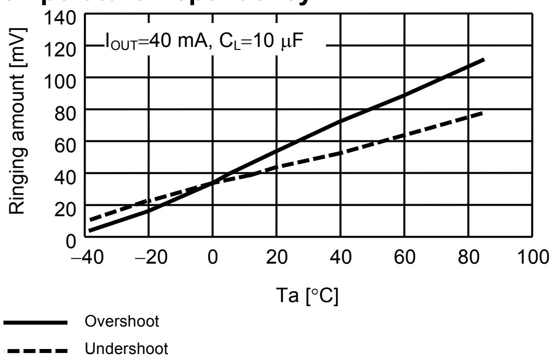
2. C_L Dependency



3. ΔV_{IN} Dependency



4. Temperature Dependency



Remark The lower voltage is fixed at 0 V.

2. Load transient response characteristics due to load current fluctuation

An overshoot and an undershoot are caused in the output voltage if the load current is changed from 50 μA to 40 mA while the input voltage is kept constant. **Figure 31** shows the output voltage fluctuation due to a change in the load current. The measuring circuit is shown in **Figure 32** for reference. The latter half of this section describes ringing waveform and parameter dependency.

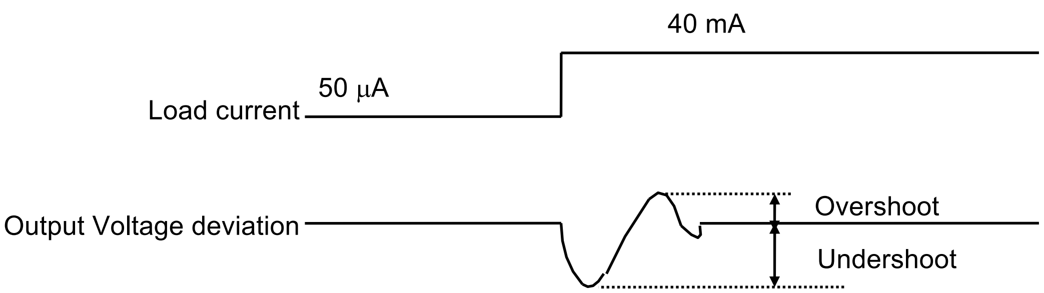
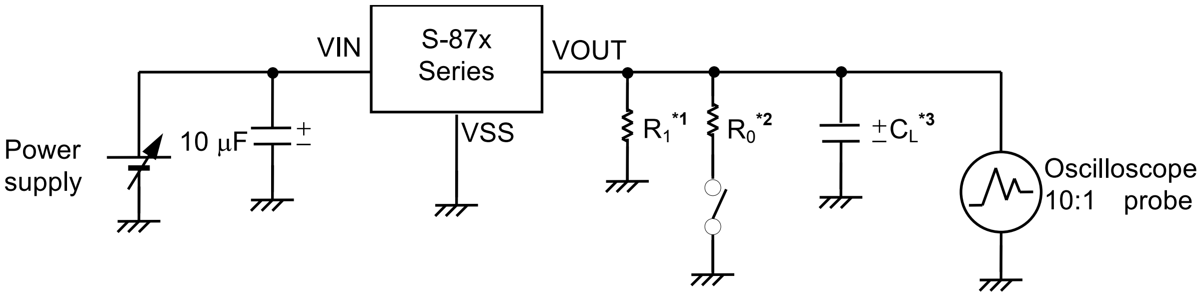


Figure 31 Output voltage fluctuation due to a change in the load current



***1.** $R_1 = \dfrac{V_{OUT}[V]}{50\ \mu A}\ [\Omega]$

***2.** $R_0 = \dfrac{V_{OUT}[V]}{40\ mA}\ [\Omega]$

***3.** AL electrolytic capacitor

Figure 32 Measuring circuit

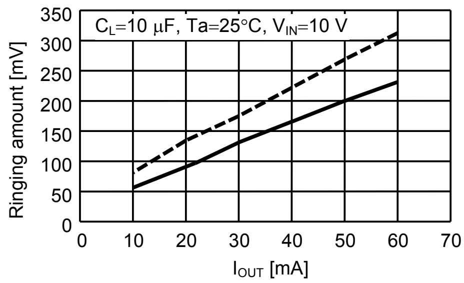
Table 22 Parameter dependency due to load current fluctuation

Series	Parameter	Conditions	Method to decrease overshoot	Method to decrease undershoot
S-8750xxx, S-8730xxx	Load current (I_{OUT})	10 to 60 mA, C_L=10 μF	Decrease	Decrease
	Load capacitance (C_L)	1 to 47 μF, I_{OUT}=40 mA	Increase	Increase
	Power supply voltage (V_{IN})	(V_{OUT}+1) to 24 V	Increase	Increase
	Temperature (Ta)	−40 °C to +85 °C	Low temperature	Low temperature

■ Reference Data

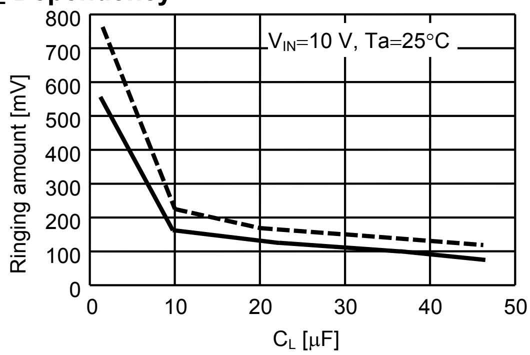
S-8750xxxSeries

1. I_{OUT} Dependency

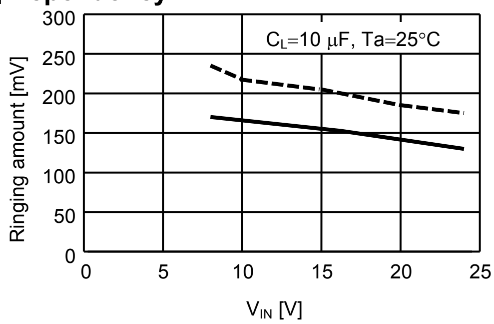


Remark The lower current is fixed at 50 μA.

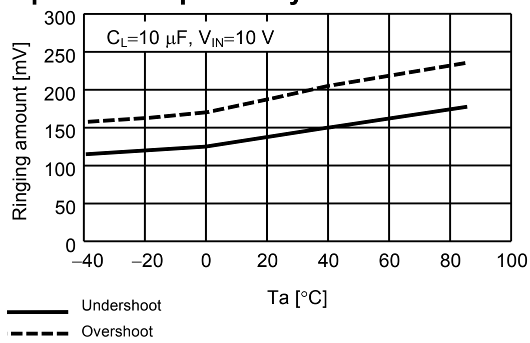
2. C_L Dependency



3. ΔV_{IN} Dependency

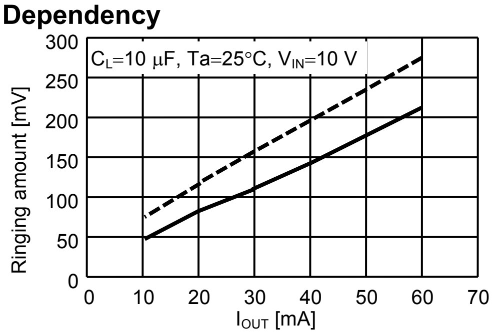


4. Temperature Dependency



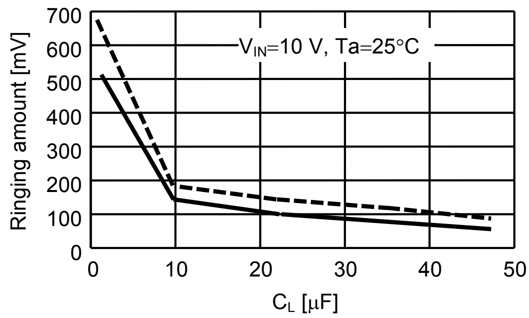
S-8730xxxSeries

1. I_{OUT} Dependency

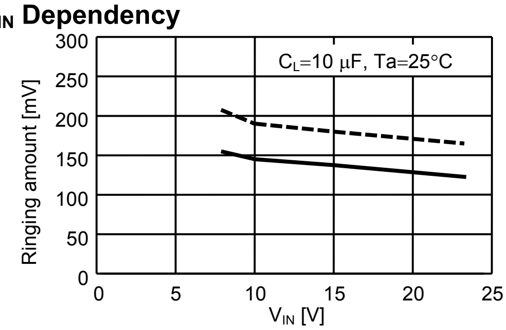


Remark The lower current is fixed at 50 μA.

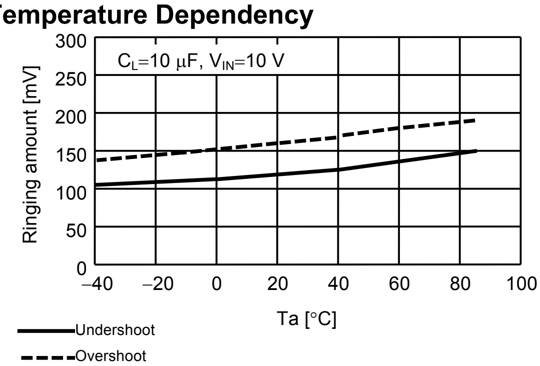
2. C_L Dependency



3. ΔV_{IN} Dependency



4. Temperature Dependency



■ Standard Circuits

1. A/B/F type

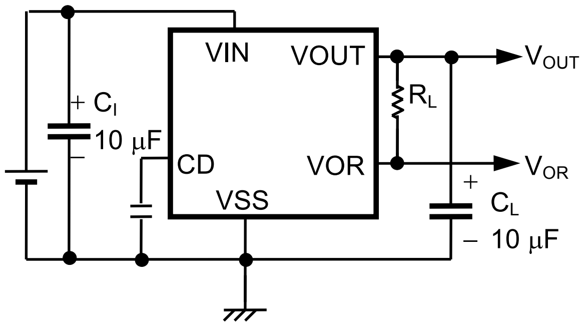


Figure 33

2. C/G type

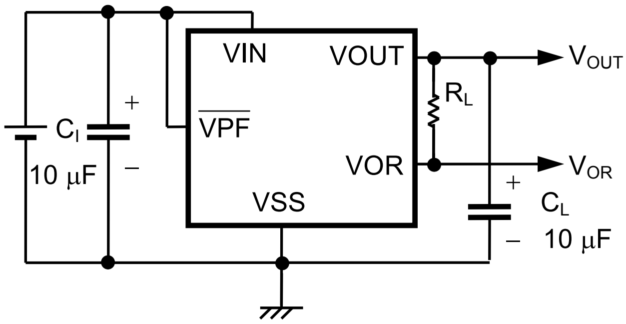


Figure 34

3. E type

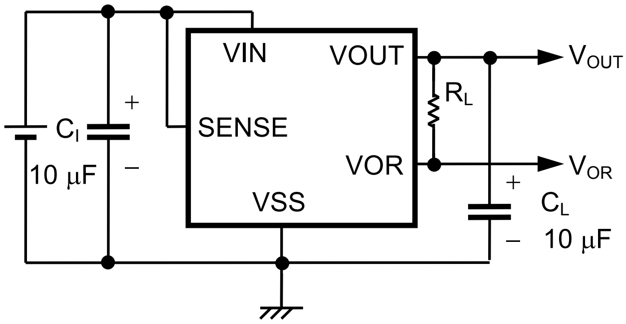


Figure 35

Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

■ Application Circuits

1. Microcomputer power supply and reset circuit

To construct a microcomputer power supply and a reset circuit using conventional ICs, a voltage regulator IC, a voltage detector IC, a delay time generation circuit and others are required. The A/B type allows you to make these circuits without these ICs, and the delay time is variable.

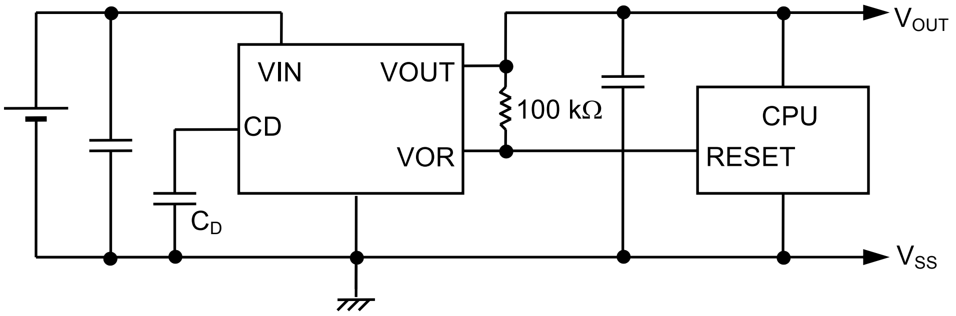


Figure 36

Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

2. Output current boost circuit

A PNP transistor is used to increase the output current.

1. A/ B type

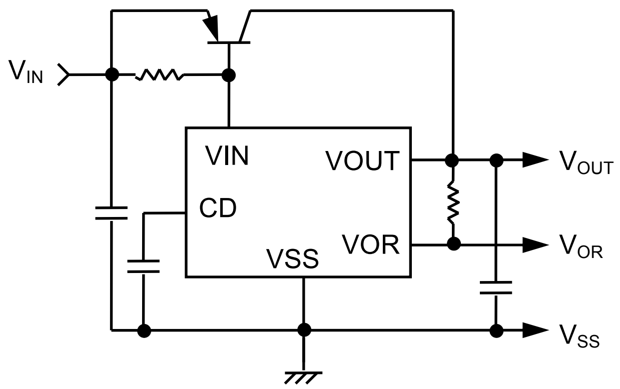


Figure 37

2. C/ G type

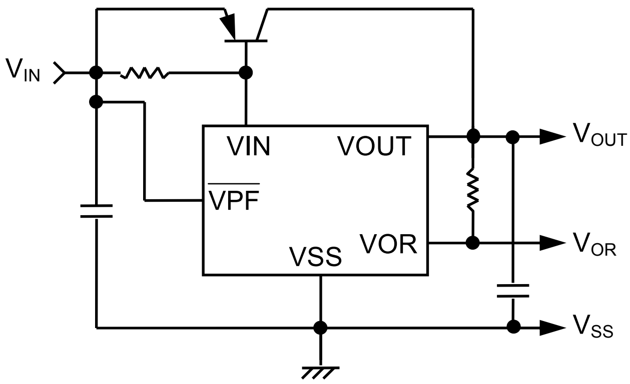


Figure 38

Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

3. Power supply for lithium-ion battery pack

When the lithium-ion battery goes down to the overdischarge voltage, the built-in voltage detector powers OFF the voltage regulator, and at the same time it transmits the RESET signal to the microcomputer. R_1, C_1, R_2 and C_2 are attached to eliminate the voltage exceeding the absolute maximum ratings of charger. C_3 is attached to give a delay and to release the RESET signal after power supply voltage for microcomputer (V_{OUT}) rises high enough.

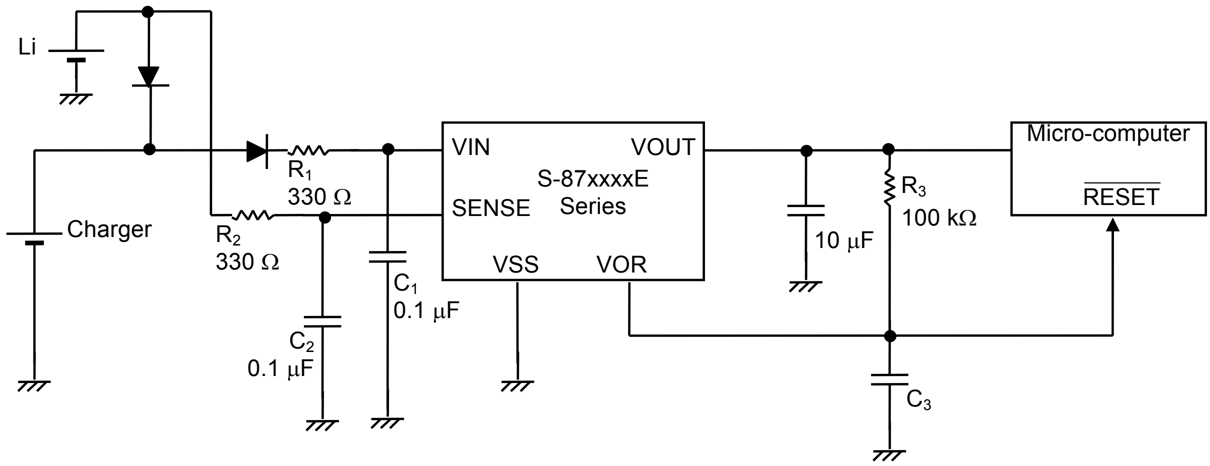
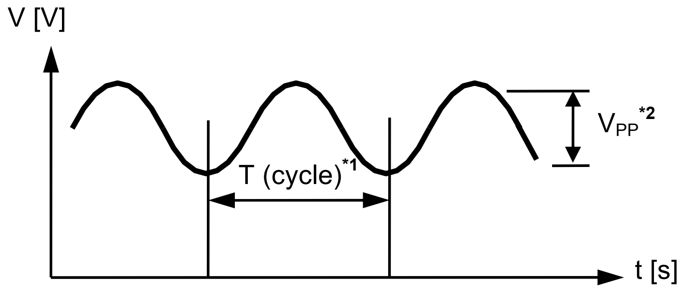


Figure 39

Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

■ Precautions

- DO NOT apply a ripple voltage of the following both conditions to VIN pin.



***1.** $f \geq 1000$ Hz ($f = \frac{1}{T}$) ("f" shows the frequency)

***2.** $V_{PP} \geq 0.5$ V

Figure 40

- When connecting another power supply to the voltage regulator output pin, insert a diode to protect the IC.

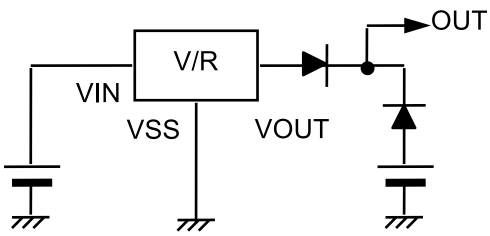


Figure 41

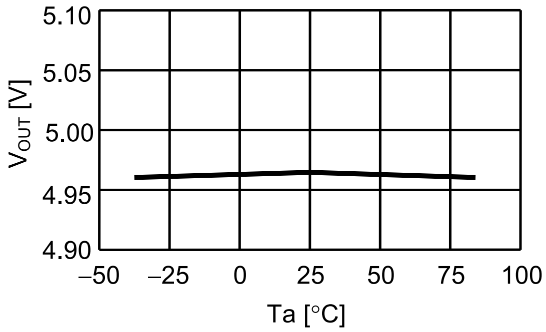
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

■ Characteristics (Typical Data)

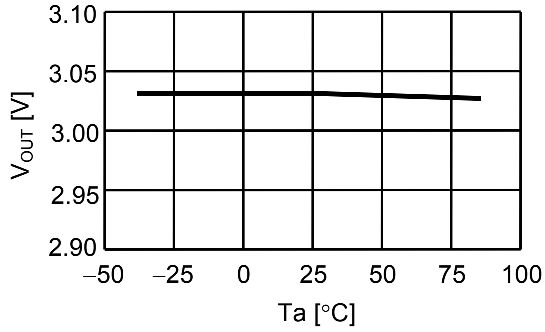
1. Voltage regulator

(1) Output voltage (V_{OUT}) - Temperature (Ta) characteristics

S-8750xxx Series

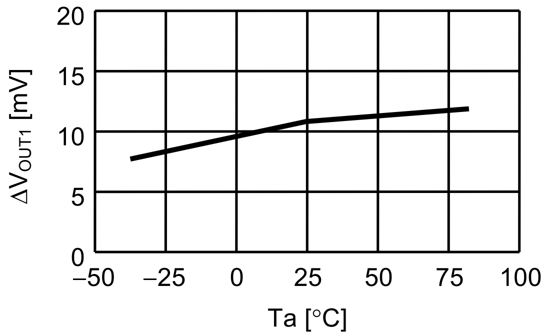


S-8730xxx Series

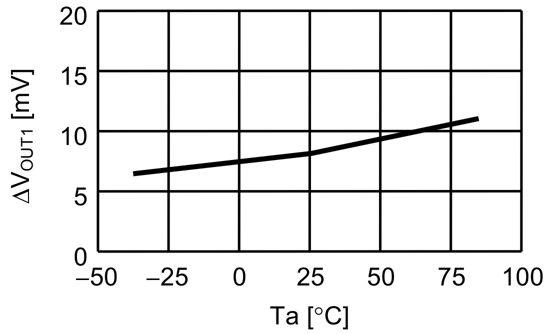


(2) Line regulation(ΔV_{OUT1}) - Temperature (Ta) characteristics

S-8750xxx Series

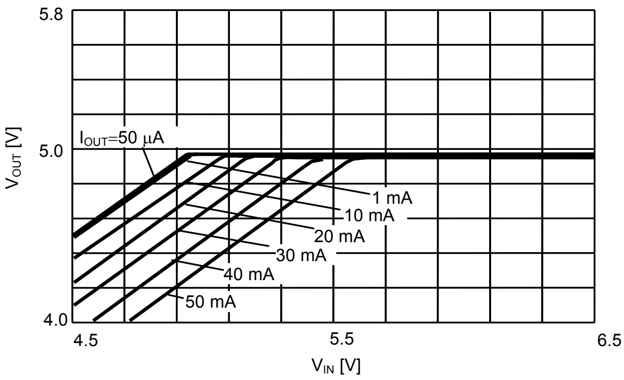


S-8730xxx Series

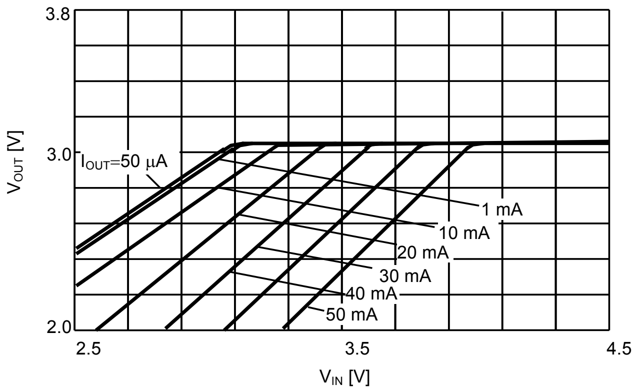


(3) Input voltage (V_{IN}) - Output voltage (V_{OUT}) characteristics

S-8750xxx Series

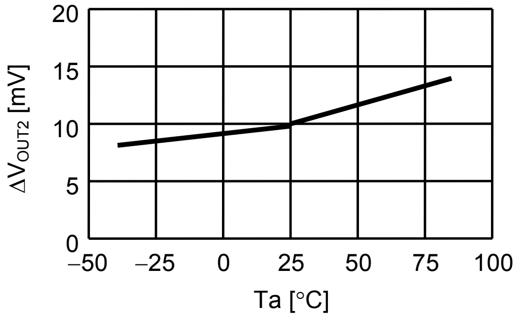


S-8730xxx Series

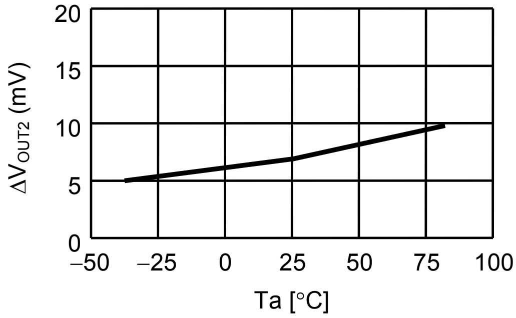


(4) Load regulation(ΔV_{OUT2}) - Temperature (Ta) characteristics

S-8750xxx Series

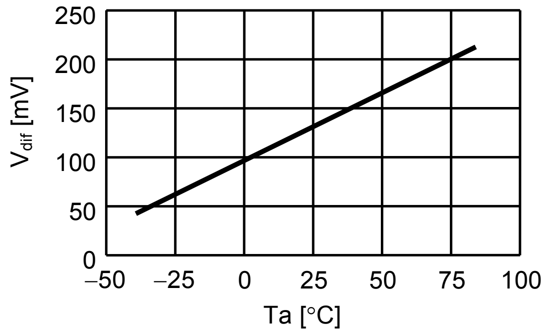


S-8730xxx Series

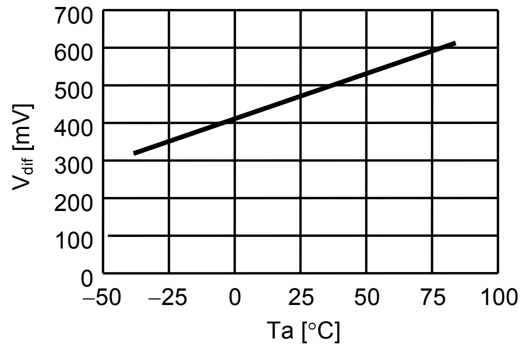


(5) I/O voltage difference (V_{dif}) - Temperature (Ta) characteristics

S-8750xxx Series

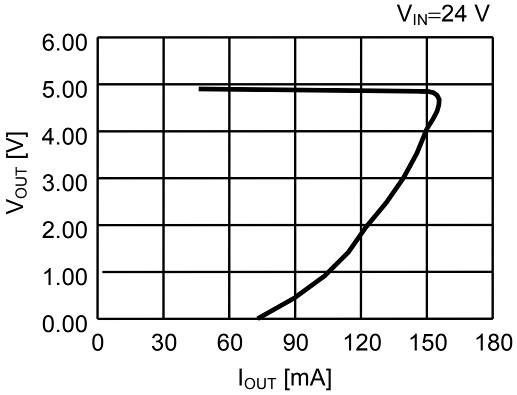


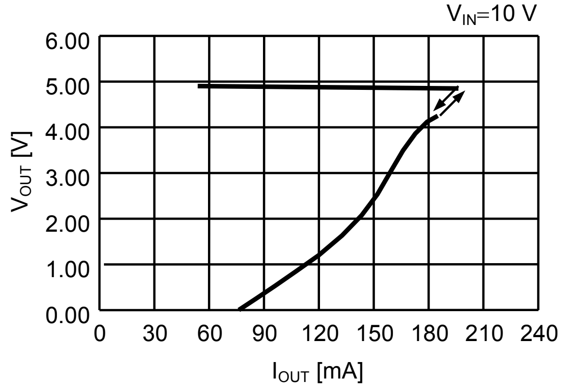
S-8730xxx Series

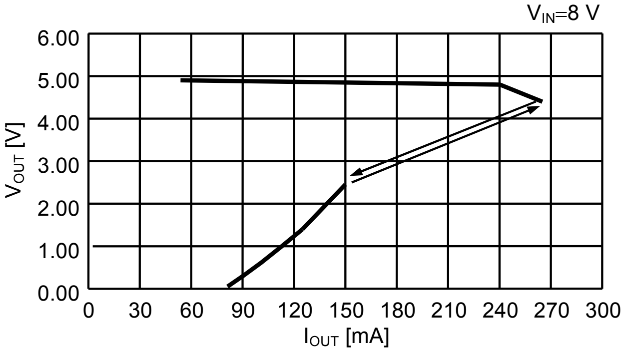


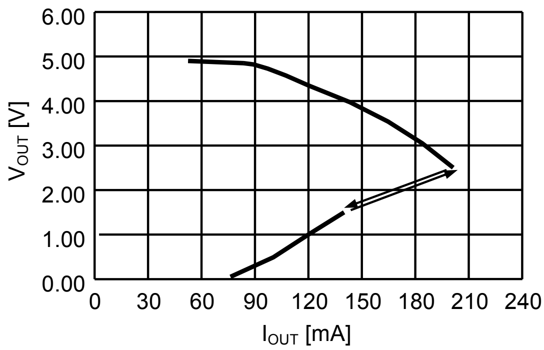
(6) Short-circuit protection circuit characteristics

S-8750xxx Series (Ta=25°C)

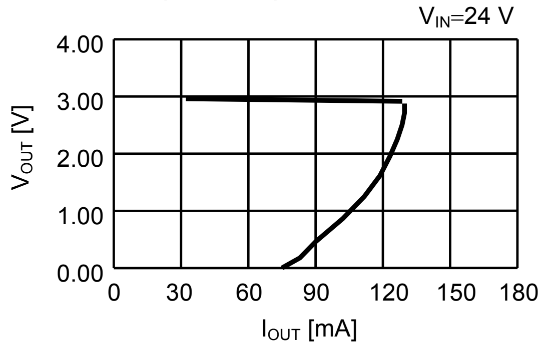




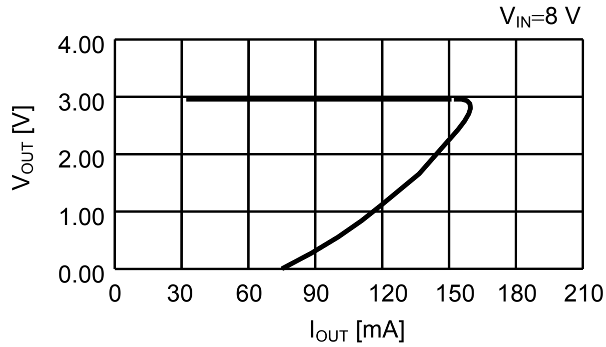


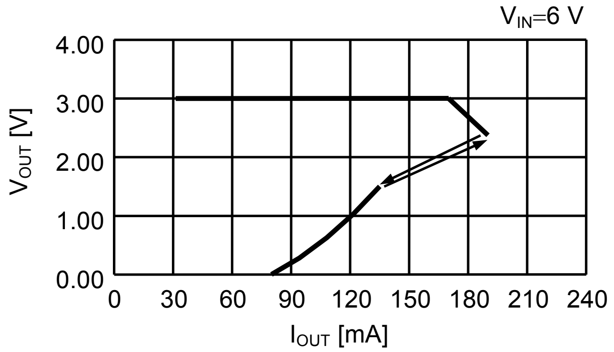


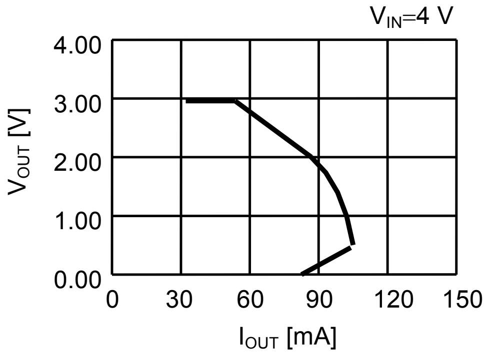
S-8730xxx Series (Ta=25°C)



S-8730xxx Series

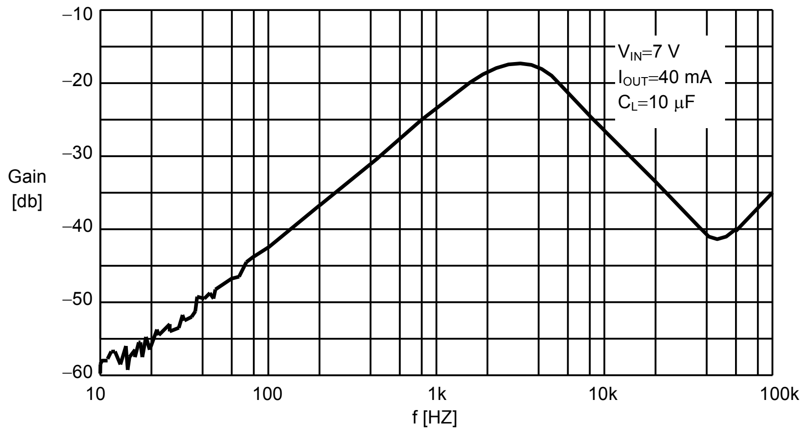




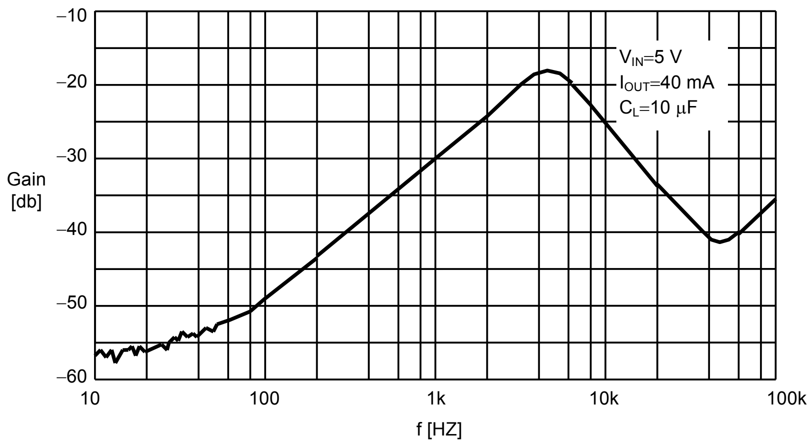


(7) Ripple rejection characteristics

S-8750xxx Series



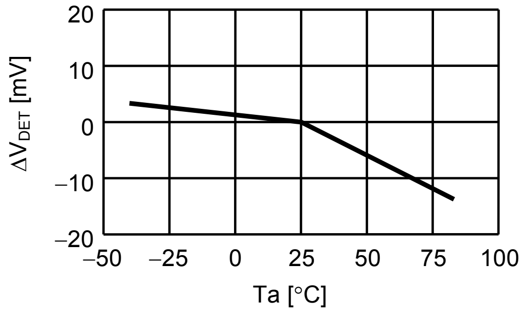
S-8730xxx Series



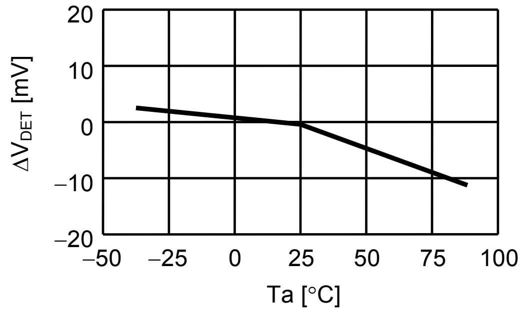
2. Voltage detector

(1) Detection voltage (V_{DET}) - Temperature (Ta) characteristics

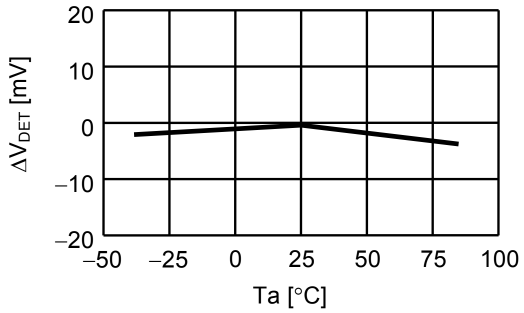
S-875045



S-875043

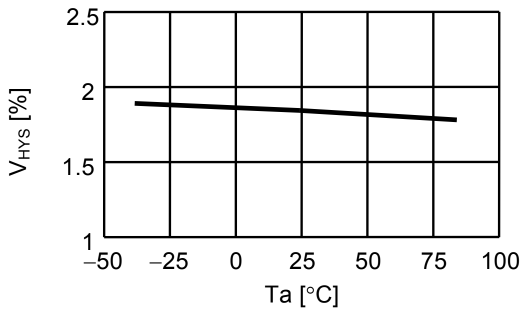


S-873023

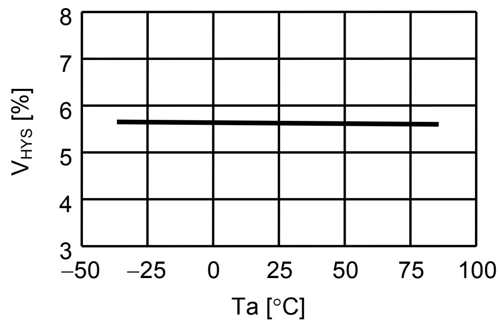


(2) Hysteresis width (V_{HYS}) - Temperature (Ta) characteristics

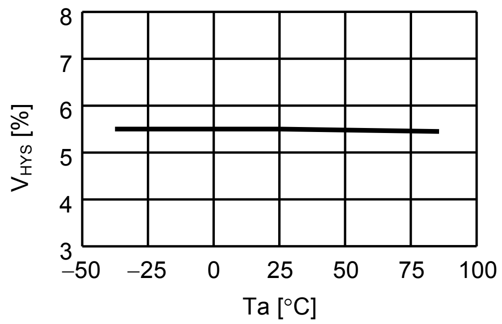
S-875045



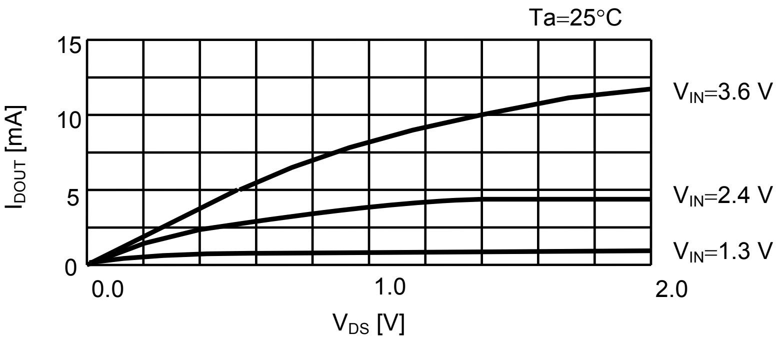
S-875043



S-873023

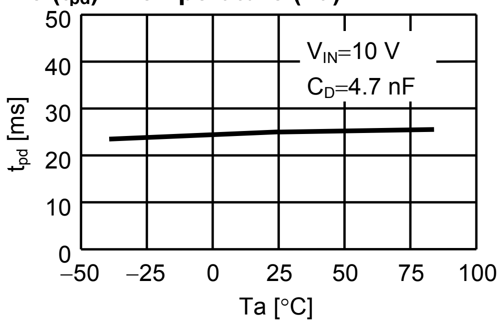


(3) Nch transistor output current (I_{DOUT}) characteristics



(4) Delay time (t_{pd}) characteristics

Delay time (t_{pd}) - Temperature (Ta)

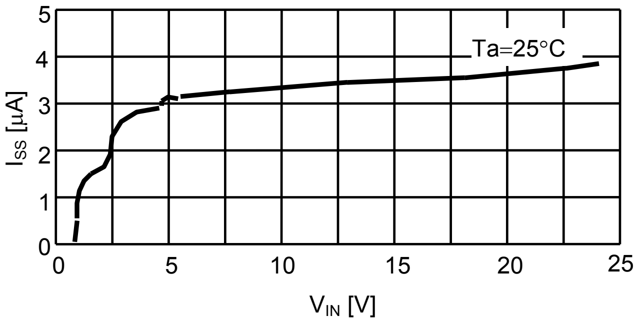


3. Total

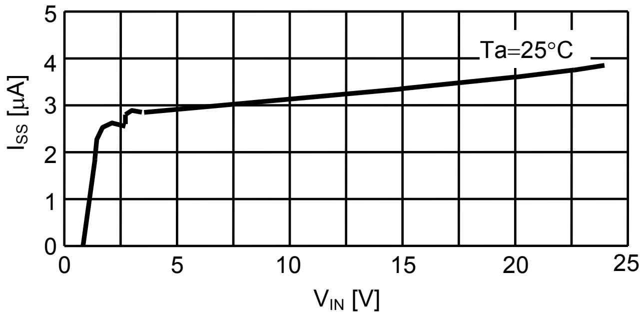
(1) Current consumption (Iss) characteristics

(a) Input voltage(V_{IN}) characteristics

S-8750xxC Series

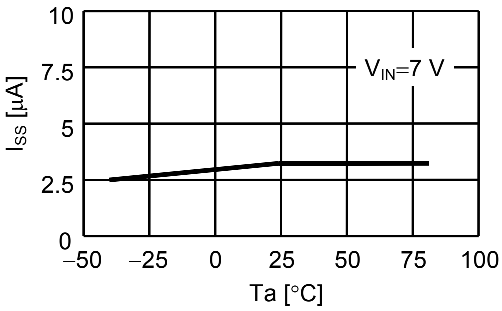


S-8730xxC Series

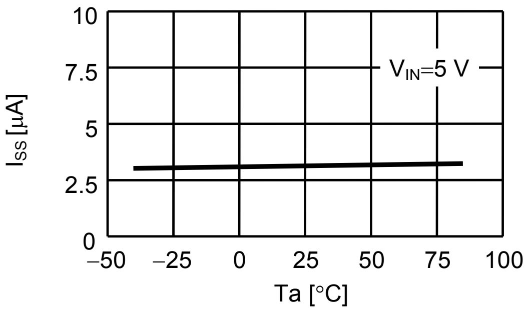


(b) Current consumption (Iss) - Temperature (Ta) characteristics

S-8750xxC Series

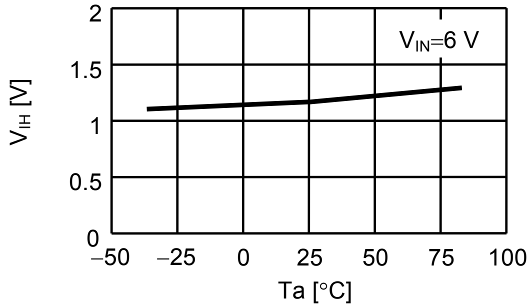


S-8730xxC Series

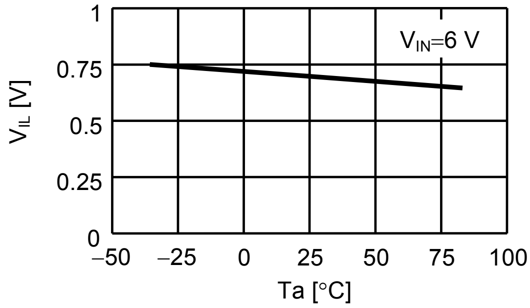


(2) Input voltage of shutdown circuit characteristics

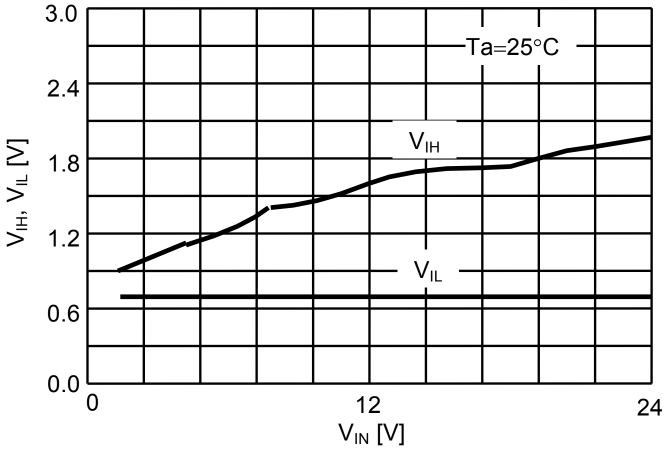
(a) High level input voltage (V_{IH}) - Temperature (Ta) characteristics

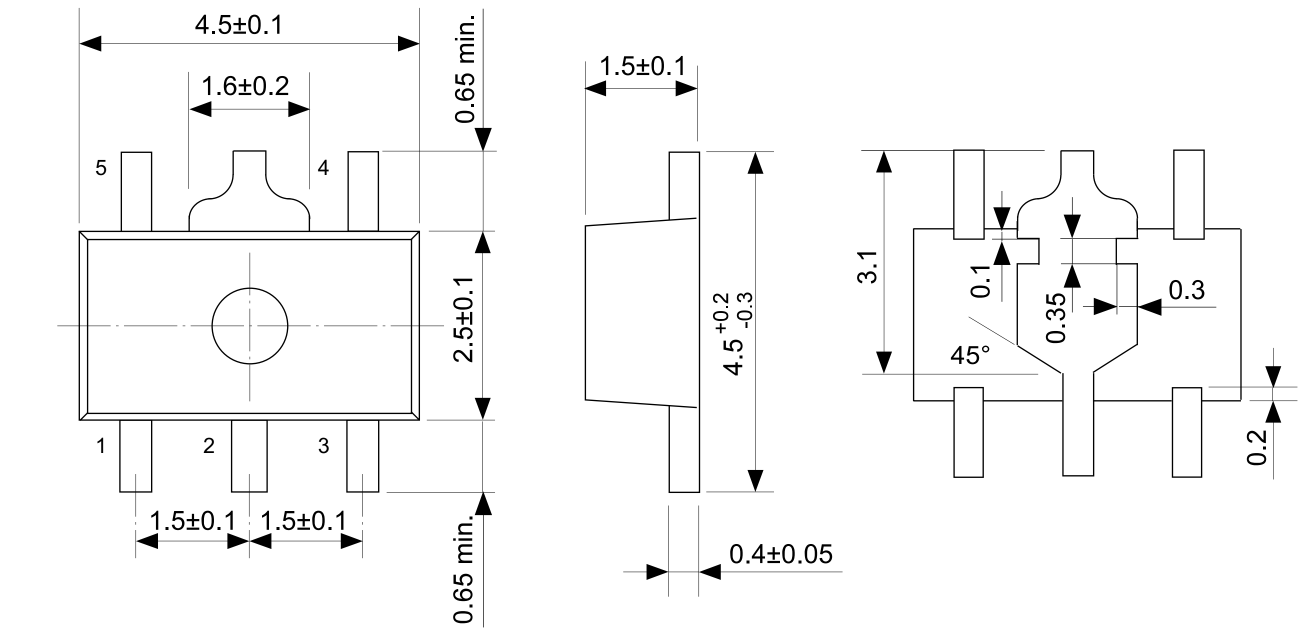


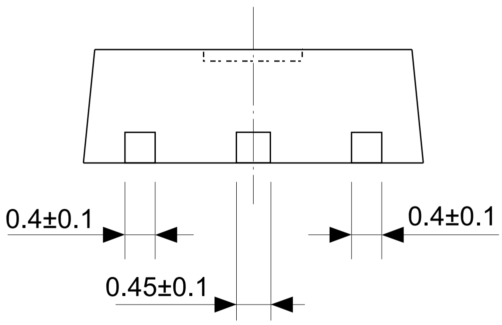
(b) Low level input voltage (V_{IL}) - Temperature (Ta) characteristics



(c) V_{IH}, V_{IL} - Power supply voltage dependency characteristics



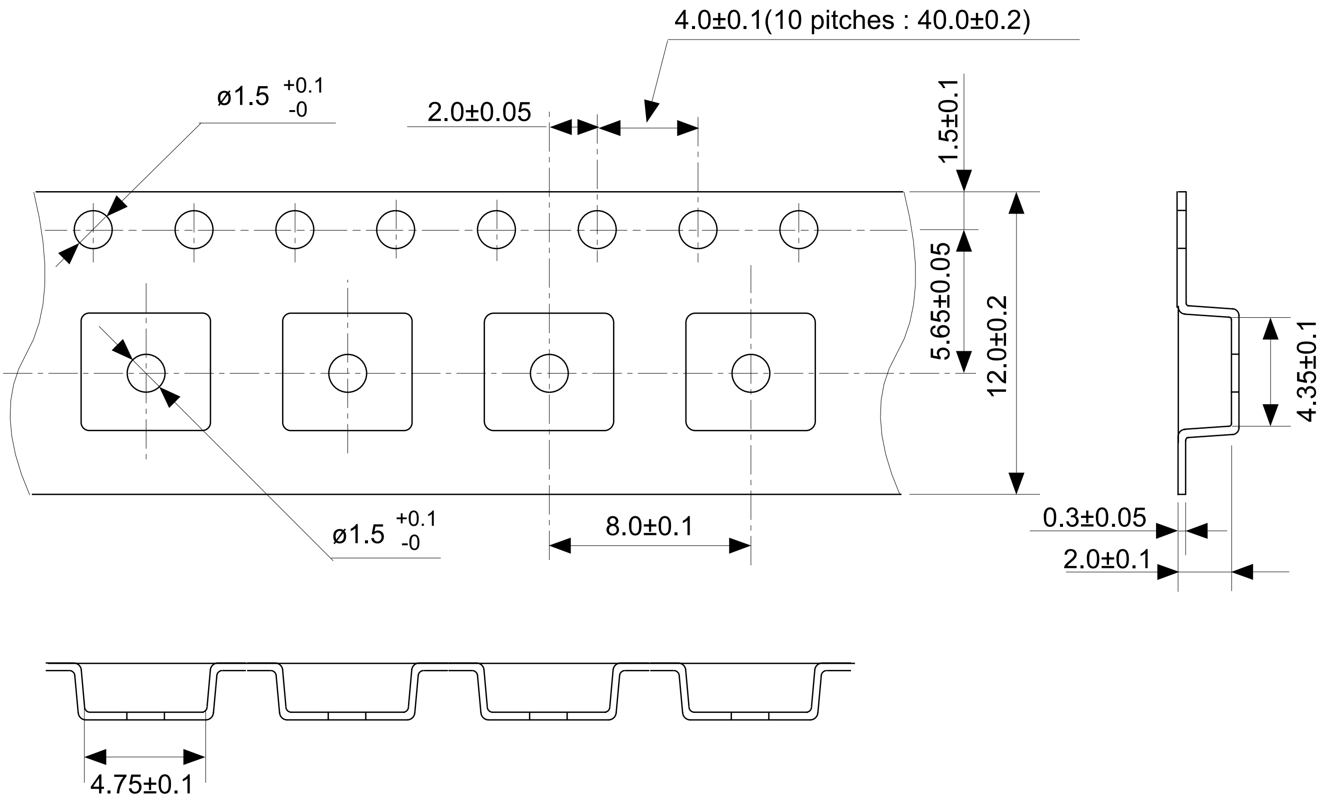


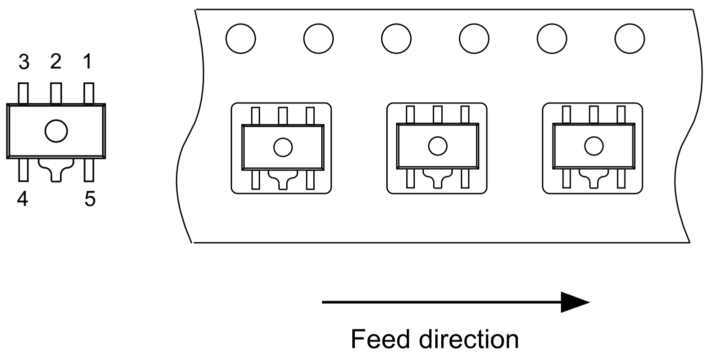


No. UP005-A-P-SD-2.0

TITLE	SOT895-A-PKG Dimensions
No.	UP005-A-P-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.

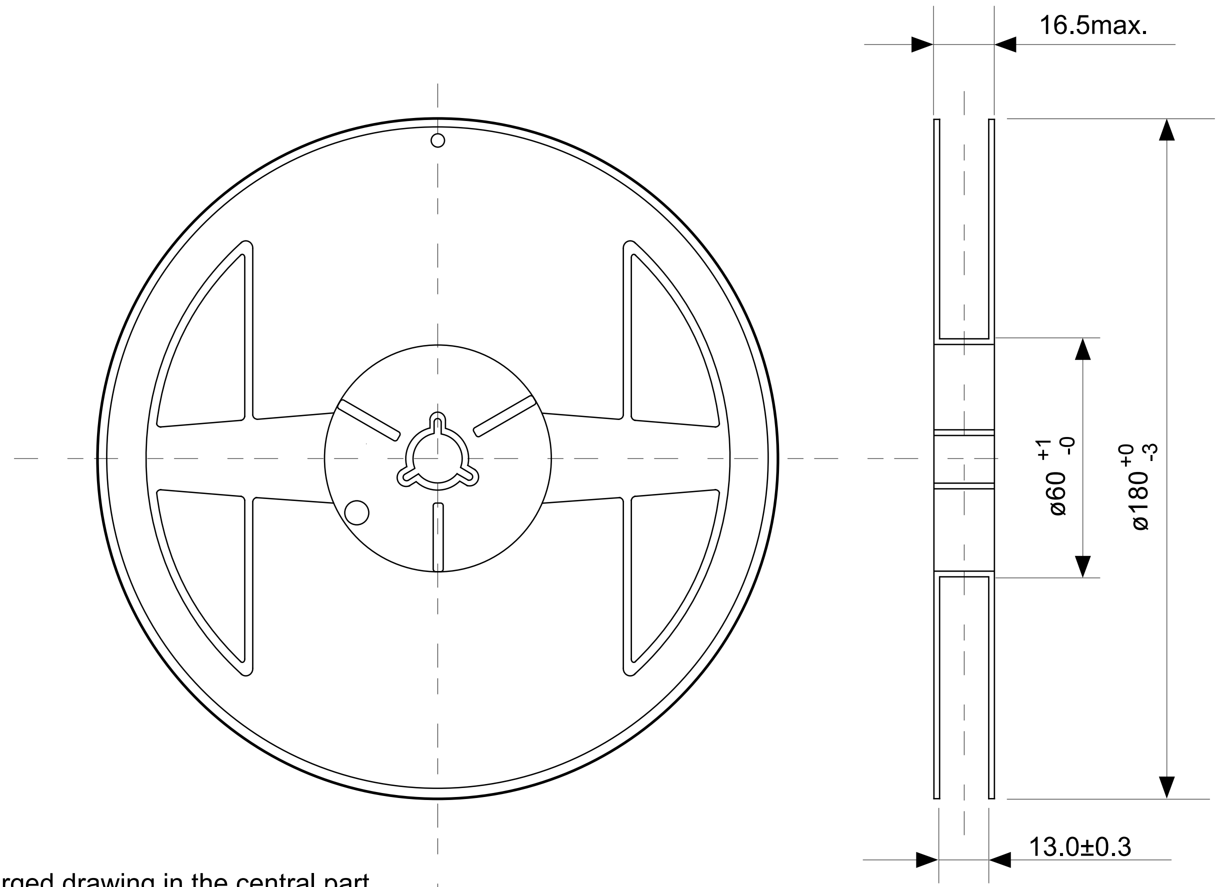




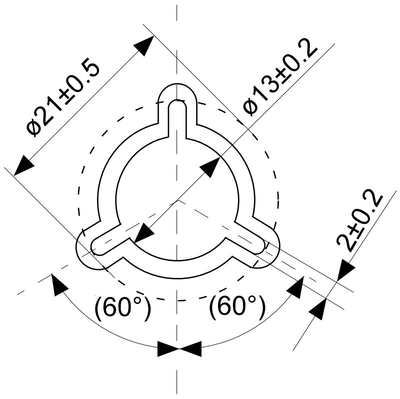
No. UP005-A-C-SD-2.0

TITLE	SOT895-A-Carrier Tape
No.	UP005-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



Enlarged drawing in the central part



No. UP005-A-R-SD-1.1

TITLE	SOT895-A-Reel		
No.	UP005-A-R-SD-1.1		
ANGLE		QTY.	1,000
UNIT	mm		

ABLIC Inc.

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07

ABLIC Inc.
www.ablic.com