## Pin Descriptions

| Pin Name | Type | Pin No | Description |
|---|---|---|---|
| SRC & SRC# | Input | 2, 3 | 0.7V Differential SRC input from PI6C410 clock synthesizer |
| OE_0 & OE_3 | Input | 8, 21 | 3.3V LVTTL input for enabling outputs, active high.<br>OE_0 for OUT0 / OUT0#<br>OE_3 for OUT3 / OUT3# |
| OE_INV | Input | 25 | 3.3V LVTTL input for inverting the OE, SRC_STOP# and PWRDWN# pins.<br>When 0 = same stage<br>When 1 = OE_0, OE_3, SRC_STOP#, PWRDWN# inverted. |
| OUT[0:3] & OUT[0:3]# | Output | 6, 7, 9, 10, 19, 20, 22, 23 | 0.7V Differential outputs |
| PLL/BYPASS# | Input | 12 | 3.3V LVTTL input for selecting fan-out of PLL operation. |
| SCLK | Input | 13 | SMBus compatible SCLOCK input |
| SDA | I/O | 14 | SMBus compatible SDATA |
| IREF | Input | 26 | External resistor connection to set the differential output current |
| SRC_STOP# | Input | 16 | 3.3V LVTTL input for SRC stop, active low |
| PLL_BW# | Input | 17 | 3.3V LVTTL input for selecting the PLL bandwidth |
| PWRDWN# | Input | 15 | 3.3V LVTTL input for Power Down operation, active low |
| $V_{DD}$ | Power | 1, 5, 11, 18, 24 | 3.3V Power Supply for Outputs |
| VSS | Ground | 4 | Ground for Outputs |
| VSS_A | Ground | 27 | Ground for PLL |
| VDD_A | Power | 28 | 3.3V Power Supply for PLL |

## Serial Data Interface (SMBus)

This part is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

## Address assignment

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | W/R |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0/1 |

## Data Protocol

| 1 bit | 7 bits | 1 | 1 | 8 bits | 1 | 8 bits | 1 | 8 bits | 1 | | 8 bits | 1 | 1 bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Start bit | Slave Addr | R/W | Ack | Register offset | Ack | Byte Count = N | Ack | Data Byte 0 | Ack | … | Data Byte N - 1 | Ack | Stop bit |

**Notes:**

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

## Data Byte 0: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|---|---|---|---|---|---|
| 0 | Outputs Mode<br>0 = Divide by 2<br>1 = Normal | RW | 1 = Normal | OUT[0:3], OUT[0:3]# | NA |
| 1 | PLL/BYPASS#<br>0 = Fanout<br>1 = PLL | RW | 1 = PLL | OUT[0:3], OUT[0:3]# | NA |
| 2 | PLL Bandwidth<br>0 = High Bandwidth,<br>1 = Low Bandwidth | RW | 1 = Low | OUT[0:3], OUT[0:3]# | NA |
| 3 | TBD | | | | NA |
| 4 | TBD | | | | NA |
| 5 | TBD | | | | NA |
| 6 | SRC_STOP#<br>0 = Driven when stopped<br>1 = Tristate | RW | 0 = Driven when stopped | OUT[0:3], OUT[0:3]# | |
| 7 | PWRDWN#<br>0 = Driven when stopped<br>1 = Tristate | RW | 0 = Driven when stopped | OUT[0:3], OUT[0:3]# | NA |

## Data Byte 1: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|---|---|---|---|---|---|
| 0 | | | | | |
| 1 | OUTPUTS enable<br>1 = Enabled<br>0 = Disabled | RW | 1 = Enabled | OUT0, OUT0# | NA |
| 2 | | RW | 1 = Enabled | OUT1, OUT1# | NA |
| 3 | | | | | |
| 4 | | | | | |
| 5 | OUTPUTS enable<br>1 = Enabled<br>0 = Disabled | RW | 1 = Enabled | OUT2, OUT2# | NA |
| 6 | | RW | 1 = Enabled | OUT3, OUT3# | NA |
| 7 | | | | | |

## Data Byte 2: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|---|---|---|---|---|---|
| 0 | | | | | |
| 1 | Allow control of OUTPUTS with assertion of SRC_STOP#<br>0 = Free running<br>1 = Stopped with SRC_Stop# | RW | 0 = Free running | OUT0, OUT0# | NA |
| 2 | | RW | 0 = Free running | OUT1, OUT1# | NA |
| 3 | | | | | |
| 4 | | | | | |
| 5 | Allow control of OUTPUTS with assertion of SRC_STOP#<br>0 = Free running<br>1 = Stopped with SRC_Stop# | RW | 0 = Free running | OUT2, OUT2# | NA |
| 6 | | RW | 0 = Free running | OUT3, OUT3# | NA |
| 7 | | | | | |

## Data Byte 3: Control Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Source Pin |
|---|---|---|---|---|---|
| 0 | TBD | RW | | | |
| 1 | | RW | | | |
| 2 | | RW | | | |
| 3 | | RW | | | |
| 4 | | RW | | | |
| 5 | | RW | | | |
| 6 | | RW | | | |
| 7 | | RW | | | |

## Data Byte 4: Pericom ID Register

| Bit | Descriptions | Type | Power Up Condition | Output(s) Affected | Pin |
|---|---|---|---|---|---|
| 0 | Pericom ID | R | 0 | NA | NA |
| 1 | | R | 0 | NA | NA |
| 2 | | R | 0 | NA | NA |
| 3 | | R | 0 | NA | NA |
| 4 | | R | 0 | NA | NA |
| 5 | | R | 1 | NA | NA |
| 6 | | R | 0 | NA | NA |
| 7 | | R | 0 | NA | NA |

## Functionality

| PWRDWN# | OUT | OUT# | SRC_Stop# | OUT | OUT# |
|---|---|---|---|---|---|
| 1 | Normal | Normal | 1 | Normal | Normal |
| 0 | $I_{REF} \times 2$ or Float | Low | 0 | $I_{REF} \times 6$ or Float | Low |

## Power Down (PWRDWN# assertion)

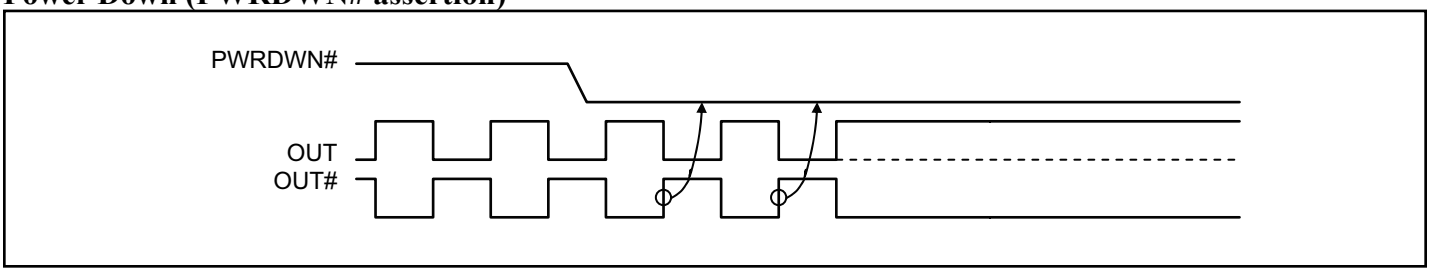



**Figure 1. Power down sequence**

## Power Down (PWRDWN# De-assertion)

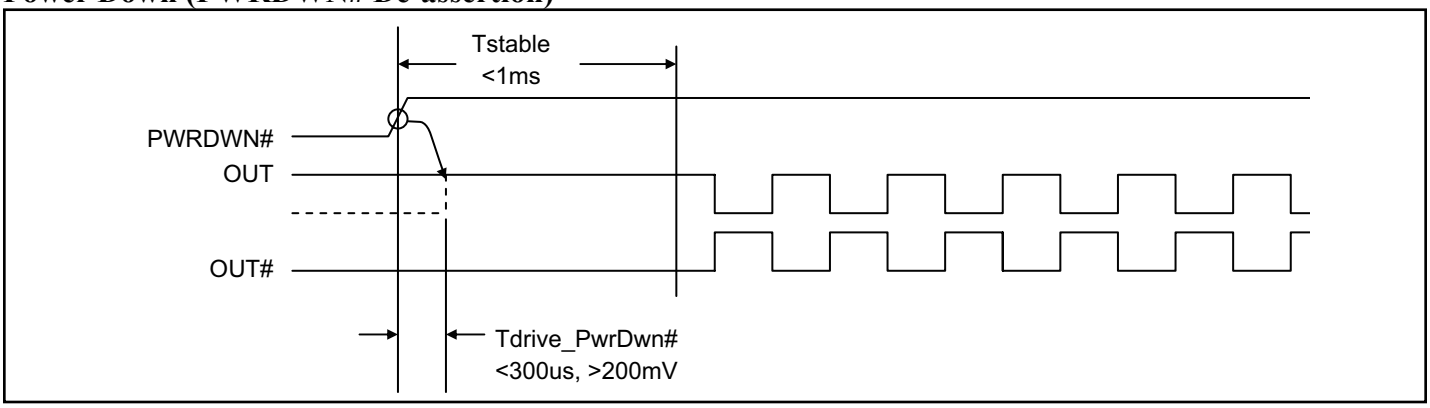



**Figure 2. Power down de-assert sequence**

## Current-mode output buffer characteristics of OUT[0:3], OUT[0:3]#

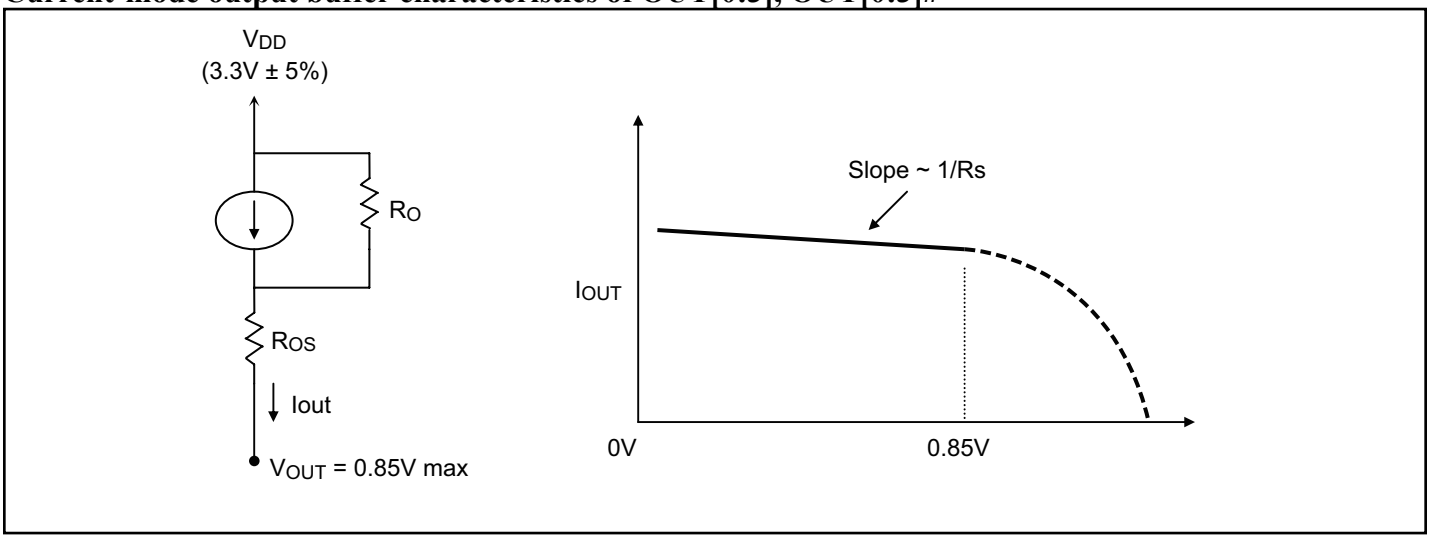



**Figure 9. Simplified diagram of current-mode output buffer**

## Differential Clock Buffer characteristics

| Symbol | Minimum | Maximum |
|---|---|---|
| $R_O$ | 3000Ω | N/A |
| $R_{OS}$ | unspecified | unspecified |
| $V_{OUT}$ | N/A | 850mV |

## Current Accuracy

| Symbol | Conditions | Configuration | Load | Min. | Max. |
|---|---|---|---|---|---|
| $I_{OUT}$ | $V_{DD}$ = 3.30 ±5% | $R_{REF}$ = 475Ω 1%<br>$I_{REF}$ = 2.32mA | Nominal test load for given configuration | -12%<br>$I_{NOMINAL}$ | +12%<br>$I_{NOMINAL}$ |

**Note:**
1. $I_{NOMINAL}$ refers to the expected current based on the configuration of the device.

## Differential Clock Output Current

| Board Target Trace/Term Z | Reference R, Iref = $V_{DD}$/(3xRr) | Output Current | $V_{OH}$ @ Z |
|---|---|---|---|
| 100Ω<br>(100Ω differential ≈ 15% coupling ratio) | $R_{REF}$ = 475Ω 1%,<br>$I_{REF}$ = 2.32mA | $I_{OH}$ = 6 x $I_{REF}$ | 0.7V @ 50 |

## Absolute Maximum Ratings (Over operating free-air temperature range)

| Symbol | Parameters | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{DD\_A}$ | 3.3V Core Supply Voltage | -0.5 | 4.6 | V |
| $V_{DD}$ | 3.3V I/O Supply Voltage | -0.5 | 4.6 | |
| $V_{IH}$ | Input High Voltage | | 4.6 | |
| $V_{IL}$ | Input Low Voltage | -0.5 | | |
| Ts | Storage Temperature | -65 | 150 | °C |
| $V_{ESD}$ | ESD Protection | 2000 | | V |

**Note:**
1. Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

## DC Electrical Characteristics ($V_{DD}$ = 3.3±5%, $V_{DD\_A}$ = 3.3±5%)

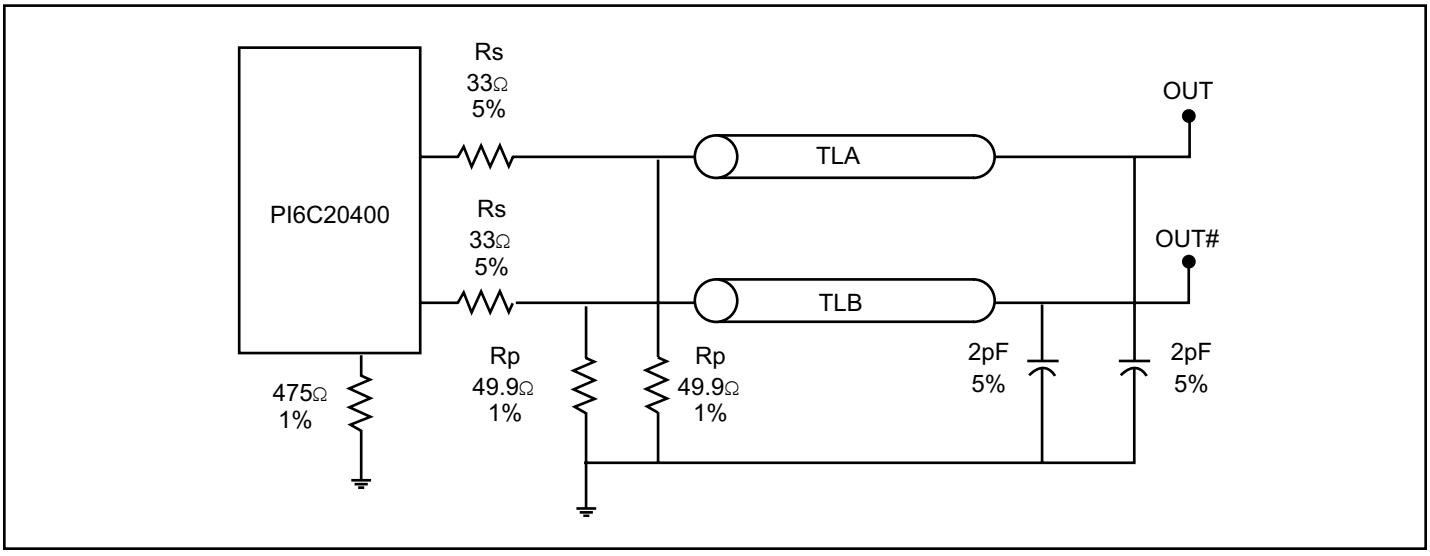
| Symbol | Parameters | Condition | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{DD\_A}$ | 3.3V Core Supply Voltage | | 3.135 | 3.465 | V |
| $V_{DD}$ | 3.3V I/O Supply Voltage | | 3.135 | 3.465 | |
| $V_{IH}$ | 3.3V Input High Voltage | $V_{DD}$ | 2.0 | $V_{DD}$ + 0.3 | |
| $V_{IL}$ | 3.3V Input Low Voltage | | $V_{SS}$ – 0.3 | 0.8 | |
| $I_{IK}$ | Input Leakage Current | 0 < $V_{IN}$ < $V_{DD}$ | -5 | +5 | µA |
| $V_{OH}$ | 3.3V Output High Voltage | $I_{OH}$ = -1mA | 2.4 | | V |
| $V_{OL}$ | 3.3V Output Low Voltage | $I_{OL}$ = 1mA | | 0.4 | |
| $I_{OH}$ | Output High Current | $I_{OH}$ = 6 x $I_{REF}$, $I_{REF}$ = 2.32mA | 12.2 | | mA |
| | | | | 15.6 | |
| $C_{IN}$ | Input Pin Capacitance | | 3 | 5 | pF |
| $C_{OUT}$ | Output Pin Capacitance | | | 6 | |
| $L_{PIN}$ | Pin Inductance | | | 7 | nH |
| $I_{DD}$ | Power Supply Current | $V_{DD}$ = 3.465V, $F_{CPU}$ = 200MHz | | 200 | mA |
| $I_{SS}$ | Power Down Current | Driven outputs | | 40 | |
| $I_{SS}$ | Power Down Current | Tristate outputs | | 12 | |
| $T_A$ | Ambient Temperature | | 0 | 70 | °C |

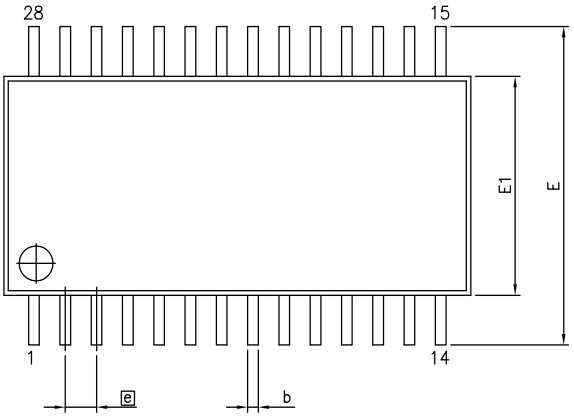
## AC Switching Characteristics ($V_{DD}$ = 3.3±5%, $V_{DD\_A}$ = 3.3±5%)

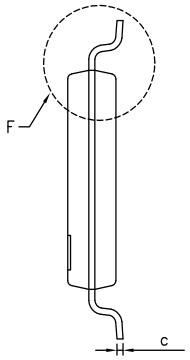
| Symbol | Parameters | Min | Max. | Units | Notes |
|---|---|---|---|---|---|
| $T_{rise}$ / $T_{fall}$ | Rise and Fall Time (measured between 0.175V to 0.525V) | 175 | 700 | ps | 2 |
| $\Delta T_{rise}$ / $\Delta T_{fall}$ | Rise and Fall Time Variation | | 125 | ps | 2 |
| | Rise/Fall Matching | | 20 | % | 2 |
| $T_{pd}$ | PLL Mode | | ±250 | ps | |
| | Non-PLL Mode | 2.5 | 6.5 | ns | |
| $T_{skew}$ | Output-to-Output Skew | | 50 | ps | 3 |
| $T_{jitter}$ | Cycle – Cycle Jitter | | 50 | ps | 3, 4 |
| $V_{HIGH}$ | Voltage High including overshoot | 660 | 1150 | mV | 2 |
| $V_{LOW}$ | Voltage Low including undershoot | -300 | | mV | 2 |
| $V_{cross}$ | Absolute crossing point voltages | 250 | 550 | mV | 2 |
| $\Delta V_{cross}$ | Total Variation of Vcross over all edges | | 140 | mV | 2 |
| $T_{DC}$ | Duty Cycle | 45 | 55 | % | 3 |

**Notes:**
1. Test configuration is $R_s$ = 33.2Ω, Rp = 49.9Ω, and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.
4. Measurement taken using M1 data capture analysis tool.

## Configuration Test Load Board Termination

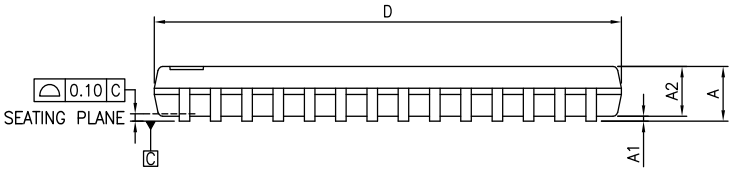


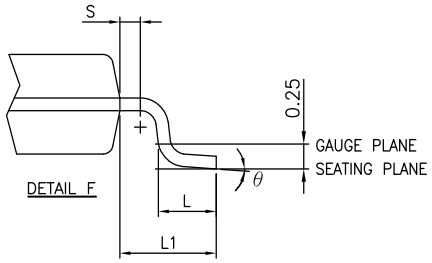



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | – | – | 1.20 |
| A1 | 0.05 | – | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | – | 0.30 |
| c | 0.09 | – | 0.20 |
| D | 9.60 | 9.70 | 9.80 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.40 BSC | | |
| e | 0.65 BSC | | |
| L1 | 1.00 REF | | |
| L | 0.45 | 0.60 | 0.75 |
| S | 0.20 | – | – |
| θ | 0° | – | 8° |




**Notes:**
1. Refer JEDEC: MO-153F/AE
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

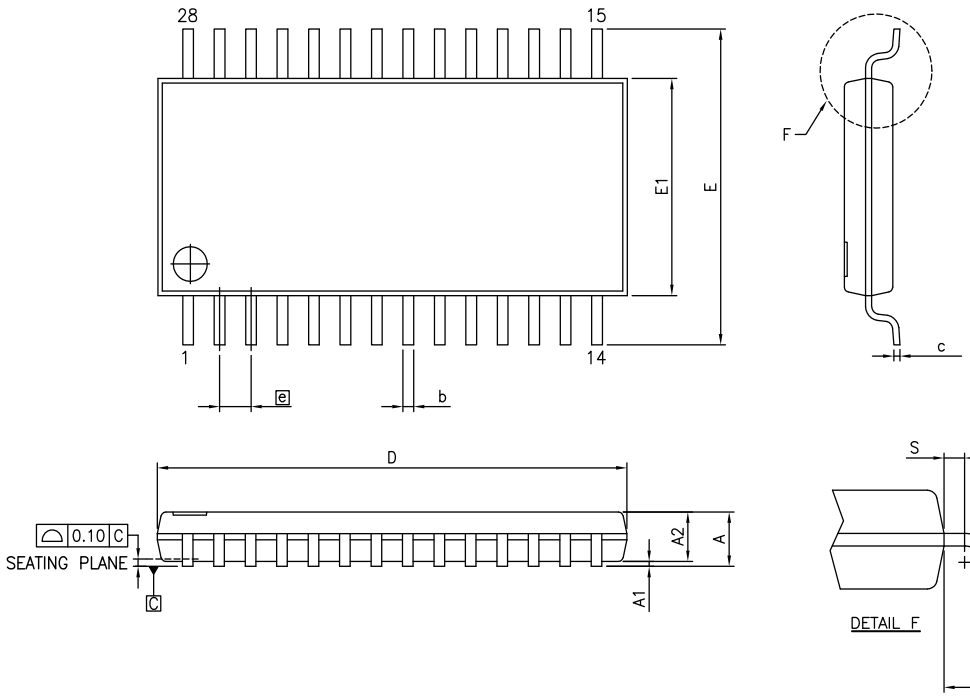
PERICOM Enabling Serial Connectivity

**DATE: 05/03/12**

**DESCRIPTION: 28 pin, 173mil wide, TSSOP**

**PACKAGE CODE: L**

**DOCUMENT CONTROL #: PD-1313** **REVISION: E**




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | – | – | 1.20 |
| A1 | 0.05 | – | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | – | 0.30 |
| c | 0.09 | – | 0.20 |
| D | 9.60 | 9.70 | 9.80 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | | 6.40 BSC | |
| e | | 0.65 BSC | |
| L1 | | 1.00 REF | |
| L | 0.45 | 0.60 | 0.75 |
| S | 0.20 | – | – |
| θ | 0° | – | 8° |

**Notes:**
1. Refer JEDEC: MO-153F/AE
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity

**DATE: 05/03/12**

**DESCRIPTION: 28 pin, 173mil wide, TSSOP**

**PACKAGE CODE: L**

**DOCUMENT CONTROL #: PD-1313** **REVISION: E**

## Ordering Information(1-3)

| Ordering Code | Package Code | Package Description |
|---|---|---|
| PI6C20400HE | HE | 28-pin, 209-mil wide, SSOP, Pb-Free and Green |
| PI6C20400LE | LE | 28-pin, 173-mil wide, TSSOP, Pb-Free and Green |

**Notes:**
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel