# 4. Ordering information

Type number	Package	Package							
	Name	Description	Version						
PCF2123TS	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1						
PCF2123BS	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body $3 \times 3 \times 0.85$ mm	SOT758-1						
PCF2123U	PCF2123U/10	wire bond die; 12 bonding pads; $1.492 \times 1.449 \times 0.20 \text{ mm}^{[1]}$	PCF2123U/10						

[1] Sawn wafer on Film Frame Carrier (FFC); 200  $\mu$ m thickness.

# 5. Marking

Table 2.   Marking codes	
Type number	Marking code
PCF2123TS	PCF2123
PCF2123BS	123
PCF2123U	PC2123-1

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# 6. Block diagram



# 7. Pinning information

# 7.1 Pinning



Fig 4. Pinning diagram of PCF2123U (bare die)

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7.2	Pin	description
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. ...

Symbol	Pin			Description		
- <b>j</b>	TSSOP14	HVQFN16	PCF2123U/10			
OSCI	1	16	7	oscillator input; high-impedance node; minimize wire length between quartz and package		
OSCO	2	1	8	oscillator output; high-impedance node; minimize wire length between quartz and package		
n.c.	3, 11	6, 7, 14, 15	-	do not connect and do not use as feed through; connect to $V_{\text{DD}}$ if floating pins are not allowed		
TEST	4	2	9	test pin; not user accessible; connect to $V_{\mbox{SS}}$ or leave floating (internally pulled down)		
INT	5	3	10	interrupt output (open-drain; active LOW)		
CE	6	4	11	chip enable input (active HIGH) with internal pull down		
V <sub>SS</sub>	7	5 <mark>[1]</mark>	12 <mark>[2]</mark>	ground		
SDO	8	8	1	serial data output, push-pull; high-impedance when not driving; can be connected to SDI for single wire data line		
SDI	9	9	2	serial data input; may float when CE is inactive		
SCL	10	10	3	serial clock input; may float when CE is inactive		
CLKOE	12	11	4	CLKOUT enable or disable pin; enable is active HIGH		
CLKOUT	13	12	5	clock output (open-drain)		
V <sub>DD</sub>	14	13	6	supply voltage; positive or negative steps in $V_{DD}$ may affect oscillator performance; recommend 10 nF decoupling close to device (see Figure 28)		

[1] The die paddle (exposed pad) is wired to V<sub>SS</sub> but should not be electrically connected.

[2] The substrate (rear side of the die) is wired to  $V_{SS}$  but should not be electrically connected.

# 8. Device protection diagram



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# 9. Functional description

The PCF2123 contains sixteen 8-bit registers with an auto-incrementing address counter, an on-chip 32.768 kHz oscillator with two integrated load capacitors, a frequency divider which provides the source clock for the Real Time Clock (RTC), a programmable clock output, and a 6.25 Mbit/s SPI-bus. An offset register allows fine tuning of the clock.

All sixteen registers are designed as addressable 8-bit parallel registers although not all bits are implemented.

- The first two registers (memory address 00h and 01h) are used as control registers.
- The memory addresses 02h through 08h are used as counters for the clock function (seconds up to years). The Seconds, Minutes, Hours, Days, Weekdays, Months and Years registers are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock and calendar during a carry condition is prevented.
- Addresses 09h through 0Ch define the alarm condition.
- Address 0Dh defines the offset calibration.
- Address 0Eh defines the clock out and timer mode.
- Address registers 0Eh and 0Fh are used for the countdown timer function. The countdown timer has four selectable source clocks allowing for countdown periods in the range from 244 µs up to four hours. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. These are defined in register Control\_2 (01h).

## 9.1 Low power operation

Minimum power operation will be achieved by reducing the number and frequency of switching signals inside the IC, i.e. low frequency timer clocks and a low frequency CLKOUT will result in lower operating power. A second prime consideration is the series resistance  $R_s$  of the quartz used.

## 9.1.1 Power consumption with respect to quartz series resistance

The series resistance acts as a loss element. Low  $\mathsf{R}_{\mathsf{s}}$  will reduce current consumption further.



### 9.1.2 Power consumptions with respect to timer mode

Four source clocks are possible for the timer. The 4.096 kHz source clock will add the greatest part to the power consumption. The selection of 64 Hz, 1 Hz or  $\frac{1}{60}$  Hz will be almost indistinguishable and add very little.



## 9.2 Register overview

16 registers are available. The time registers are encoded in the binary coded decimal format (BCD) to simplify application use. Other registers are either bit-wise or standard binary.

#### Table 4. Registers overview

Bit positions labelled as - are not implemented and will return a 0 when read. Bit positions labelled with 0 should always be written with logic 0<sup>[1]</sup>.

Address	Register name	Bit								
		7	6	5	4	3	2	1	0	
00h	Control_1	EXT_TEST	0	STOP	SR	0	12_24	CIE	0	
01h	Control_2	MI	SI	MSF	TI_TP	AF	TF	AIE	TIE	
02h	Seconds	OS	SECOND	S (0 to 59)						
03h	Minutes	-	MINUTES	(0 to 59)						
04h Ho	Hours	-	-	AMPM	HOURS (1	l to 12) in 1	2 h mode			
				HOURS (0 to 23) in 24 h mode						
05h	Days	-	-	DAYS (1 to 31)						
06h	Weekdays	-	-	-	-	-	WEEKDA	/S		
07h	Months	-	-	-	MONTHS	(1 to 12)				
08h	Years	YEARS (0 to 99	9)							
09h	Minute_alarm	AEN_M	MINUTE_	ALARM (0	to 59)					
0Ah	Hour_alarm	AEN_H	-	AMPM HOUR_ALARM (1 to 12) in 12 h mode						
				HOUR_ALARM (0 to 23) in 24 h mode						
0Bh	Day_alarm	AEN_D	-	DAY_ALA	RM (1 to 31	)				
0Ch	Weekday_alarm	AEN_W	-	-	-	-	WEEKDAY	′_ALARM		
0Dh	Offset_register	MODE	OFFSET							
0Eh	Timer_clkout	-	COF2	COF1	COF0	TE	-	CTD1	CTD0	
0Fh	Countdown_timer	COUNTDOWN	TIMER							

[1] Except in the case of software reset, see Section 9.5

# 9.3 Control registers

# 9.3.1 Register Control\_1

Table 5.         Register Control_1 (address 00h) bits description				
Bit	Symbol	Value	Description	Reference
7	EXT_TEST	0	normal mode	Section 9.12
		1	external clock test mode	
6	-	-	unused	-
5	STOP	0	the RTC source clock runs	Section 9.13
		1	the RTC clock is stopped;	
		RTC divider chain flip-flops are asynchronously set to logic 0;		
			CLKOUT at 32.768 kHz, 16.384 kHz or 8.192 kHz is still available	
4	SR	0	no software reset	Section 9.5
		1	initiate software reset <sup>[1]</sup> ;	
			this register will always return a 0 when read	
3	-	-	unused	-
2	12_24	0	24 hour mode is selected	-
		1	12 hour mode is selected	
1	CIE	0	no correction interrupt generated	Section 9.11
		1	interrupt pulses will be generated at every correction cycle	
0	-	-	unused	-

[1] To prevent an accidental software reset, 01011000 (58h) must be sent to register Control\_1 (see Section 9.5).

Table 6.         Register Control_2 (address 01h) bits description						
Bit	Symbol	Value	Description	Reference		
7	MI	0	minute interrupt is disabled	Section 9.8.1		
		1	minute interrupt is enabled			
6	SI	0	second interrupt is disabled			
		1	second interrupt is enabled			
5	MSF	0	no minute or second interrupt generated			
		1	flag set when minute or second interrupt generated;			
			flag must be cleared to clear interrupt when TI_IP = 0			
4	TI_TP	0	interrupt pin follows timer flags	Section 9.9.2		
		1	interrupt pin generates a pulse			
3	AF	0	no alarm interrupt generated	Section 9.7.1		
		1	flag set when alarm triggered;			
			flag must be cleared to clear interrupt			
2	TF	0	no countdown timer interrupt generated	-		
		1	flag set when countdown timer interrupt generated;			
			flag must be cleared to clear interrupt when TI_IP = 0			
1	AIE	0	no interrupt generated from the alarm flag	Section 9.9.3		
		1	interrupt generated when alarm flag set			
0	TIE	0	no interrupt generated from the countdown timer	Section 9.9.2		
		1	interrupt generated by the countdown timer			

## 9.3.2 Register Control\_2

# 9.4 OS flag

The PCF2123 includes a flag (bit OS) which is set whenever the oscillator is stopped (see Figure 8 and Figure 9). The flag will remain set until cleared by software. If the flag cannot be cleared, then the PCF2123 oscillator is not running. This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to the point where oscillation fails.



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The oscillator may be stopped, for example, by grounding one of the oscillator pins, OSCI or OSCO. The oscillator is also considered to be stopped during the time between power-on and stable crystal resonance. This time may be in the range of 200 ms to 2 s depending on crystal type, temperature and supply voltage. At power-on the OS flag is always set.

## 9.5 Reset

A reset is automatically generated at power-on. A reset can also be initiated with the software reset command. It is generally recommended to make a software reset after power-on.

A software reset can be initiated by setting the bits 6, 4 and 3 in register Control\_1 to logic 1 and all other bits to logic 0 by sending the bit sequence 01011000 (58h), see Figure 10. If this bit sequence is not correct, the software reset instruction will be ignored to protect the device from accidently being reset. When sending the software instruction, the other bits are not written.



The SPI-bus is reset whenever the chip enable pin CE is inactive.

#### Table 7. Register reset values

Bits labeled as - are not implemented. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit									
		7	6	5	4	3	2	1	0		
00h	Control_1	0	0	0	0	0	0	0	0		
01h	Control_2	0	0	0	0	0	0	0	0		
02h	Seconds	1	Х	Х	Х	Х	Х	Х	Х		
03h	Minutes	1	Х	Х	Х	Х	Х	Х	Х		
04h	Hours	-	-	Х	Х	Х	Х	Х	Х		
05h	Days	-	-	Х	Х	Х	Х	Х	Х		
06h	Weekdays	-	-	-	-	-	Х	Х	Х		
07h	Months	-	-	-	Х	Х	Х	Х	Х		
08h	Years	Х	Х	Х	Х	Х	Х	Х	Х		
09h	Minute_alarm	1	Х	Х	Х	Х	Х	Х	Х		
0Ah	Hour_alarm	1	-	Х	Х	Х	Х	Х	Х		
0Bh	Day_alarm	1	-	Х	Х	Х	Х	Х	Х		
0Ch	Weekday_alarm	1	-	-	-	-	Х	Х	Х		
0Dh	Offset_register	0	0	0	0	0	0	0	0		
0Eh	Timer_clkout	-	0	0	0	0	-	1	1		
0Fh	Countdown_timer	Х	Х	Х	Х	Х	Х	Х	Х		

After reset, the following mode is entered:

- 32.768 kHz on pin CLKOUT active
- 24 hour mode is selected
- Offset register is set to 0
- No alarms set
- Timer disabled
- No interrupts enabled

## 9.6 Time and date function

The majority of the registers are coded in the Binary Coded Decimal (BCD) format. BCD is used to simplify application use. An example is shown for the Minutes register in Table 8.

#### Table 8. BCD example

Minutes value	Upper-di	git			Digit			
(decimal)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
09	0	0	0	0	1	0	0	1
10	0	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:	:
58	0	1	0	1	1	0	0	0
59	0	1	0	1	1	0	0	1

### Table 9. Register Seconds (address 02h) bits description

Bit	Symbol	Value	Description
7	OS	0	clock integrity is guaranteed
		1	clock integrity is not guaranteed; oscillator has stopped or been interrupted
6 to 0	SECONDS	00 to 59[1]	this register holds the current seconds coded in BCD format

[1] Values shown in decimal.

#### Table 10. Register Minutes (address 03h) bits description

Bit	Symbol	Value	Description
7	-	-	unused
6 to 0	MINUTES	00 to 59[1]	this register holds the current minutes coded in BCD format

Bit	Symbol	Value	Description
7 and 6	-	-	unused
12 hour	mode <sup>[2]</sup>		
5 AMPM		0	indicates AM
		1	indicates PM
4 to 0	HOURS	01 to 12[1]	this register holds the current hours coded in BCD format for 12 hour mode
24 hour	mode <sup>[2]</sup>		
5 to 0	HOURS	00 to 23[1]	this register holds the current hours coded in BCD format for 24 hour mode

#### Table 11. Register Hours (address 04h) bits description

[1] Values shown in decimal.

[2] Hour mode is set by the 12\_24 bit in register Control\_1.

#### Table 12. Register Days (address 05h) bits description

Bit	Symbol	Value	Description
7 and 6	-	-	unused
5 to 0	DAYS	01 to 31[1]	this register holds the current day coded in BCD format <sup>[2]</sup>

[1] Values shown in decimal.

[2] The RTC compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

#### Table 13. Register Weekdays (address 06h) bits description

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0 <sup>[1]</sup>	WEEKDAYS	0 to 6 <sup>[2]</sup>	this register holds the current weekday, see Table 14

[1] These bits may be re-assigned by the user.

[2] Values shown in decimal.

#### Table 14.Weekday assignments

Day <sup>[1]</sup>	Upper-digit				Digit			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sunday	Х	Х	Х	Х	Х	0	0	0
Monday	Х	Х	Х	Х	Х	0	0	1
Tuesday	Х	Х	Х	Х	Х	0	1	0
Wednesday	Х	Х	Х	Х	Х	0	1	1
Thursday	Х	Х	Х	Х	Х	1	0	0
Friday	Х	Х	Х	Х	Х	1	0	1
Saturday	Х	Х	Х	Х	Х	1	1	0

[1] The weekday assignments may be re-defined by the user.

	integrator month	0 (uuuu 000 )	
Bit	Symbol	Value	Description
7 to 5	-	-	unused
4 to 0	MONTHS	01 to 12 <sup>[1]</sup>	this register holds the current month coded in BCD format, see Table 16

#### Table 15. Register Months (address 07h) bits description

[1] Values shown in decimal.

#### Table 16. Month assignments

	•							
Month	Upper-di	git			Digit			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	Х	Х	Х	0	0	0	0	1
February	Х	Х	Х	0	0	0	1	0
March	Х	Х	Х	0	0	0	1	1
April	Х	Х	Х	0	0	1	0	0
Мау	Х	Х	Х	0	0	1	0	1
June	Х	Х	Х	0	0	1	1	0
July	Х	Х	Х	0	0	1	1	1
August	Х	Х	Х	0	1	0	0	0
September	Х	Х	Х	0	1	0	0	1
October	Х	Х	Х	1	0	0	0	0
November	Х	Х	Х	1	0	0	0	1
December	Х	Х	Х	1	0	0	1	0

#### Table 17. Register Years (address 08h) bits description

Bit	Symbol	Value	Description
7 to 0	YEARS	00 to 99[1]	this register holds the current year coded in BCD format

#### 9.6.1 Data flow

Figure 11 shows the data flow and data dependencies starting from the 1 Hz clock tick.



In order to read the correct time it is important to read all time registers in one access i.e. seconds up to years. If the time registers are read by making individual access to the chip, then there is the risk that the time will increment between accesses.

## 9.7 Alarm function

When one or more of these registers are loaded with a valid minute, hour, day or weekday and its corresponding alarm enable not bit (AEN\_x) is logic 0, then that information will be compared with the current minute, hour, day and weekday.

	-		
Bit	Symbol	Value	Description
7 AEN	AEN_M	0	minute alarm is enabled
		1	minute alarm is disabled
6 to 0	MINUTE_ALARM	00 to 59[1]	this register holds the minute alarm information coded in BCD format

 Table 18.
 Register Minute\_alarm (address 09h) bits description

#### Table 19. Register Hour\_alarm (address 0Ah) bits description

Bit	Symbol	Value	Description
7	AEN_H	0	hour alarm is enabled
		1	hour alarm is disabled
6	-	-	unused
12 hour	mode		
5	AMPM	0	indicates AM
		1	indicates PM
4 to 0	HOUR_ALARM	01 to 12[1]	this register holds the hour alarm information coded in BCD format when in 12 hour mode
24 hour	mode		
5 to 0	HOUR_ALARM	00 to 23[1]	this register holds the hour alarm information coded in BCD format when in 24 hour mode

[1] Values shown in decimal.

#### Table 20. Register Day\_alarm (address 0Bh) bits description

Bit	Symbol	Value	Description
7	AEN_D	0	day alarm is enabled
		1	day alarm is disabled
6	-	-	unused
5 to 0	DAY_ALARM	01 to 31[1]	this register holds the day alarm information coded in BCD format

[1] Values shown in decimal.

#### Table 21. Register Weekday\_alarm (address 0Ch) bits description

	-		
Bit	Symbol	Value	Description
7	AEN_W	0	weekday alarm is enabled
		1	weekday alarm is disabled
3 to 6	-	-	unused
2 to 0	WEEKDAY_ ALARM	0 to 6[1]	this register holds the weekday alarm information



The generation of interrupts from the alarm function is described in Section 9.9.3.

#### 9.7.1 Alarm flag

When all enabled comparisons first match, the alarm flag bit AF is set. Bit AF will remain set until cleared by software. Once bit AF has been cleared it will only be set again when the time increments to match the alarm condition.

Alarm registers which have bit AEN\_x at logic 1 are ignored.

Table 23 shows an example for clearing bit AF but leaving bit MSF and bit TF unaffected. Clearing the flags is made by a write command; therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.



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To prevent the timer flags being overwritten while clearing AF, a logical AND is performed during a write access. Writing a logic 1 will cause the flag to maintain its value, whereas writing a logic 0 will cause the flag to be reset.

	Table 22.	Flag	location	in	register	Control	2
--	-----------	------	----------	----	----------	---------	---

Register	Bit								
	7	6	5	4	3	2	1	0	
Control_2	-	-	MSF	-	AF	TF	-	-	

The following tables show what instruction must be sent to clear bit AF. In this example, bit MSF and bit TF are unaffected.

Table 23. Example to clear only AF (bit 3) in register Control\_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	1	-	0	1	-	-

## 9.8 Timer functions

The countdown timer has four selectable source clocks allowing for countdown periods in the range from 244  $\mu$ s to 4 h 15 min. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. For periods greater than 4 hours, the alarm function can be used.

Registers 01h, 0Eh and 0Fh are used to control the timer function and output.

Table 24. Register Timer\_clkout (address 0Eh) bits description

Bit	Symbol	Value	Description	Reference
7	-	-	unused	-
6 to 4	COFx	<u>[1]</u>	CLKOUT control	Section 9.10
3	TE	0	countdown timer is disabled	Section 9.8.2
		1	countdown timer is enabled	
2	-	-	unused	
1 to 0	CTD	00	4.096 kHz countdown timer source clock	
		01	64 Hz countdown timer source clock	
		10	1 Hz countdown timer source clock	
		11	$1_{60}^{1}$ Hz countdown timer source clock	

[1] Values of COF[2:0] see <u>Table 35</u>.

#### Table 25. Register Countdown\_timer (address 0Ah) bits description

Bit	Symbol	Value	Description	Reference
7 to 0	COUNTDOWN_ TIMER	0h to FFh	countdown value = n; $CountdownPeriod = \frac{n}{SourceClockFrequent}$	Section 9.8.2

#### 9.8.1 Minute and second interrupt

The minute and second interrupts (bits MI and SI) are pre-defined timers for generating periodic interrupts. The timers can be enabled independently from one another. However, a minute interrupt enabled on top of a second interrupt will not be distinguishable since it will occur at the same time; see Figure 14.



#### Table 26. Effect of bits MI and SI on INT generation

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	no interrupt generated
1	0	an interrupt once per minute
0	1	an interrupt once per second
1	1	an interrupt once per second

The minute and second flag (bit MSF) is set to logic 1 when either the seconds or the minutes counter increments according to the currently enabled interrupt. The flag can be read and cleared by the interface. The status of bit MSF does not affect the INT pulse generation. If the MSF flag is not cleared prior to the next coming interrupt period, an INT pulse will still be generated.

The purpose of the flag is to allow the controlling system to interrogate the PCF2123 and identify the source of the interrupt i.e. minute or second, countdown timer or alarm.

#### Table 27. Effect of MI and SI on MSF

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	MSF never set
1	0	MSF set when <b>minutes</b> counter increments
0	1	MSF set when <b>seconds</b> counter increments
1	1	MSF set when <b>seconds</b> counter increments

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The duration of both of these timers will be affected by the register Offset\_register (see <u>Section 9.11</u>). Only when the Offset\_register has the value 00h will the periods be consistent.

#### 9.8.2 Countdown timer function

The 8-bit countdown timer at address 0Fh is controlled by the register Timer\_clkout at address 0Eh. The register Timer\_clkout selects one of 4 source clock frequencies for the timer (4.096 kHz, 64 Hz, 1 Hz, or  $\frac{1}{60}$  Hz) and enables or disables the timer.

# Table 28. Bits CTD0 and CTD1 for timer frequency selection and countdown timer durations

CTD[1:0]	Timer source clock	Delay					
	frequency <sup>[1]</sup>	Minimum timer duration n = 1	Maximum timer duration n = 255				
00	4.096 kHz	244 μs	62.256 ms				
01	64 Hz	15.625 ms	3.984 s				
10	1 Hz <sup>[2]</sup>	1 s	255 s				
11	<sup>1</sup> / <sub>60</sub> Hz <sup>[2]</sup>	60 s	4 h 15 min				

[1] When not in use, CTD must be set to  $\frac{1}{60}$  Hz for power saving.

[2] Time periods can be affected by correction pulses.

**Remark:** Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency will result in deviation in timings. This is not applicable to interface timing.

The timer counts down from a software-loaded 8-bit binary value, n. Loading the counter with 0 stops the timer. Values from 1 to 255 are valid. When the counter reaches 1, the countdown timer flag (bit TF) will be set and the counter automatically re-loads and starts the next timer period. Reading the timer will return the current value of the countdown counter (see Figure 15).



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If a new value of n is written before the end of the current timer period, then this value will take immediate effect. NXP does not recommend changing n without first disabling the counter (by setting bit TE = 0). The update of n is asynchronous to the timer clock, therefore changing it without setting bit TE = 0 may result in a corrupted value loaded into the countdown counter which results in an undetermined countdown period for the first period. The countdown value n will, however, be correctly stored and correctly loaded on subsequent timer periods.

When the countdown timer flag is set, an interrupt signal on INT will be generated provided that this mode is enabled. See <u>Section 9.9.2</u> for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period will have an uncertainty which is a result of the enable instruction being generated from the interface clock which is asynchronous from the timer source clock. Subsequent timer periods will have no such delay. The amount of delay for the first timer period will depend on the chosen source clock, see Table 29.

Timer source clock	Minimum timer period	Maximum timer period
4.096 kHz	n	n + 1
64 Hz	n	n + 1
1 Hz	(n – 1) + 1⁄ <sub>64</sub> Hz	n + <sup>1</sup> ⁄ <sub>64</sub> Hz
<sup>1</sup> / <sub>60</sub> Hz	(n – 1) + ½ <sub>64</sub> Hz	n + <sup>1</sup> ⁄ <sub>64</sub> Hz

#### Table 29. First period delay for timer counter value n

At the end of every countdown, the timer sets the countdown timer flag (bit TF). Bit TF may only be cleared by software. The asserted bit TF can be used to generate an interrupt (INT). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI\_TP is used to control this mode selection and the interrupt output may be disabled with bit TIE, see Table 6.

When reading the timer, the current countdown value is returned and **not** the initial value n. For accurate read back of the countdown value, the SPI-bus clock (SCL) must be operating at a frequency of at least twice the selected timer clock. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

Timer source clock frequency selection of 1 Hz and  $\frac{1}{60}$  Hz will be affected by the Offset\_register. The duration of a program period will vary according to when the offset is initiated. For example, if a 100 s timer is set using the 1 Hz clock as source, then some 100 s periods will contain correction pulses and therefor be longer or shorter depending on the setting of the Offset\_register. See Section 9.11 to understand the operation of the Offset\_register.

# 9.8.3 Timer flags

When a minute or second interrupt occurs, bit MSF is set to logic 1. Similarly, at the end of a timer countdown or alarm event, bit TF or AF are set to logic 1. These bits maintain their value until overwritten by software. If both countdown timer and minute or second interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another a logical AND is performed during a write access. Writing a logic 1 will cause the flag to maintain its value, whilst writing a logic 0 will cause the flag to be reset.

Three examples are given for clearing the flags. Clearing the flags is made by a write command, therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.

Table 30	). Flac	location	in	register	Control	2
		jiocation		register	0011101	_

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	MSF	-	AF	TF	-	-

<u>Table 31</u>, <u>Table 32</u> and <u>Table 33</u> show what instruction must be sent to clear the appropriate flag.

#### Table 31. Example to clear only TF (bit 2) in register Control\_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	1	-	1	0	-	-

#### Table 32. Example to clear only MSF (bit 5) in register Control\_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	0	-	1	1	-	-

Table 33. Example to clear both TF and MSF (bit 2 and bit 5) in register Control\_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	0	-	1	0	-	-

Clearing the alarm flag (bit AF) operates in exactly the same way, see Section 9.7.1.

## 9.9 Interrupt output

An active LOW interrupt signal is available at pin INT. Operation is controlled via the bits of register Control\_2. Interrupts may be sourced from four places: second and minute timer, countdown timer, alarm function or offset function.

With bit TI\_TP, the timer generated interrupts can be configured to either generate a pulse or to follow the status of the interrupt flags (bits TF and MSF). Correction interrupt pulses are always  $\frac{1}{128}$  second long. Alarm interrupts always follow the condition of AF.

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**Remark:** Note that the interrupts from the four sources are wired-OR, meaning they will mask one another (see Figure 16).

#### 9.9.1 Minute and second interrupts

The pulse generator for the minute and second interrupt operates from an internal 64 Hz clock and consequently generates a pulse of  $\frac{1}{64}$  second in duration.

If the MSF flag is cleared before the end of the INT pulse, then the INT pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced i.e. the system does not have to wait for the completion of the pulse before continuing; see Figure 17. Instructions for clearing MSF are given in Section 9.8.3.

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The timing shown for clearing bit MSF in <u>Figure 17</u> is also valid for the non-pulsed interrupt mode i.e. when bit  $TI_TP = 0$ ,  $\overline{INT}$  may be shortened by setting both MI and SI or MSF to logic 0.

## 9.9.2 Countdown timer interrupts

The generation of interrupts from the countdown timer is controlled via bit TIE.

The pulse generator for the countdown timer interrupt also uses an internal clock, but this time it is dependent on the selected source clock for the countdown timer and on the countdown value n. As a consequence, the width of the interrupt pulse varies (see Table 34).

Source clock (Hz)	INT period (s)	INT period (s)				
	n = 1[1]	n > 1				
4096	1/8192	1⁄4096				
64	<sup>1</sup> / <sub>128</sub>	1⁄64				
1	1/64	1⁄64				
1/60	1/64	1⁄64				

#### Table 34. INT operation (bit TI\_TP = 1)

[1] n = loaded countdown value. Timer stopped when n = 0.

If the TF flag is cleared before the end of the  $\overline{INT}$  pulse, then the  $\overline{INT}$  pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced i.e. the system does not have to wait for the completion of the pulse before continuing (see Figure 18). Instructions for clearing MSF can be found in Section 9.8.3.

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The timing shown for clearing bit TF in Figure 18 is also valid for the non-pulsed interrupt mode i.e. when bit  $TI_TP = 0$ ,  $\overline{INT}$  may be shortened by setting bit TIE to logic 0.

#### 9.9.3 Alarm interrupts

The generation of interrupts from the alarm function is controlled via bit AIE (see <u>Table 6</u>). If bit AIE is enabled, the <u>INT</u> pin follows the condition of bit AF. Clearing bit AF will immediately clear <u>INT</u>. No pulse generation is possible for alarm interrupts (see <u>Figure 19</u>).



#### 9.9.3.1 Correction pulse interrupts

Interrupt pulses generated by correction events can be shortened by writing a logic 1 to bit CIE in register Control\_1.

## 9.10 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] bits in the register Timer\_clkout. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Pin CLKOUT is an open-drain output and enabled at power-on. When disabled the output is high-impedance.

The duty cycle of the selected clock is not controlled. However, due to the nature of the clock generation, all will be 50 : 50 except the 32.768 kHz frequencies.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When the STOP bit is set to logic 1, the CLKOUT pin will generate a continuous LOW for those frequencies that can be stopped. For more details of the STOP bit function see Section 9.13.

Bits COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle <sup>[1]</sup>	Effect of STOP bit
000	32768	60 : 40 to 40 : 60	no effect
001	16384	50 : 50	no effect
010	8192	50 : 50	no effect
011	4096	50 : 50	CLKOUT = LOW
100	2048	50 : 50	CLKOUT = LOW
101	1024	50 : 50	CLKOUT = LOW
110	1 <sup>[2]</sup>	50 : 50	CLKOUT = LOW
111	CLKOUT = high-Z	-	-

#### Table 35. CLKOUT frequency selection

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

[2] 1 Hz clock pulses will be affected by offset correction pulses.

#### 9.10.1 CLKOE pin

The CLKOE pin can be used to block the CLKOUT function and force the CLKOUT pin to an high-impedance state. The effect is the same as setting COF[2:0] = 111.

## 9.11 Offset register

The PCF2123 incorporates an offset register (address 0Dh) which can be used to implement several functions, such as:

- Ageing adjustment
- Temperature compensation
- Accuracy tuning

The offset is made once every two hours in the normal mode, or once every hour in the course mode. Each LSB will introduce an offset of 2.17 ppm for normal mode and 4.34 ppm for course mode. The values of 2.17 ppm and 4.34 ppm are based on a nominal 32.768 kHz clock. The offset value is coded in two's complement giving a range of +63 LSB to -64 LSB.

OFFSET[6:0]	Offset value in	Offset value in ppm				
	decimal	Normal mode MODE = 0	Course mode MODE = 1			
0 1 1 1 1 1 1	+63	+136.71	+273.42			
0 1 1 1 1 1 0	+62	+134.54	+269.08			
:	:	:	:			
0 0 0 0 0 1 0	+2	+4.34	+8.68			
0 0 0 0 0 0 1	+1	+2.17	+4.34			
0 0 0 0 0 0 0	0 <u>[1]</u>	0	0			
1 1 1 1 1 1 1	-1	-2.17	-4.34			
1 1 1 1 1 1 0	-2	-4.34	-8.68			
:	:	:	:			
1 0 0 0 0 0 1	-63	-136.71	-273.42			
1 0 0 0 0 0 0	-64	-138.88	-277.76			

#### Table 36. Register Offset\_register

[1] Default mode.

The correction is made by adding or subtracting 64 Hz clock correction pulses, thereby changing the period of a single second.

Table 37. Example of converting the offset in ppm to seconds

Offset in ppm	Seconds per							
	Day	Week	Month	Year				
2.17	0.187	1.31	5.69	68.2				
4.34	0.375	2.62	11.4	136				

In normal mode, the correction is triggered once per two hours and then correction pulses are applied once per minute until the programmed correction values has been implement.

In course mode, the correction is triggered once per hour and then correction pulses are applied once per minute up to a maximum of 60 minutes. When correction values greater than 60 are used, additional correction pulses are made in the 59th minute (see Table 38).

Correction value	Hour:Minute <sup>[1]</sup>	Correction pulses on INT per minute <sup>[2]</sup>
+1 or –1	02:00	1
	02:01 to 02:59	0
+2 or –2	02:00	1
	02:01	1
	02:02 to 02:59	0
+3 or –3	02:00	1
	02:01	1
	02:02	1
	02:03 to 02:59	0
:	:	:
+59 or –59	02:00 to 02:58	1
	02:59	0
+60 or –60	02:00 to 02:59	1
+61 or –61	02:00 to 02:58	1
	02:59	2
+62 or –62	02:00 to 02:58	1
	02:59	3
+63 or –63	02:00 to 02:58	1
	02:59	4
-64	02:00 to 02:58	1
	02:59	5

 Table 38.
 Correction pulses for course mode

[1] Example is given in a time range from 2:00 to 2:59.

[2] Correction  $\overline{INT}$  pulses are  $\frac{1}{128}$  s wide. For multiple pulses they are repeated at  $\frac{1}{64}$  s interval.

It is possible to monitor when correction pulses are applied. The correction interrupt enable mode (bit CIE) will generate a  $1_{128}$  second pulse on  $\overline{INT}$  for every correction applied. In the case where multiple correction pulses are applied, a  $1_{128}$  second interrupt pulse will be generated and repeated every  $1_{64}$  seconds.

Correction is applied to the 1 Hz clock. Any timer or clock output using a frequency of 1 Hz or below will also be affected by the correction pulses.

Frequency (Hz)	Effect of correction
CLKOUT	
32768	no effect
16384	no effect
8192	no effect
4096	no effect
2048	no effect
1024	no effect
1	effected
Time source clock	
4096	no effect
64	no effect
1	effected
1/60	effected

 Table 39.
 Effect of correction pulses

## 9.12 External clock test mode

A test mode is available which allows for on-board testing. In this mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit EXT\_TEST in register Control\_1. Then pin CLKOUT becomes an input. The test mode replaces the internal clock signal with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT generates an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a minimum period of 1000 ns. The internal clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2<sup>6</sup> divide chain called a prescaler. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0. (STOP must be cleared before the prescaler can operate again.)

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

**Remark:** Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

- 1. Set EXT\_TEST test mode (register Control\_1, bit EXT\_TEST = 1).
- 2. Set STOP (Control\_1, bit STOP = 1).
- 3. Clear STOP (Control\_1, bit STOP = 0).
- 4. Set time registers to desired value.
- 5. Apply 32 clock pulses to pin CLKOUT.
- 6. Read time registers to see the first change.
- 7. Apply 64 clock pulses to pin CLKOUT.
- 8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

## 9.13 STOP bit function

The function of the STOP bit is to allow for accurate starting of the time circuits. The STOP bit function will cause the upper part of the prescaler ( $F_2$  to  $F_{14}$ ) to be held in reset and thus no 1 Hz ticks will be generated. The time circuits can then be set and will not increment until the STOP bit is released (see Figure 21 and Table 40).

The STOP bit function will not affect the output of 32.768 kHz, 16.384 kHz or 8.192 kHz (see Section 9.10).



The lower two stages of the prescaler ( $F_0$  and  $F_1$ ) are not reset and because the SPI-bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between 0 and one 8.192 kHz cycle (see Figure 21).

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The first increment of the time circuits is between 0.499888 s and 0.500000 s after STOP bit is released. The uncertainty is caused by the prescaler bits  $F_0$  and  $F_1$  not being reset (see Table 40).



[1]  $F_0$  is clocked at 32.768 kHz.

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## 9.14 3-line serial interface

Data transfer to and from the device is made via a 3-wire SPI-bus (see Table 41). The data lines for input and output are split. The data input and output lines can be connected together to facilitate a bidirectional data bus. The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the Most Significant Bit (MSB) sent first (see Figure 23).

Table 41.	Serial interface	
Symbol	Function	Description
CE	chip enable input	when LOW, the interface is reset; pull-down resistor included; active input may be higher than V <sub>DD</sub> , but may not be wired permanently HIGH
SCL	serial clock input	when CE is LOW, this input may float; input may be higher than $V_{DD}$
SDI	serial data input	when CE is LOW, input may float; input may be higher than $V_{DD}$ ; input data is sampled on the rising edge of SCL
SDO	serial data output	push-pull output; drives from $V_{SS}$ to $V_{DD}$ ; output data is changed on the falling edge of SCL; will be high-Z when not driving; may be connected directly to SDI



The transmission is controlled by the active HIGH chip enable signal CE. The first byte transmitted is the command byte. Subsequent bytes will be either data to be written or data to be read. Data is sampled on the rising edge of the clock and transferred internally on the falling edge.



The command byte defines the address of the first register to be accessed and the read/write mode. The address counter will auto increment after every access and will rollover to zero after the last register is accessed. The read/write bit (R/W) defines if the following bytes will be read or write information.

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Table 4	42. Command by	te definition	
Bit	Symbol	Value	Description
7	R/W		data read or data write selection
		0	write data
		1	read data
6 to 4	SA	001	subaddress; other codes will cause the device to ignore data transfer
3 to 0	RA	0h to Fh	register address range

-1 - C - 10 ....

In Figure 24, the register Seconds is set to 45 seconds and the register Minutes is set to 10 minutes.



In Figure 25, the Months and Years registers are read. In this example, pins SDI and SDO are not connected together. For this configuration, it is important that pin SDI is never left floating. It must always be driven either HIGH or LOW. If pin SDI is left open, high IDD currents may result. Short transition periods in the order of 200 ns will not cause any problems.



## 9.14.1 Interface watchdog timer

During read/write operations, the time counting circuits are frozen. To prevent a situation where the accessing device becomes locked and does not clear the interface by setting pin CE LOW, the PCF2123 has a built in watchdog timer. Should the interface be active for more than 1 s from the time a valid subaddress is transmitted, then the PCF2123 will automatically clear the interface and allow the time counting circuits to continue counting. CE must return LOW once more before a new data transfer can be executed.



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The watchdog is implemented to prevent the excessive loss of time due to interface access failure e.g. if main power is removed from a battery backed-up system during an interface access.

Each time the watchdog period is exceeded, 1 s will be lost from the time counters. The watchdog will trigger between 1 s and 2 s after receiving a valid subaddress.

# 10. Limiting values

Table 43. Limiting values           In accordance with the Absolute Maximum Rating System (IEC 60134).								
Symbol	Parameter	Conditions	Min	Max	Unit			
V <sub>DD</sub>	supply voltage		<u>[1]</u> –0.5	+6.5	V			
I <sub>DD</sub>	supply current		-50	+50	mA			
VI	input voltage		<u>[1]</u> –0.5	+6.5	V			
Vo	output voltage		<u>[1]</u> –0.5	+6.5	V			
l <sub>l</sub>	input current		-10	+10	mA			
lo	output current		-10	+10	mA			
P <sub>tot</sub>	total power dissipation		-	300	mW			
T <sub>amb</sub>	ambient temperature		-40	+85	°C			
V <sub>esd</sub>	electrostatic discharge	HBM	[2] _	±3000	V			
	voltage	MM	[3] _	±300	V			
l <sub>lu</sub>	latch-up current		<u>[4]</u> _	200	mA			
T <sub>stg</sub>	storage temperature		<u>[5]</u> –65	+150	°C			

[1] With respect to V<sub>SS</sub>.

[2] Pass level; Human Body Model (HBM) according to JESD22-A114.

[3] Pass level; Machine Model (MM), according to JESD22-A115

[4] Pass level; latch-up testing, according to JESD78.

[5] According to the NXP store and transport conditions (document *SNW-SQ-623*) the devices have to be stored at a temperature of +5 °C to +45 °C and a humidity of 25 % to 75 %.

# **11. Static characteristics**

#### Table 44. Static characteristics

 $V_{DD}$  = 1.1 V to 5.5 V;  $V_{SS}$  = 0 V;  $T_{amb}$  = -40 °C to +85 °C;  $f_{osc}$  = 32.768 kHz; quartz  $R_s$  = 15 k $\Omega$ ;  $C_L$  = 7 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Supplies					<i>,</i>		
V <sub>DD</sub>	supply voltage	for clock data integrity; SPI-bus inactive	<u>[1]</u>	1.1	-	5.5	V
		T <sub>amb</sub> = 25 °C		-	0.9	-	V
		SPI-bus active		1.6	-	5.5	V
I <sub>DD</sub>	supply current	SPI-bus active					
		$f_{SCL}$ = 4.5 MHz; V <sub>DD</sub> = 5 V		-	250	400	μA
		f <sub>SCL</sub> = 1.0 MHz; V <sub>DD</sub> = 3 V		-	30	80	μA
		SPI-bus inactive; CLKOUT disabled	[2]				
		$T_{amb} = 25 \ ^{\circ}C;$ $V_{DD} = 2.0 \ V$		-	100	-	nA
		$T_{amb} = 25 \ ^{\circ}C;$ $V_{DD} = 3.0 \ V$		-	110	-	nA
		$T_{amb} = 25 \ ^{\circ}C;$ $V_{DD} = 5.0 \ V$		-	120	-	nA
		SPI-bus inactive; CLKOUT disabled; T <sub>amb</sub> = -40 °C to +85 °C	[2]				
		V <sub>DD</sub> = 2.0 V		-	-	330	nA
		V <sub>DD</sub> = 3.0 V		-	-	350	nA
		V <sub>DD</sub> = 5.0 V		-	-	380	nA
		SPI-bus inactive; CLKOUT enabled at 32 kHz; T <sub>amb</sub> = 25 °C					
		V <sub>DD</sub> = 2.0 V		-	260	-	nA
		V <sub>DD</sub> = 3.0 V		-	340	-	nA
		V <sub>DD</sub> = 5.0 V		-	520	-	nA
		SPI-bus inactive; CLKOUT enabled at 32 kHz; $T_{amb} = -40 \text{ °C}$ to +85 °C					
		V <sub>DD</sub> = 2.0 V		-	-	450	nA
		V <sub>DD</sub> = 3.0 V		-	-	550	nA
		V <sub>DD</sub> = 5.0 V		-	-	750	nA
Inputs							
V <sub>IL</sub>	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V <sub>IH</sub>	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
VI	input voltage	on pins CE, SDI, SCL, OSCI, CLKOE, CLKOUT		-0.5	-	5.5	V

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#### Table 44. Static characteristics ...continued

 $V_{DD} = 1.1 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 \circ C to +85 \circ C; f_{osc} = 32.768 \text{ kHz}; \text{ quartz } R_s = 15 \text{ k}\Omega; C_L = 7 \text{ pF}; \text{ unless otherwise}$ specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
IL	leakage current	$V_I = V_{DD}$ or $V_{SS}$ on pins SDI, SCL, OSCI, CLKOE, CLKOUT		-1	0	+1	μΑ
		$V_I = V_{SS}$ on pin CE		-1	0	-	μΑ
R <sub>pd</sub>	pull-down resistance	on pin CE		-	240	550	kΩ
Ci	input capacitance	-	[3]	-	-	7	pF
Outputs							
Vo	output voltage	on pins CLKOUT and INT	<u>[4]</u>	-0.5	-	5.5	V
		on pin OSCO		-0.5	-	5.5	V
		on pin SDO		-0.5	-	V <sub>DD</sub> +0.5	V
V <sub>OH</sub>	HIGH-level output voltage	on pin SDO		0.8V <sub>DD</sub>	-	V <sub>DD</sub>	V
V <sub>OL</sub>	LOW-level output voltage	on pin SDO		V <sub>SS</sub>	-	$0.2V_{DD}$	V
		on pins CLKOUT and $\overline{INT}$ ; V <sub>DD</sub> = 5 V; I <sub>OL</sub> =1.5 mA		V <sub>SS</sub>	-	0.4	V
I <sub>OH</sub>	HIGH-level output current	$V_{OH} = 4.6 \text{ V};$ $V_{DD} = 5 \text{ V on pin SDO}$		-	-	1.5	mA
I <sub>OL</sub>	LOW-level output current	$V_{OL} = 0.4 V;$ $V_{DD} = 5 V \text{ on pins } \overline{INT}, \text{ SDO}$ and CLKOUT		-1.5	-	-	mA
I <sub>LO</sub>	output leakage current	$V_{O} = V_{DD}$ or $V_{SS}$		-1	0	+1	μΑ
C <sub>L(itg)</sub>	integrated load capacitance	on pins OSCO and OSCI	[5]	3.3	7	14	pF

[1] For reliable oscillator start at power-on:  $V_{DD} = V_{DD(min)} + 0.3 V.$ 

[2] Timer source clock =  $\frac{1}{60}$  Hz, level of pins CE, SDI and SCL is V<sub>DD</sub> or V<sub>SS</sub>.

Implicit by design. [3]

Refers to external pull-up voltage. [4]

Refers to external pull-up voltage. Integrated load capacitance,  $C_{L(itg)}$ , is a calculation of  $C_{OSCI}$  and  $C_{OSCO}$  in series.  $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$ [5]

# **12. Dynamic characteristics**

#### Table 45. SPI-bus characteristics

 $V_{SS} = 0 V$ ;  $T_{amb} = -40 \circ C$  to +85 °C. All timing values are valid within the operating supply voltage and temperature range and referenced to  $V_{IL}$  and  $V_{IH}$  with an input voltage swing of  $V_{SS}$  to  $V_{DD}$ .

Symbol	Parameter	Conditions	V <sub>DD</sub> = 1.6 V		$V_{DD} = 2.4 V$		V <sub>DD</sub> = 3.3 V		V <sub>DD</sub> = 5.0 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Timing ch	naracteristics (see <mark>Fig</mark>	ure 27)									
f <sub>clk(SCL)</sub>	SCL clock frequency		-	2.9	-	4.54	-	5.71	-	8.0	MHz
t <sub>SCL</sub>	SCL time		345	-	220	-	175	-	125	-	ns
t <sub>clk(H)</sub>	clock HIGH time		90	-	50	-	45	-	40	-	ns
t <sub>clk(L)</sub>	clock LOW time		200	-	120	-	95	-	70	-	ns
t <sub>r</sub>	rise time	for SCL signal	-	100	-	100	-	50	-	50	ns
t <sub>f</sub>	fall time	for SCL signal	-	100	-	100	-	50	-	50	ns
t <sub>su(CE)</sub>	CE set-up time		40	-	35	-	30	-	25	-	ns
t <sub>h(CE)</sub>	CE hold time		40	-	30	-	25	-	15	-	ns
t <sub>rec(CE)</sub>	CE recovery time		30	-	25	-	20	-	15	-	ns
t <sub>w(CE)</sub>	CE pulse width	measured after valid subaddress is received	-	0.99	-	0.99	-	0.99	-	0.99	S
t <sub>su</sub>	set-up time	set-up time for SDI data	10	-	5	-	3	-	2	-	ns
t <sub>h</sub>	hold time	hold time for SDI data	25	-	10	-	8	-	5	-	ns
t <sub>d(R)SDO</sub>	SDO read delay time	bus load = 50 pF	-	190	-	108	-	85	-	60	ns
t <sub>dis(SDO)</sub>	SDO disable time	no load value; bus will be held up by bus capacitance; use RC time constant with application values	-	70	-	45	-	40	-	27	ns
$t_{t(SDI-SDO)}$	transition time from SDI to SDO	to avoid bus conflict	0	-	0	-	0	-	0	-	ns

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# **13. Application information**



# 14. Package outline



#### Fig 29. Package outline of PCF2123TS (SOT402-1)

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# HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm

SOT758-1

Fig 30. Package outline of PCF2123BS (SOT758-1)

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# 15. Bare die outline



#### Fig 31. Bare die outline of PCF2123U/10

Table 46.	Bonding pad locations				
Symbol	Pad	Coordinates <sup>[1]</sup>	Coordinates <sup>[1]</sup>		
		x	У		
SDO	1	648.0	-575.0		
SDI	2	648.0	-377.0		
SCL	3	648.0	-179.0		
CLKOE	4	648.0	171.2		
CLKOUT	5	648.0	369.2		
$V_{DD}$	6	648.0	625.7		
OSCI	7	-648.0	639.0		
OSCO	8	-648.0	421.9		
TEST	9	-648.0	-25.9		
INT	10	-648.0	-223.9		
CE	11	-648.0	-441.0		
V <sub>SS</sub> [2]	12	-648.0	-639.0		
Alignment	mark	693	-516.2		

[1] All coordinates are referenced in  $\mu$ m to the center of the die (see Figure 31).

[2] The substrate (rear side of the die) is wired to  $V_{SS}$  but should not be electrically connected.

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# **16. Handling information**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

# 17. Packing information



# **18. Soldering of SMD packages**

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

# 18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- · Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- · Solder bath specifications, including temperature and impurities

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## 18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see <u>Figure 34</u>) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 47 and 48

#### Table 47. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	≥ 350	
< 2.5	235	220	
≥ 2.5	220	220	

#### Table 48. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)			
	Volume (mm <sup>3</sup> )			
	< 350	350 to 2000	> 2000	
< 1.6	260	260	260	
1.6 to 2.5	260	250	245	
> 2.5	250	245	245	

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 34.

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For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

# **19. Abbreviations**

Table 49.	Abbreviations
Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
BCD	Binary Coded Decimal
FFC	Film Frame Carrier
HBM	Human Body Model
LSB	Least Significant Bit
MM	Machine Model
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
RTC	Real Time Clock
SMD	Surface Mount Device
SPI	Serial Peripheral Interface

# 20. Revision history

Table 50. Revision history					
Document ID	Release date	Data sheet status	Change notice	Supersedes	
PCF2123_1	20081119	Product data sheet	-	-	

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Product data sheet

# 21. Legal information

## 21.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## **NXP Semiconductors**

# **PCF2123**

SPI Real time clock/calendar

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