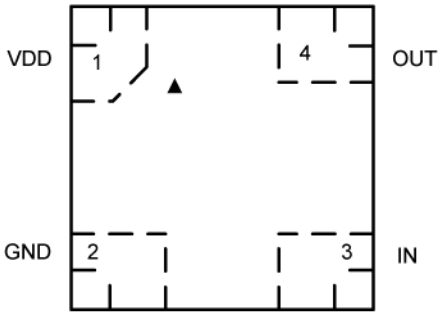
Ordering Information

Part Number	Marking	Package	Junction Temperature Range	Lead Finish
MIC5019YFT	H9	4-pin 1.2mm x 1.2mm Thin QFN	-40˚C to +125˚C	Pb-Free

Note:
Thin QFN pin 1 identifier = "▲"

Pin Configuration



1.2mm x 1.2mm Thin QFN (FT)
(TOP View)

Pin Description

Pin Number	Pin Name	Pin Function
1	VDD	Supply Voltage: +2.7V to +9V supply.
2	GND	Ground.
3	IN	Control Input: Logic high drives the gate output above the supply voltage. Logic low forces the gate output near ground. Do not leave this pin floating.
4	OUT	Gate Output: Connection to gate of external MOSFET.

Absolute Maximum Ratings[1]

VDD to GND..……..…….. ……..……..……...+10V
IN to GND……..…….-0.6V to +10V
OUT to GND……..……..+19V
Junction Temperature (T_J) .....–55°C to +150°C
Storage Temperature (T_s) .....–55°C to +165°C
ESD Rating[2]……..……1.5kV HBM
ESD Rating ……..200V MM

Operating Ratings[3]

VDD to GND…….....……+2.7V to +9V
IN to GND……0V to VDD
Junction Temperature (T_J)……...–40°C to +125°C
Thermal Resistance
(θ_{JC})……..60°C/W
(θ_{JA})……..……140°C/W

Electrical Characteristics[4]

2.7V ≤ VDD ≤ 9V; T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

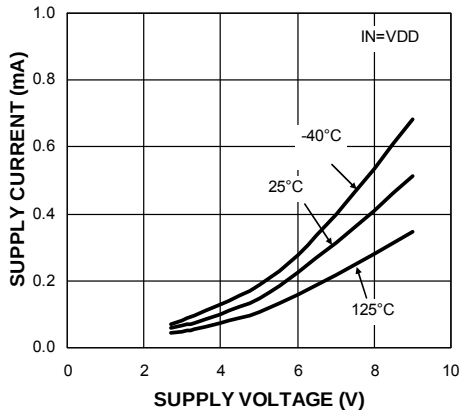
Parameter	Condition		Min	Typ	Max	Units
Supply Current	VDD = 3.3V	IN = 0V		0.15	**1**	µA
		IN = 3.3V		77	**140**	
	VDD = 5V	IN = 0V			**1**	
		IN = 3.3V		150	**300**	
IN Voltage		IN =Logic Low			**0.8**	V
	2.7V ≤ VDD ≤ 3.6V	IN = Logic High	**2.7**			
	3.6V < VDD ≤ 9V	IN = Logic High	**3.0**			
IN Current	2.7V ≤ VDD ≤ 9V			0.1	1	µA
IN Capacitance				5		pF
OUT Voltage	VDD = 2.7V		6.3	8.2		V
	VDD = 3.0V		7.1	9.3		
	VDD = 4.5V		11.4	14.8		
OUT Zener Diode Clamp Voltage	VDD = 9V		13	16.5	19	V
OUT Current[5]	VDD = 5V	VOUT = 10V		10.6		µA
OUT Turn-On Time[6]	VDD = 4.5V	C_L = 1000pF		0.440	1.5	ms
		C_L = 3000pF		1.34	4.2	
OUT Turn-Off Time[7]	VDD = 4.5V	CL = 1000pF		5.56	20	µs
		CL = 3000 pF		17.6	60	

Notes:

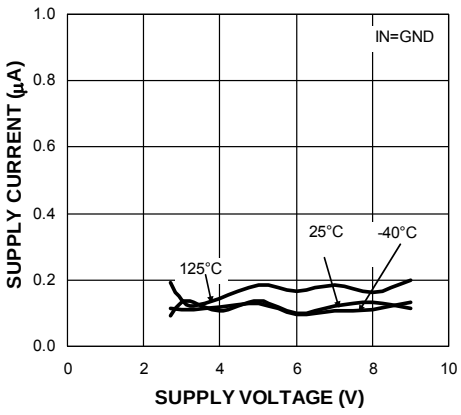
1. Exceeding the absolute maximum rating may damage the device.
2. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
3. The device is not guaranteed to function outside operating range.
4. Specification for packaged product only.
5. Resistive load selected to achieve V_{OUT} = 10V.
6. Turn-On Time is the time required for the gate voltage to rise to 4V above the supply voltage.
7. Turn-Off Time is the time required for the gate voltage to fall to 4V above the supply voltage.

Typical Characteristics

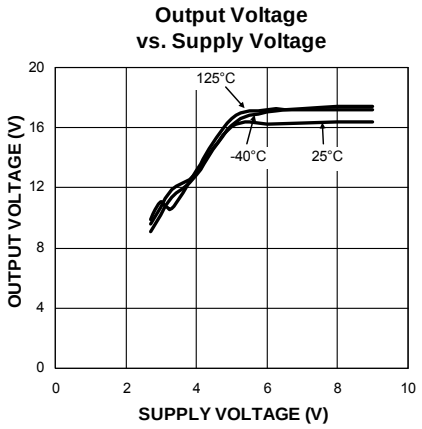
VDD Supply Current vs. Supply Voltage



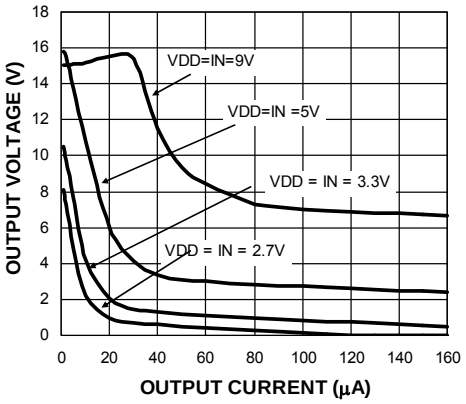
VDD Supply Current vs. Supply Voltage



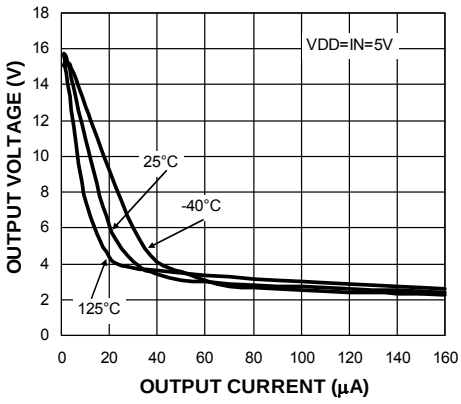
Output Voltage vs. Supply Voltage



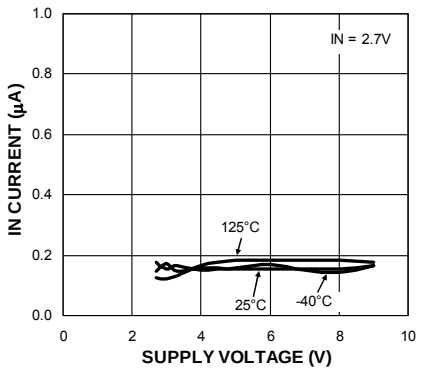
Output Voltage vs. Output Current



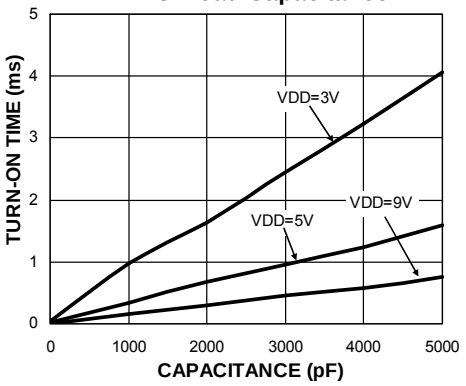
Output Voltage vs. Output Current



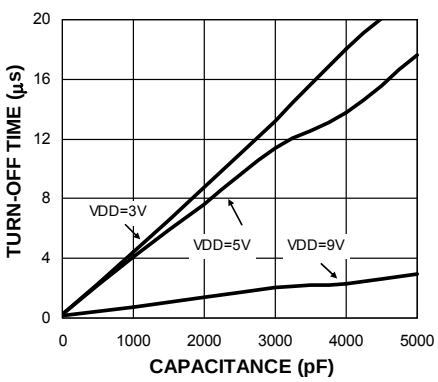
IN Current vs. Supply Voltage



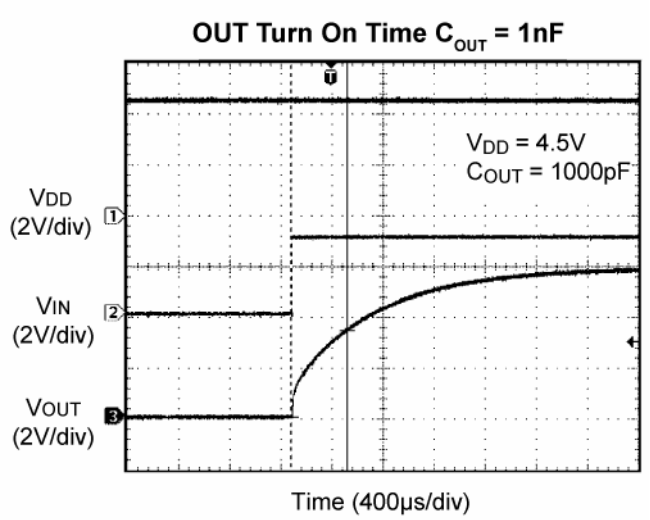
OUT Turn-On Time vs. Load Capacitance

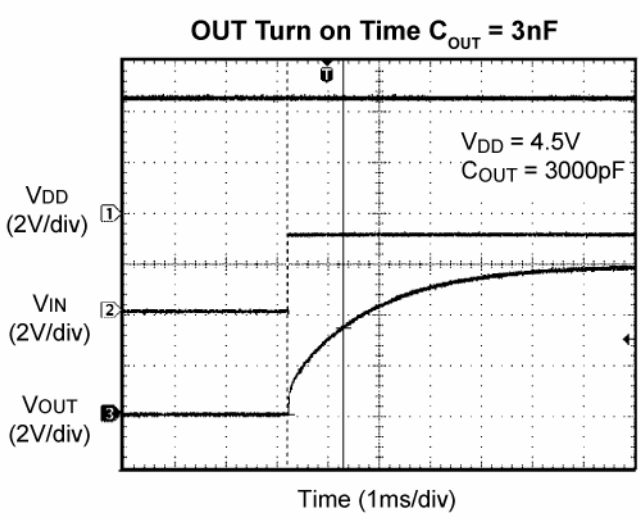


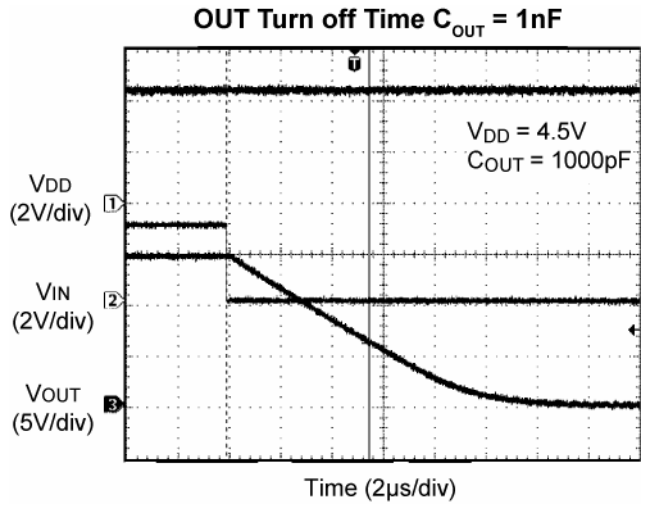
OUT Turn-Off Time vs. Load Capacitance

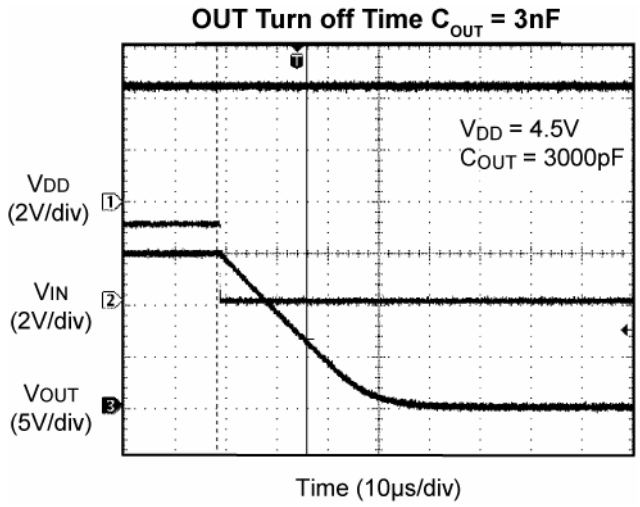


Functional Characteristics

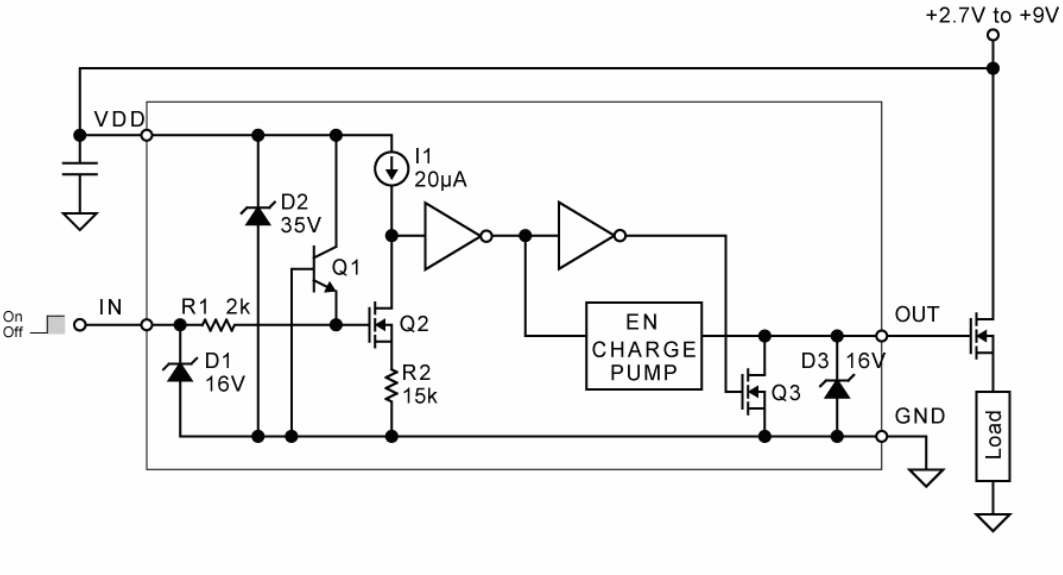








Functional Diagram



Functional Diagram with External Components
(High-Side Driver Configuration)

Functional Description

The MIC5019 is a non-inverting device. Applying a logic high signal to IN (control input) produces gate drive output. The OUT (Gate Output) is used to turn on an external N-channel MOSFET.

Supply

VDD (supply) is rated for +2.7V to +9V. An external capacitor is recommended to decouple noise.

Control

IN is the control input. IN must be forced high or low by an external signal. Do not leave IN floating as a floating input may cause unpredictable operation.

A high input turns on Q2, which sinks the output of current source I1, making the input of the first inverter low. The inverter output becomes high enabling the charge pump.

Charge Pump

The charge pump is enabled when IN is logic high. The charge pump consists of an oscillator and voltage quadrupler (4×). The output voltage is limited to 16V typically by a zener diode. The charge pump output voltage will be approximately:

$V_{OUT} = 4 \times V_{DD} – 2.8V$, but not exceeding 19Vmax.

The oscillator operates from approximately 70kHz to approximately 100kHz depending upon the supply voltage and temperature.

OUT

The charge pump output is connected directly to the OUT pin. The charge pump is active only when IN is high. When IN is low, Q3 is turned on by the second inverter and discharges the gate of the external MOSFET to force it off.

If IN is high, and the voltage applied to VDD drops to zero, the gate output will be floating (unpredictable).

ESD Protection

D1 and D2 clamp positive and negative ESD voltages. R1 isolates the gate of Q2 from sudden changes on the IN input. Q1 turns on if the emitter (IN input) is forced below ground to provide additional input protection. Zener D3 also clamps ESD voltages for the OUT (gate output).

Application Information

Supply Bypass

A capacitor from VDD to GND is recommended to control switching and supply transients. Load current and supply lead length are some of the factors that affect capacitor size requirements.

A 4.7µF or 10µF ceramic capacitor, aluminum electrolytic or tantalum capacitor is suitable for many applications.

The low ESR (equivalent series resistance) of ceramic and tantalum capacitors makes them especially effective, but also makes them susceptible to uncontrolled inrush current from low impedance voltage sources (such as NiCd batteries or automatic test equipment). Avoid applying voltage instantaneously, capable of high peak current, directly to or near tantalum capacitors without additional current limiting. Normal power supply turn-on (slow rise time) or printed circuit trace resistance is usually adequate for normal product usage.

MOSFET Selection

The MIC5019 is designed to drive N-channel enhancement type MOSFETs. The gate output (OUT) of the MIC5019 provides a voltage, referenced to ground, that is greater than the supply voltage. Refer to the "Typical Characteristics: Output Voltage vs. Supply Voltage" graph.

The supply voltage and the MOSFET drain-to-source voltage drop determine the gate-to-source voltage.

$$V_{GS} = V_{OUT} - (V_{SUPPLY} - V_{DS})$$

where:

V_{GS} = gate-to-source voltage (enhancement)

V_{OUT} = OUT voltage (from graph "OUT Voltage vs Supply Voltage)

V_{DD} = supply voltage

V_{DS} = drain-to-source voltage
(approx. 0V at low current, or when fully enhanced)

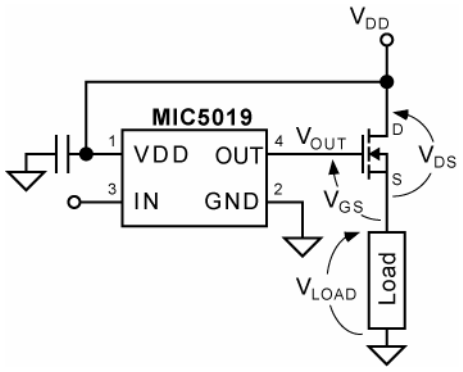


Figure 1. Node Voltages

The performance of the MOSFET is determined by the gate-to-source voltage. Choose the type of MOSFET according to the calculated gate-to-source voltage.

Standard MOSFET

Standard MOSFETs are fully enhanced with a gate-to-source voltage of about 10V. Their absolute maximum gate-to-source voltage is ±20V.With a 4.5V supply, the MIC5019 produces a gate output of approximately 15V. Figure 2 shows how the remaining voltages conform. The actual drain-to-source voltage drop across an IRFZ24 is less than 0.1V with a 1A load and 10V enhancement. Higher current increases the drain-to-source voltage drop, increasing the gate-to-source voltage.

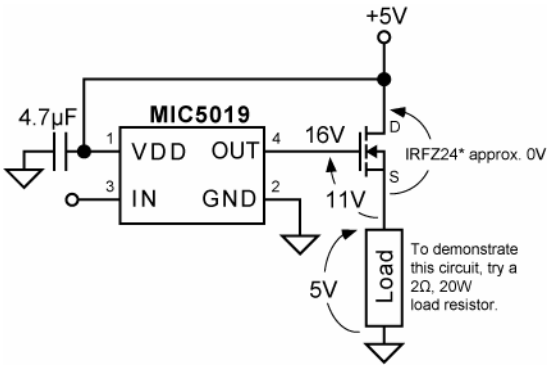


Figure 2. Using a Standard MOSFET

The MIC5019 has an internal zener diode that limits the gate-to-ground voltage to approximately 16V.

Lower supply voltages, such as 3.3V, produce lower gate output voltages which will not fully enhance standard MOSFETs. This significantly reduces the maximum current that can be switched. Always refer to the MOSFET data sheet to predict the MOSFET's performance in specific applications.

Logic-Level MOSFET

Logic-level N-channel MOSFETs are fully enhanced with a gate-to-source voltage of approximately 5V. Some of the MOSFET's may have an absolute maximum gate-to-source voltage of ±10V (Refer to MOSFET datasheet).

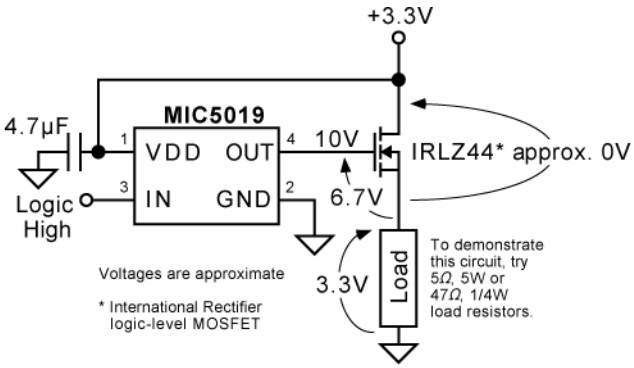


Figure 3. Using a Logic-Level MOSFET

Refer to Figure 3 for an example showing nominal voltages. The maximum gate-to-source voltage rating of some of the logic-level MOSFET can be ±10V; this can be exceeded if a higher supply voltage is used. An external zener diode can clamp the gate-to-source voltage as shown in Figure 4. The zener voltage, plus its tolerance, must not exceed the absolute maximum gate voltage of the MOSFET.

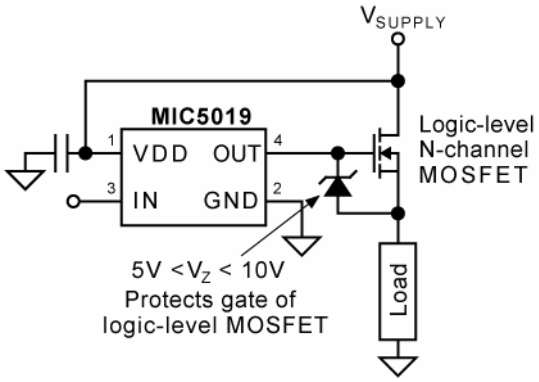


Figure 4. Gate-to-Source Protection

A gate-to-source zener may also be required when the maximum gate-to-source voltage could be exceeded due to normal part-to-part variation in gate output voltage. Other conditions can momentarily increase the gate-to-source voltage, such as turning on a capacitive load or shorting a load.

Inductive Loads

Inductive loads include relays, and solenoids. Long leads may also have enough inductance to cause adverse effects in some circuits.

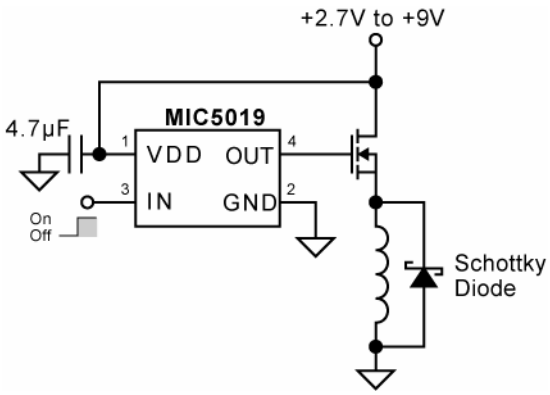


Figure 5. Switching an Inductive Load

Switching off an inductive load in a high-side application momentarily forces the MOSFET source negative (as the inductor opposes changes to current). This voltage spike can be very large and can exceed a MOSFET's gate-to-source and drain-to-source ratings. A Schottky diode across the inductive load provides a discharge current path to minimize the voltage spike. The peak current rating of the diode should be greater than the load current.

In a low-side application, switching off an inductive load will momentarily force the MOSFET drain higher than the supply voltage. The same precaution applies.

Split Power Supply

Refer to Figure 6. The MIC5019 can be used to control a 12V load by separating the driver supply from the load supply.

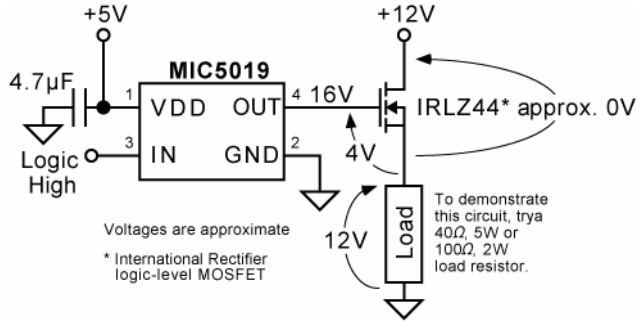


Figure 6. 12V High-Side Switch

A logic-level MOSFET is required. The MOSFET's maximum current is limited slightly because the gate is not fully enhanced. To predict the MOSFETs performance for any pair of supply voltages, calculate the gate-to-source voltage and refer to the MOSFET data sheet.

$$V_{GS} = V_{OUT} – (V_{LOAD\ SUPPLY} – V_{DS})$$

V_{OUT} is determined from the driver supply voltage using the "Typical Characteristics: Output Voltage vs. Supply Voltage" graph.

Low-Side Switch Configuration

The low-side configuration makes it possible to switch a voltage much higher than the MIC5019's maximum supply voltage.

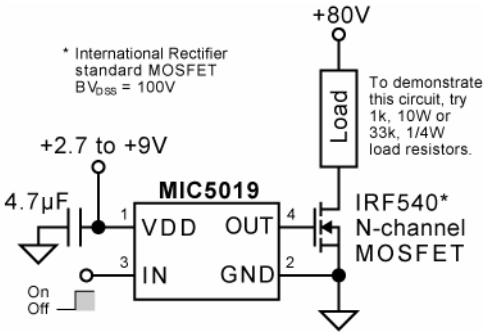
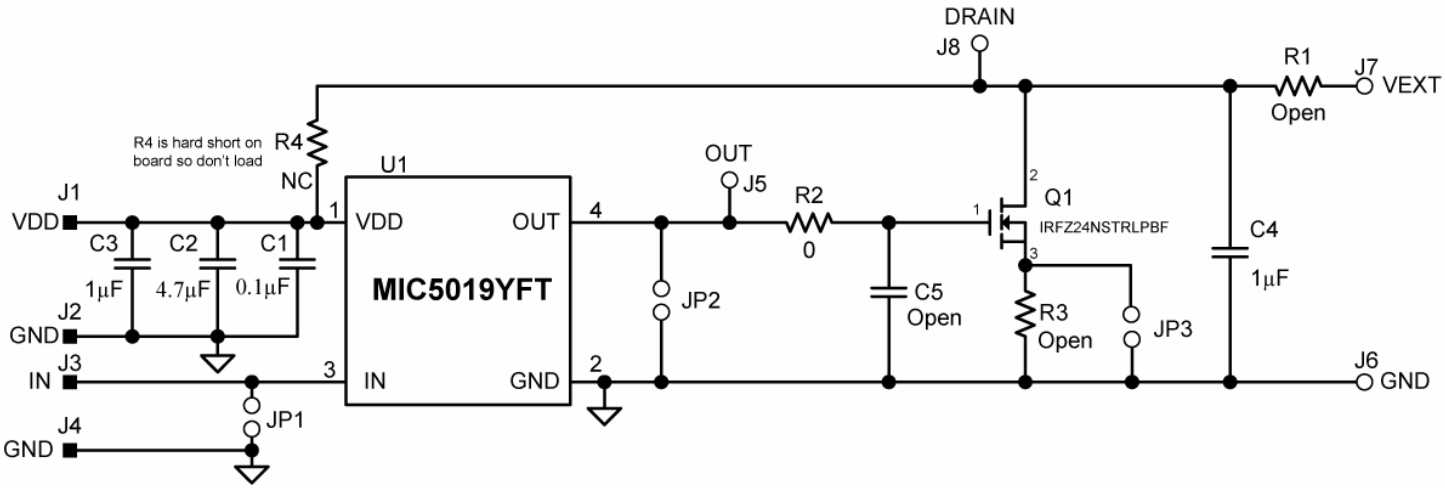


Figure 7. Low-Side Switch Configuration

The maximum switched voltage is limited only by the MOSFET's maximum drain-to-source ratings.

Evaluation Board Schematic



Bill of Materials

Item	Part Number	Manufacturer	Description	Qty
C1	GRM188R71C104KA01D	Murata[1]	0.1µF/16V Ceramic Capacitor, X7R, Size 0603	1
C2	C2012X7R1C475K	TDK[2]	4.7µF/16V Ceramic Capacitor, X7R, Size 0805	1
	GRM21BR71C475KA73L	Murata		
	0805YC475KAT2A	AVX[3]		
R1, R3, C3, C4, Q1 (Open)				
C5 (Open)			Used as gate Cap, different values	
R2	CRCW06030000FKEA	Vishay Dale[4]	0Ω Resistor, Size 0603, 5%	1
U1	**MIC5019YFT**	**Micrel. Inc.[5]**	**High Side/Low Side MOSFET Driver**	**1**

Notes:

1. Murata: www.murata.com.
2. TDK: www.tdk.com.
3. AVX: www.avx.com
4. Vishay: www.vishay.com
5. **Micrel, Inc.: www.micrel.com.**

PCB Layout

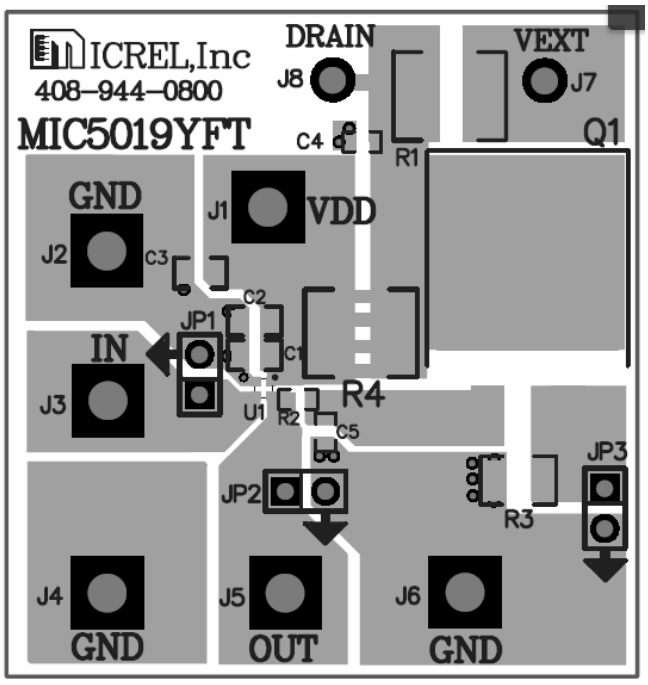


Figure 8. MIC5019 Evaluation Board Top Layer

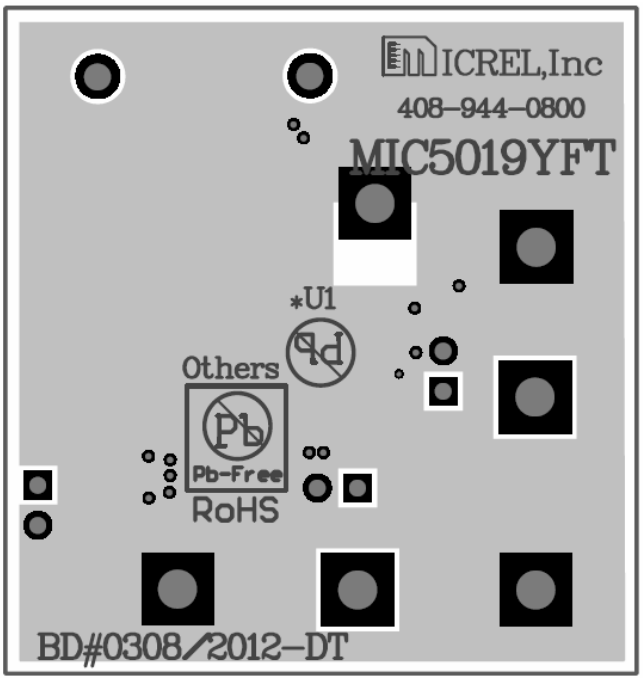
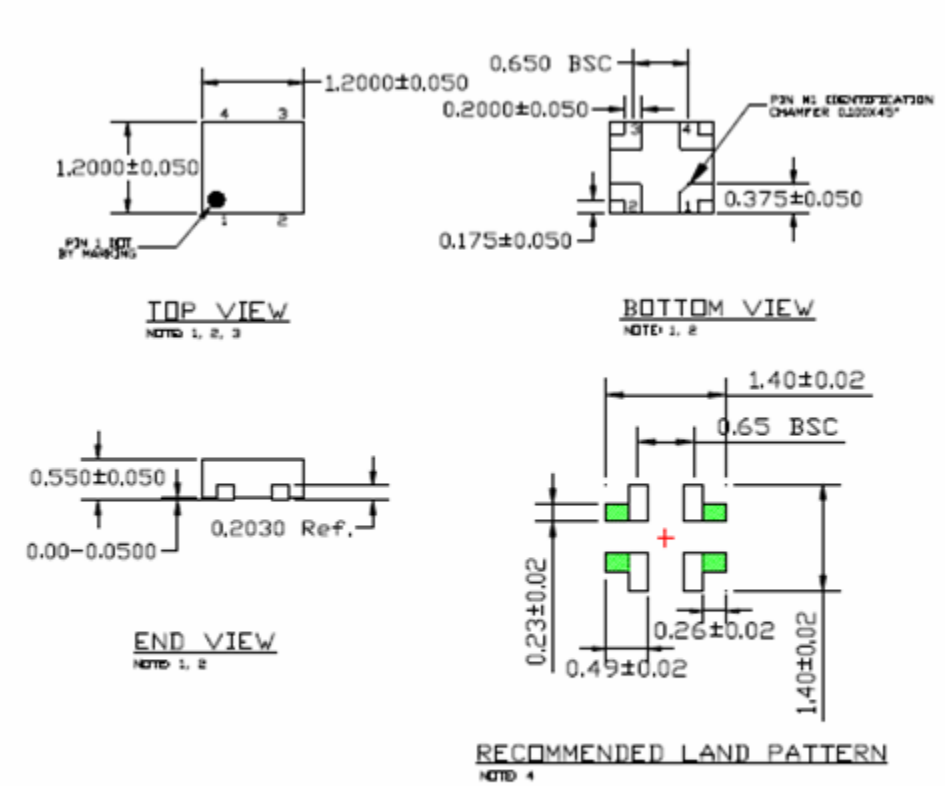


Figure 9. MIC5019 Evaluation Board Bottom Layer

Package Information



1.2mm x 1.2mm x 0.55mm 4 Pin QFN (FT)

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TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com