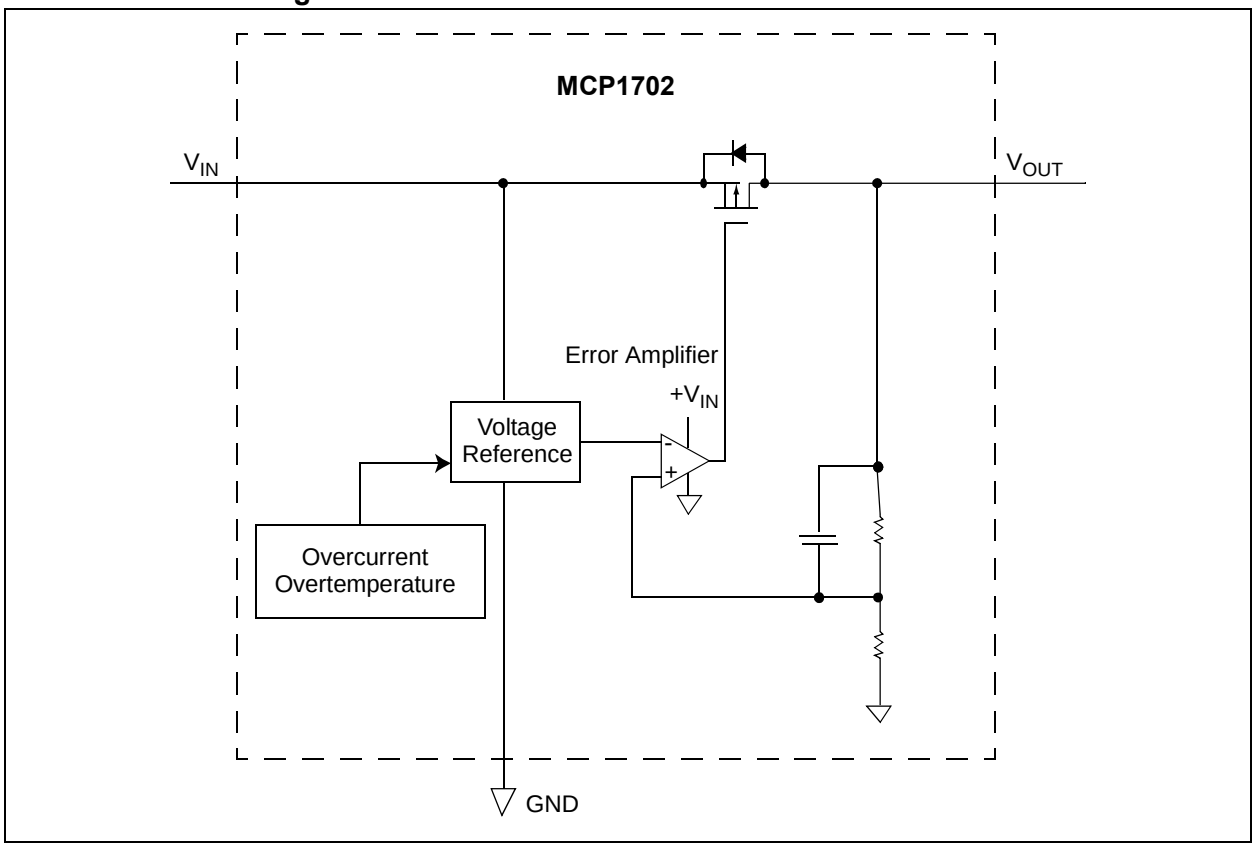
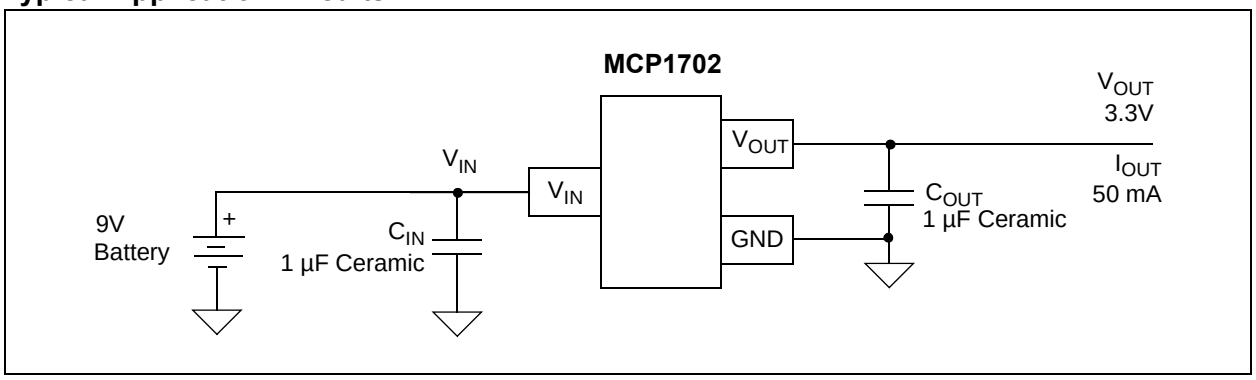
Functional Block Diagrams



Typical Application Circuits



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD}.....+14.5V

All inputs and outputs w.r.t. .....(V_{SS}-0.3V) to (V_{IN}+0.3V)

Peak Output Current .....500 mA

Storage temperature .....-65°C to +150°C

Maximum Junction Temperature..... 150°C

ESD protection on all pins (HBM;MM)..... ≥ 4 kV; ≥ 400V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all limits are established for $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$, **Note 1**, I_{LOAD} = 100 µA, C_{OUT} = 1 µF (X7R), C_{IN} = 1 µF (X7R), T_A = +25°C.
Boldface type applies for junction temperatures, T_J of -40°C to +125°C. **(Note 7)**

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input / Output Characteristics						
Input Operating Voltage	V_{IN}	**2.7**	—	**13.2**	V	**Note 1**
Input Quiescent Current	I_q	—	2.0	**5**	µA	I_L = 0 mA
Maximum Output Current	I_{OUT_mA}	**250**	—	—	mA	For $V_R \geq 2.5V$
		50	100	—	mA	For $V_R < 2.5V$, $V_{IN} \geq 2.7V$
		100	130	—	mA	For $V_R < 2.5V$, $V_{IN} \geq 2.95V$
		150	200	—	mA	For $V_R < 2.5V$, $V_{IN} \geq 3.2V$
		200	250	—	mA	For $V_R < 2.5V$, $V_{IN} \geq 3.45V$
Output Short Circuit Current	I_{OUT_SC}	—	400	—	mA	$V_{IN} = V_{IN(MIN)}$ **(Note 1)**, V_{OUT} = GND, Current (average current) measured 10 ms after short is applied.
Output Voltage Regulation	V_{OUT}	**V_R-3.0%**	V_R±0.4%	**V_R+3.0%**	V	**Note 2**
		V_R-2.0%	V_R±0.4%	V_R+2.0%	V	
		V_R-1.0%	V_R±0.4%	V_R+1.0%	V	1% Custom
V_{OUT} Temperature Coefficient	TCV_{OUT}	—	50	—	ppm/°C	**Note 3**
Line Regulation	$\Delta V_{OUT}/(V_{OUT} X \Delta V_{IN})$	**-0.3**	±0.1	**+0.3**	%/V	$(V_{OUT(MAX)} + V_{DROPOUT(MAX)}) \leq V_{IN} \leq 13.2V$, **(Note 1)**
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	**-2.5**	±1.0	**+2.5**	%	I_L = 1.0 mA to 250 mA for $V_R \geq 2.5V$ I_L = 1.0 mA to 200 mA for $V_R < 2.5V$, V_{IN} = 3.45V (**Note 4**)

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage. For example: V_R = 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V, 4.0V, or 5.0V. The input voltage $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$ or V_{IN} = 2.7V (whichever is greater); I_{OUT} = 100 µA.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta Temperature)$, $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its measured value with an applied input voltage of $V_{OUT(MAX)} + V_{DROPOUT(MAX)}$ or 2.7V, whichever is greater.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the ambient temperature is not significant.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are established for $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$, **Note 1**, I_{LOAD} = 100 µA, C_{OUT} = 1 µF (X7R), C_{IN} = 1 µF (X7R), T_A = +25°C.
Boldface type applies for junction temperatures, T_J of -40°C to +125°C. **(Note 7)**

Parameters	Sym	Min	Typ	Max	Units	Conditions
Dropout Voltage (**Note 1**, **Note 5**)	$V_{DROPOUT}$	—	330	**650**	mV	I_L = 250 mA, V_R = 5.0V
		—	525	**725**	mV	I_L = 250 mA, 3.3V ≤ V_R < 5.0V
		—	625	**975**	mV	I_L = 250 mA, 2.8V ≤ V_R < 3.3V
		—	750	**1100**	mV	I_L = 250 mA, 2.5V ≤ V_R < 2.8V
		—	—	—	mV	V_R < 2.5V, See Maximum Output Current Parameter
Output Delay Time	T_{DELAY}	—	1000	—	µs	V_{IN} = 0V to 6V, V_{OUT} = 90% V_R R_L = 50Ω resistive
Output Noise	e_N	—	8	—	µV/(Hz)$^{1/2}$	I_L = 50 mA, f = 1 kHz, C_{OUT} = 1 µF
Power Supply Ripple Rejection Ratio	PSRR	—	44	—	dB	f = 100 Hz, C_{OUT} = 1 µF, I_L = 50 mA, V_{INAC} = 100 mV pk-pk, C_{IN} = 0 µF, V_R = 1.2V
Thermal Shutdown Protection	T_{SD}	—	150	—	°C	

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage. For example: V_R = 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V, 4.0V, or 5.0V. The input voltage $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$ or V_{IN} = 2.7V (whichever is greater); I_{OUT} = 100 µA.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) *10^6 / (V_R * \Delta Temperature)$, $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its measured value with an applied input voltage of $V_{OUT(MAX)} + V_{DROPOUT(MAX)}$ or 2.7V, whichever is greater.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the ambient temperature is not significant.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40		+125	°C	Steady State
Maximum Junction Temperature	T_J	—		+150	°C	Transient
Storage Temperature Range	T_A	-65		+150	°C	
Thermal Package Resistance (Note 2)						
Thermal Resistance, 3L-SOT-23A	θ_{JA}	—	336	—	°C/W	EIA/JEDEC JESD51-7 FR-4 0.063 4-Layer Board
	θ_{JC}	—	110	—	°C/W	
Thermal Resistance, 3L-SOT-89	θ_{JA}	—	153.3	—	°C/W	EIA/JEDEC JESD51-7 FR-4 0.063 4-Layer Board
	θ_{JC}	—	100	—	°C/W	
Thermal Resistance, 3L-TO-92	θ_{JA}	—	131.9	—	°C/W	
	θ_{JC}	—	66.3	—	°C/W	

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

2: Thermal Resistance values are subject to change. Please visit the Microchip web site for the latest packaging information.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: V_R = 2.8V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

Note: Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction temperature over the Ambient temperature is not significant.

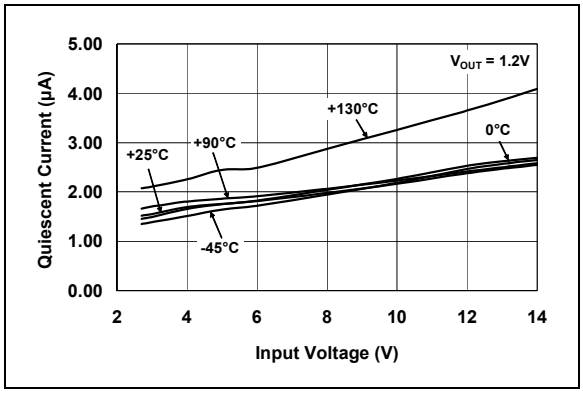


FIGURE 2-1: *Quiescent Current vs. Input Voltage.*

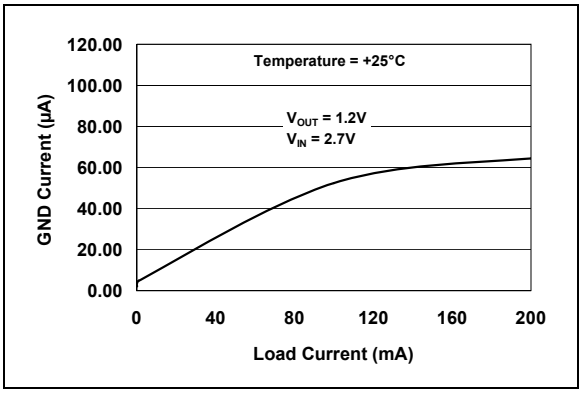


FIGURE 2-4: *Ground Current vs. Load Current.*

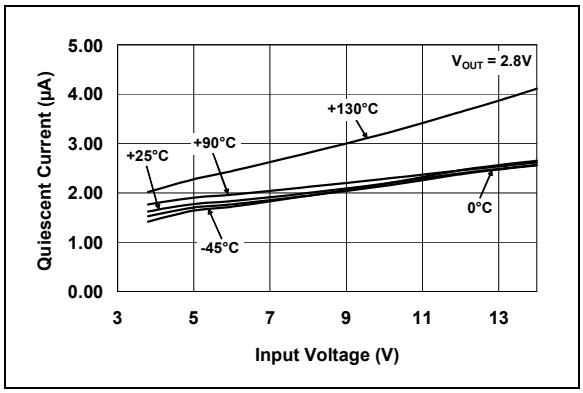


FIGURE 2-2: *Quiescent Current vs.Input Voltage.*

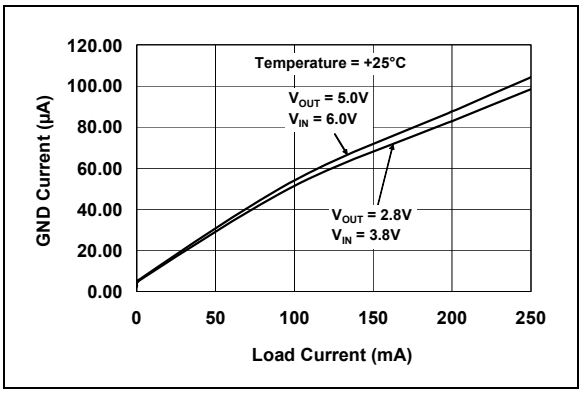


FIGURE 2-5: *Ground Current vs. Load Current.*

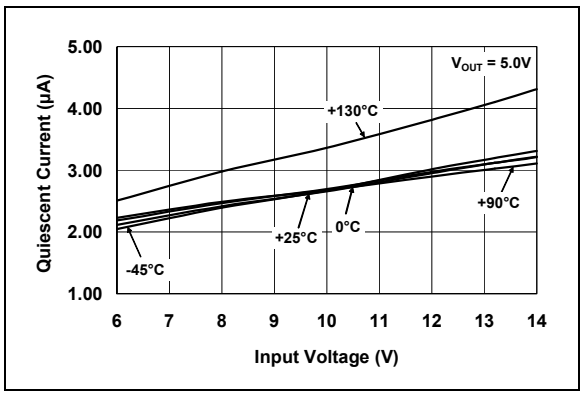


FIGURE 2-3: *Quiescent Current vs.Input Voltage.*

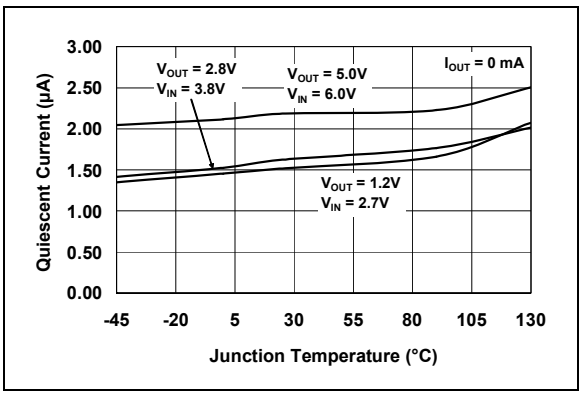


FIGURE 2-6: *Quiescent Current vs. Junction Temperature.*

Note: Unless otherwise indicated: V_R = 2.8V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

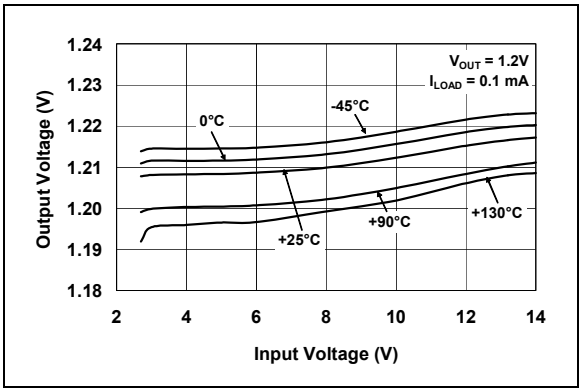


FIGURE 2-7: *Output Voltage vs. Input Voltage.*

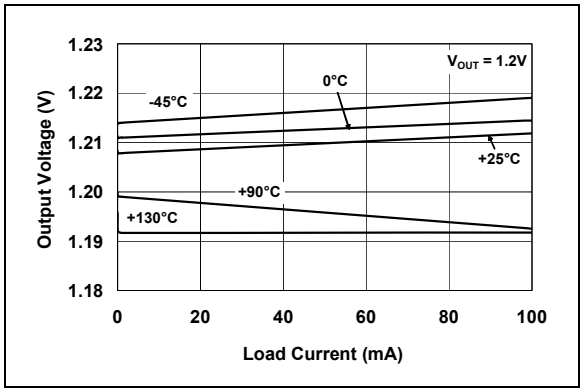


FIGURE 2-10: *Output Voltage vs. Load Current.*

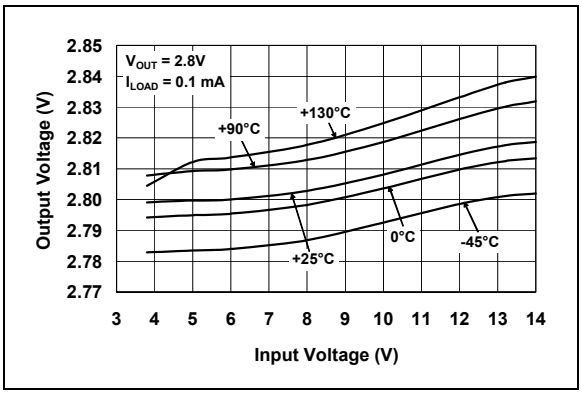


FIGURE 2-8: *Output Voltage vs. Input Voltage.*

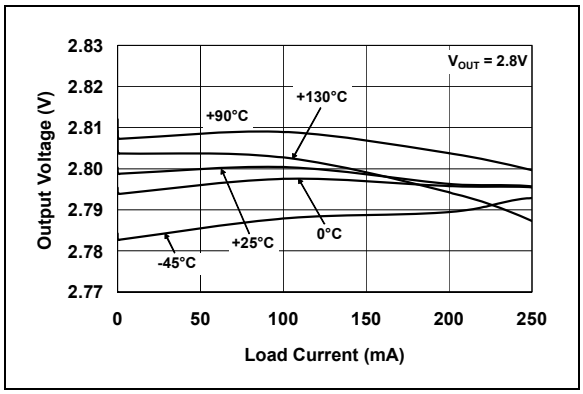


FIGURE 2-11: *Output Voltage vs. Load Current.*

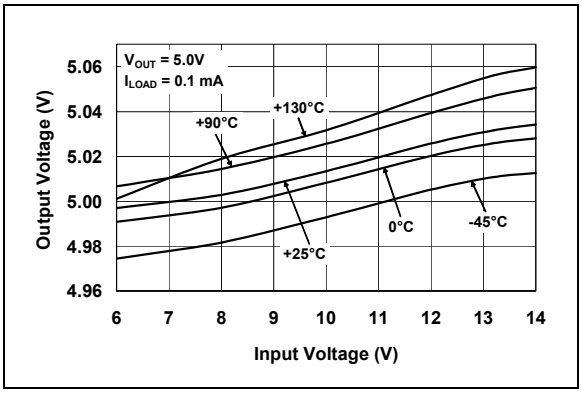


FIGURE 2-9: *Output Voltage vs. Input Voltage.*

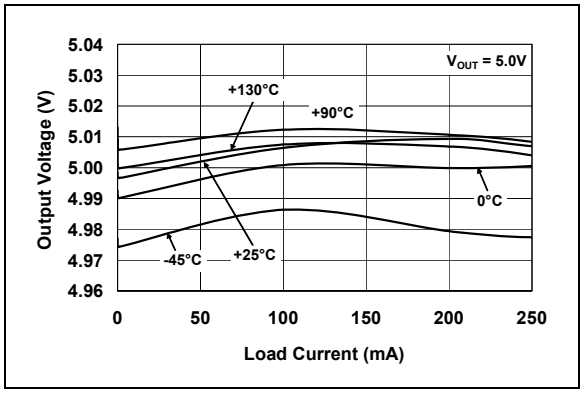


FIGURE 2-12: *Output Voltage vs. Load Current.*

Note: Unless otherwise indicated: V_R = 2.8V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

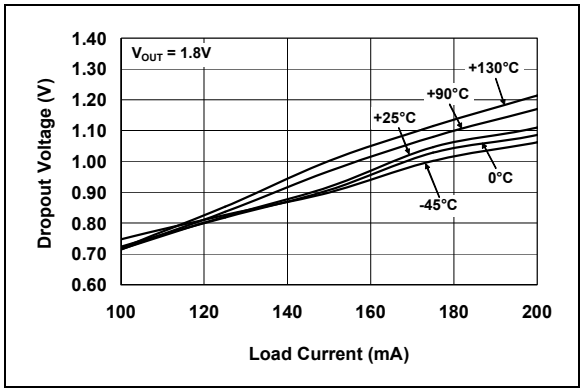


FIGURE 2-13: *Dropout Voltage vs. Load Current.*

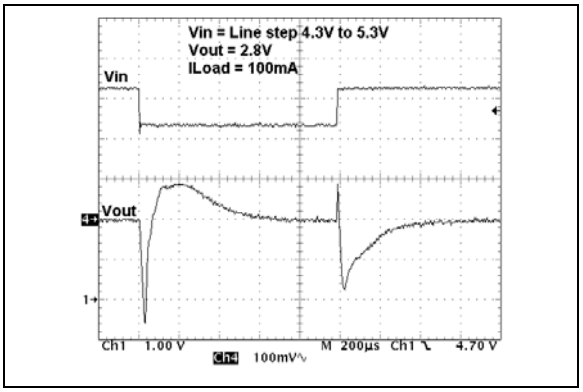


FIGURE 2-16: *Dynamic Line Response.*

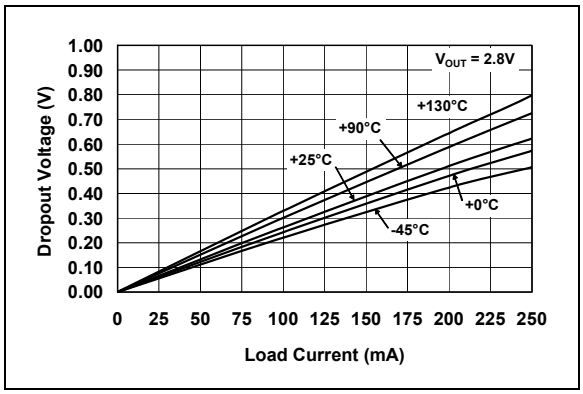


FIGURE 2-14: *Dropout Voltage vs. Load Current.*

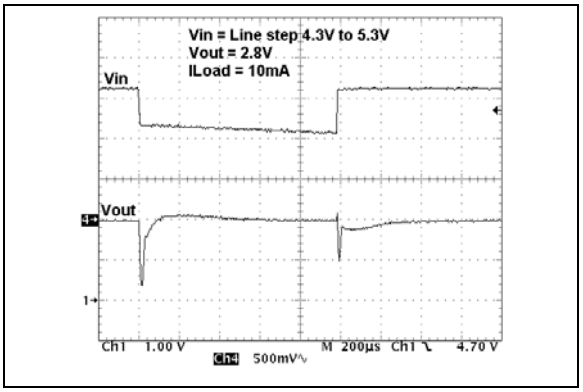


FIGURE 2-17: *Dynamic Line Response.*

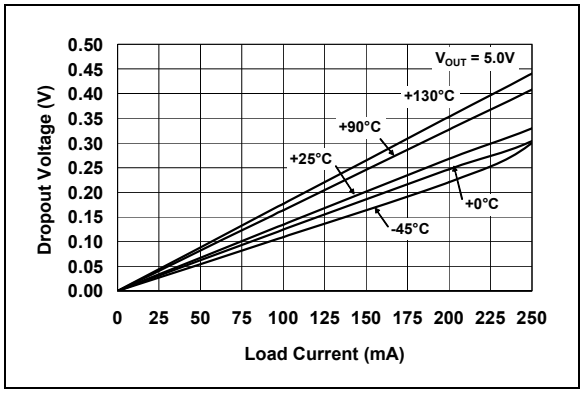


FIGURE 2-15: *Dropout Voltage vs. Load Current.*

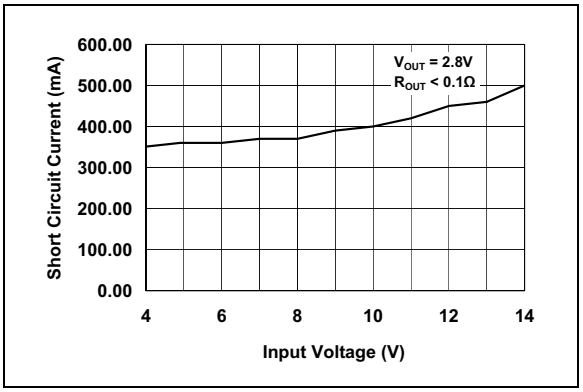


FIGURE 2-18: *Short Circuit Current vs. Input Voltage.*

Note: Unless otherwise indicated: V_R = 2.8V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

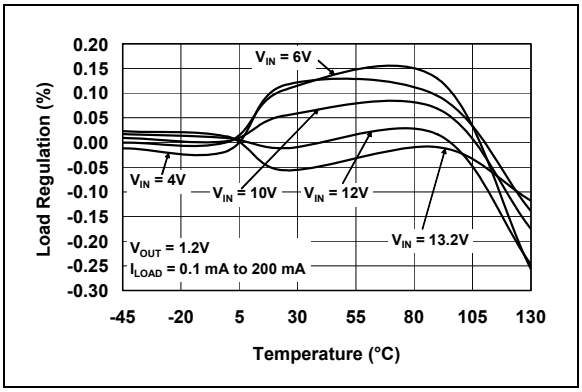


FIGURE 2-19: *Load Regulation vs. Temperature.*

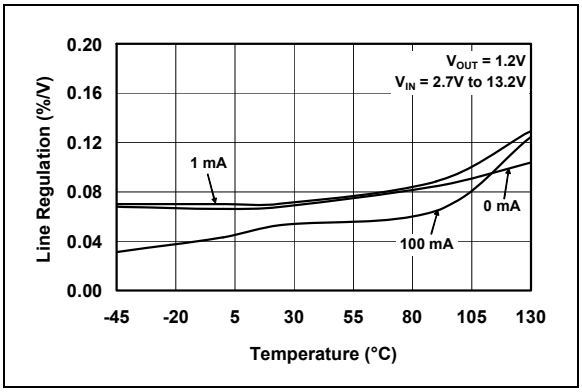


FIGURE 2-22: *Line Regulation vs. Temperature.*

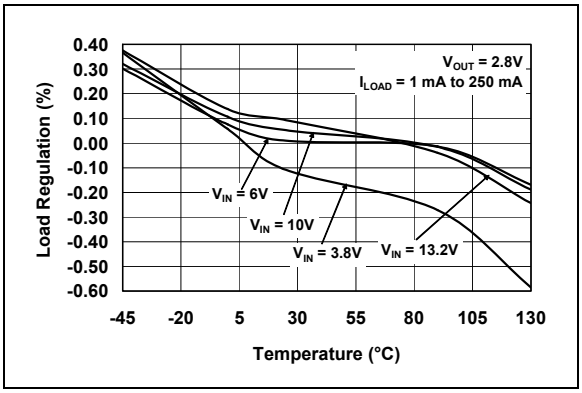


FIGURE 2-20: *Load Regulation vs. Temperature.*

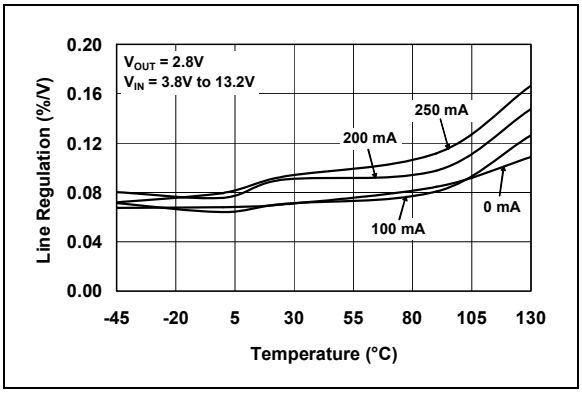


FIGURE 2-23: *Line Regulation vs. Temperature.*

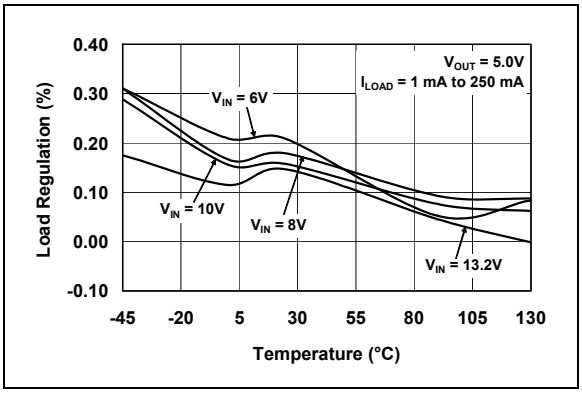


FIGURE 2-21: *Load Regulation vs. Temperature.*

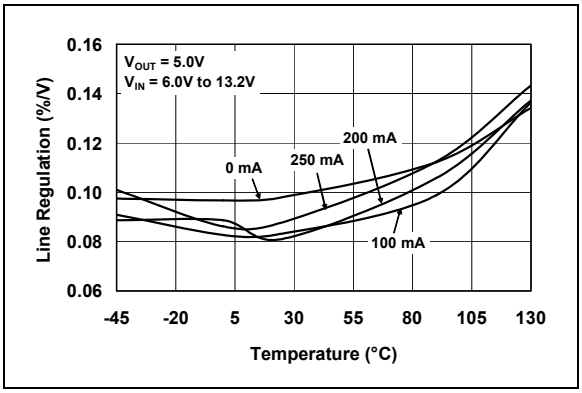


FIGURE 2-24: *Line Regulation vs. Temperature.*

Note: Unless otherwise indicated: V_R = 2.8V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 100 µA, T_A = +25°C, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

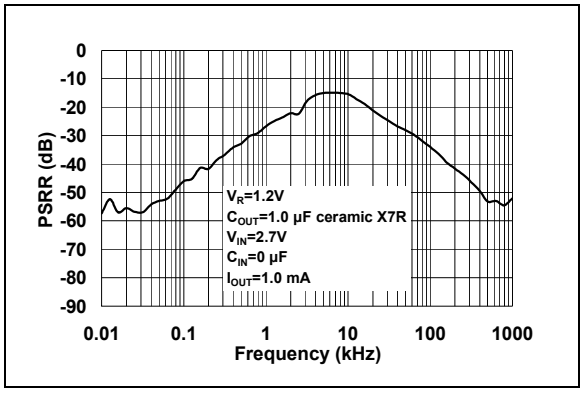


FIGURE 2-25: *Power Supply Ripple Rejection vs. Frequency.*

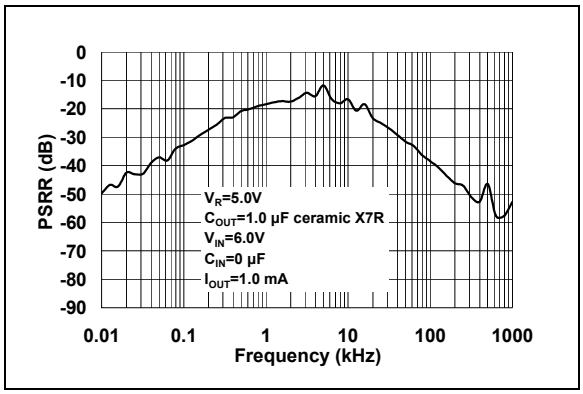


FIGURE 2-26: *Power Supply Ripple Rejection vs. Frequency.*

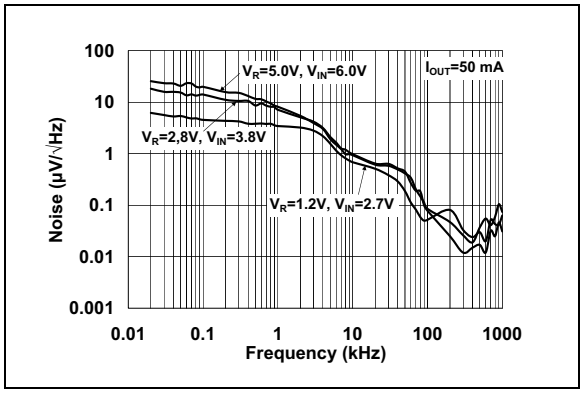


FIGURE 2-27: *Output Noise vs. Frequency.*

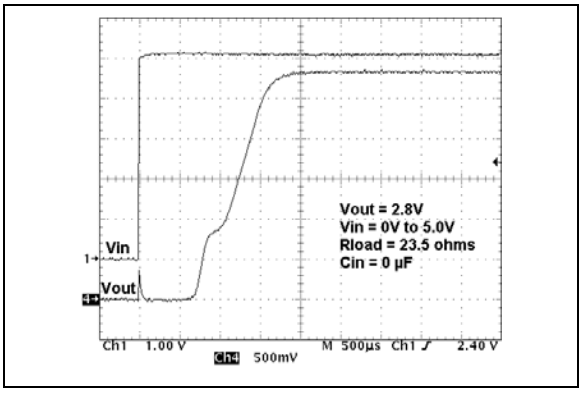


FIGURE 2-28: *Power Up Timing.*

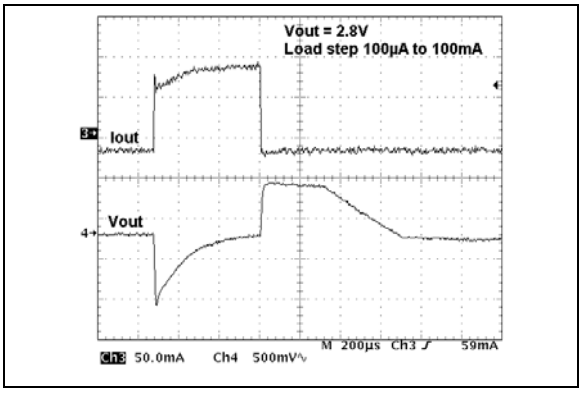


FIGURE 2-29: *Dynamic Load Response.*

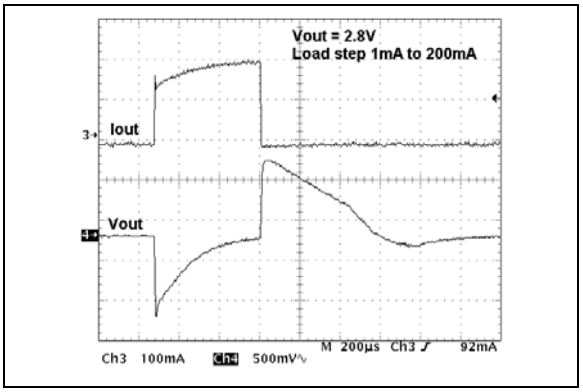


FIGURE 2-30: *Dynamic Load Response.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. SOT-23A	Pin No. SOT-89	Pin No. TO-92	Symbol	Function
1	1	1	GND	Ground Terminal
2	3	3	V_{OUT}	Regulated Voltage Output
3	2, Tab	2	V_{IN}	Unregulated Supply Voltage
–	–	–	NC	No connection

3.1 Ground Terminal (GND)

Regulator ground. Tie GND to the negative side of the output and the negative side of the input capacitor. Only the LDO bias current (2.0 µA typical) flows out of this pin; there is no high current. The LDO output regulation is referenced to this pin. Minimize voltage drops between this pin and the negative side of the load.

3.2 Regulated Output Voltage (V_{OUT})

Connect V_{OUT} to the positive side of the load and the positive terminal of the output capacitor. The positive side of the output capacitor should be physically located as close to the LDO V_{OUT} pin as is practical. The current flowing out of this pin is equal to the DC load current.

3.3 Unregulated Input Voltage Pin (V_{IN})

Connect V_{IN} to the input unregulated source voltage. Like all LDO linear regulators, low source impedance is necessary for the stable operation of the LDO. The amount of capacitance required to ensure low source impedance will depend on the proximity of the input source capacitors or battery type. For most applications, 1 µF of capacitance will ensure stable operation of the LDO circuit. For applications that have load currents below 100 mA, the input capacitance requirement can be lowered. The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high-frequency.

4.0 DETAILED DESCRIPTION

4.1 Output Regulation

A portion of the LDO output voltage is fed back to the internal error amplifier and compared with the precision internal band gap reference. The error amplifier output will adjust the amount of current that flows through the P-Channel pass transistor, thus regulating the output voltage to the desired value. Any changes in input voltage or output current will cause the error amplifier to respond and adjust the output voltage to the target voltage (refer to Figure 4-1).

4.2 Overcurrent

The MCP1702 internal circuitry monitors the amount of current flowing through the P-Channel pass transistor. In the event of a short-circuit or excessive output current, the MCP1702 will turn off the P-Channel device for a short period, after which the LDO will attempt to restart. If the excessive current remains, the cycle will repeat itself.

4.3 Overtemperature

The internal power dissipation within the LDO is a function of input-to-output voltage differential and load current. If the power dissipation within the LDO is excessive, the internal junction temperature will rise above the typical shutdown threshold of 150°C. At that point, the LDO will shut down and begin to cool to the typical turn-on junction temperature of 130°C. If the power dissipation is low enough, the device will continue to cool and operate normally. If the power dissipation remains high, the thermal shutdown protection circuitry will again turn off the LDO, protecting it from catastrophic failure.

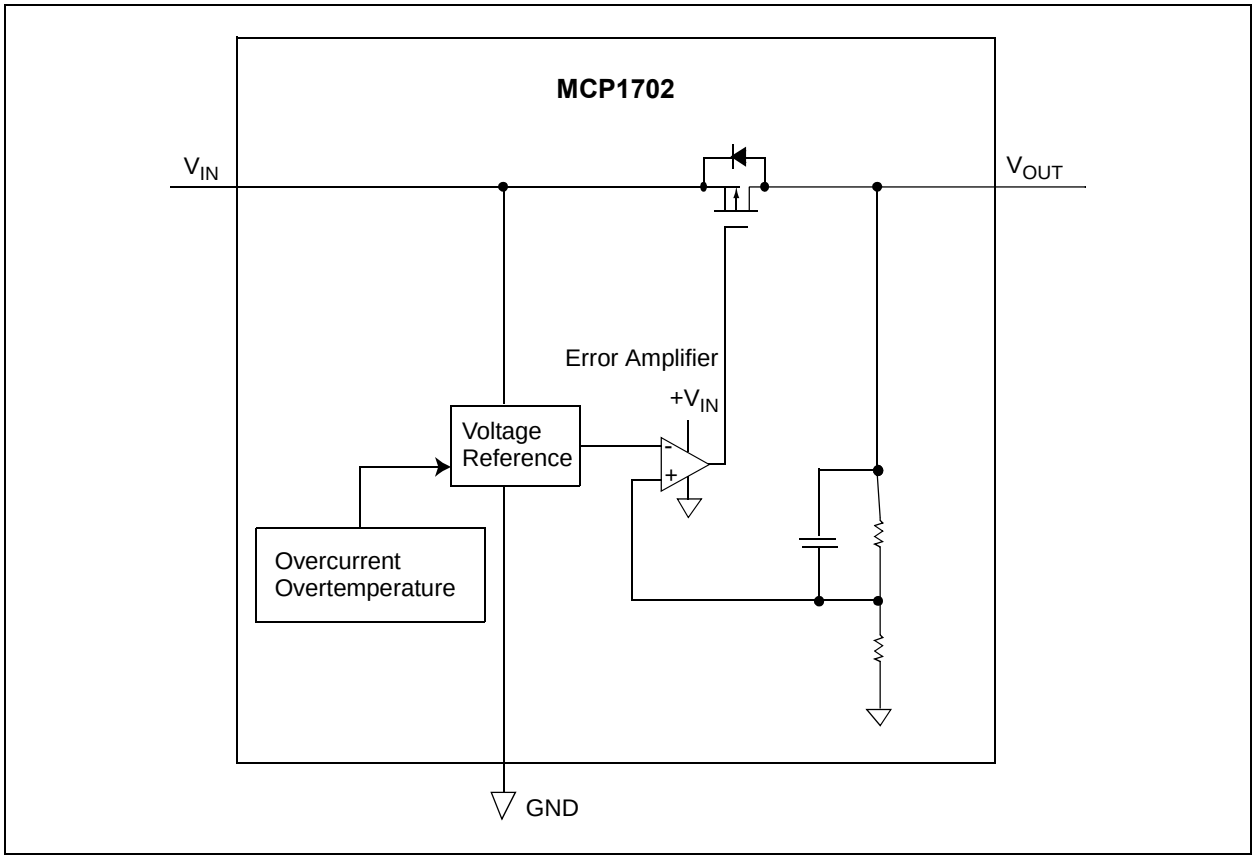


FIGURE 4-1: *Block Diagram.*

5.0 FUNCTIONAL DESCRIPTION

The MCP1702 CMOS LDO linear regulator is intended for applications that need the lowest current consumption while maintaining output voltage regulation. The operating continuous load range of the MCP1702 is from 0 mA to 250 mA ($V_R \geq 2.5V$). The input operating voltage range is from 2.7V to 13.2V, making it capable of operating from two or more alkaline cells or single and multiple Li-Ion cell batteries.

5.1 Input

The input of the MCP1702 is connected to the source of the P-Channel PMOS pass transistor. As with all LDO circuits, a relatively low source impedance (10Ω) is needed to prevent the input impedance from causing the LDO to become unstable. The size and type of the capacitor needed depends heavily on the input source type (battery, power supply) and the output current range of the application. For most applications (up to 100 mA), a 1 µF ceramic capacitor will be sufficient to ensure circuit stability. Larger values can be used to improve circuit AC performance.

5.2 Output

The maximum rated continuous output current for the MCP1702 is 250 mA ($V_R \geq 2.5V$). For applications where $V_R < 2.5V$, the maximum output current is 200 mA.

A minimum output capacitance of 1.0 µF is required for small signal stability in applications that have up to 250 mA output current capability. The capacitor type can be ceramic, tantalum or aluminum electrolytic. The esr range on the output capacitor can range from 0Ω to 2.0Ω.

The output capacitor range for ceramic capacitors is 1 µF to 22 µF. Higher output capacitance values may be used for tantalum and electrolytic capacitors. Higher output capacitor values pull the pole of the LDO transfer function inward that results in higher phase shifts which in turn cause a lower crossover frequency. The circuit designer should verify the stability by applying line step and load step testing to their system when using capacitance values greater than 22 µF.

5.3 Output Rise Time

When powering up the internal reference output, the typical output rise time of 500 µs is controlled to prevent overshoot of the output voltage. There is also a start-up delay time that ranges from 300 µs to 800 µs based on loading. The start-up time is separate from and precedes the Output Rise Time. The total output delay is the Start-up Delay plus the Output Rise time.

6.0 APPLICATION CIRCUITS AND ISSUES

6.1 Typical Application

The MCP1702 is most commonly used as a voltage regulator. Its low quiescent current and low dropout voltage makes it ideal for many battery-powered applications.

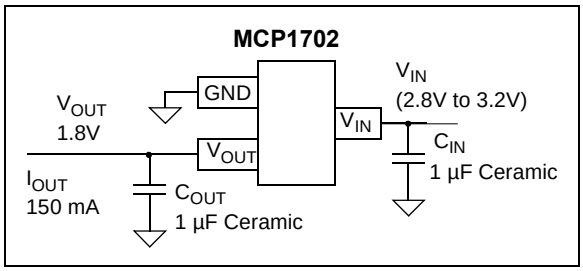


FIGURE 6-1: *Typical Application Circuit.*

6.1.1 APPLICATION INPUT CONDITIONS

Package Type	=	SOT-23A
Input Voltage Range	=	2.8V to 3.2V
V_{IN} maximum	=	3.2V
V_{OUT} typical	=	1.8V
I_{OUT}	=	150 mA maximum

6.2 Power Calculations

6.2.1 POWER DISSIPATION

The internal power dissipation of the MCP1702 is a function of input voltage, output voltage and output current. The power dissipation, as a result of the quiescent current draw, is so low, it is insignificant (2.0 µA x V_{IN}). The following equation can be used to calculate the internal power dissipation of the LDO.

EQUATION 6-1:

$$P_{LDO} = (V_{IN(MAX))} - V_{OUT(MIN)}) \times I_{OUT(MAX))}$$

Where:

P_{LDO}	=	LDO Pass device internal power dissipation
$V_{IN(MAX)}$	=	Maximum input voltage
$V_{OUT(MIN)}$	=	LDO minimum output voltage

The maximum continuous operating junction temperature specified for the MCP1702 is +125°C. To estimate the internal junction temperature of the MCP1702, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ($R\theta_{JA}$). The thermal resistance from junction to ambient for the SOT-23A pin package is estimated at 336°C/W.

EQUATION 6-2:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{AMAX}$$

Where:

$T_{J(MAX)}$	=	Maximum continuous junction temperature
P_{TOTAL}	=	Total device power dissipation
$R\theta_{JA}$		Thermal resistance from junction to ambient
T_{AMAX}	=	Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

EQUATION 6-3:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

Where:

$P_{D(MAX)}$	=	Maximum device power dissipation
$T_{J(MAX)}$	=	Maximum continuous junction temperature
$T_{A(MAX)}$		Maximum ambient temperature
$R\theta_{JA}$	=	Thermal resistance from junction to ambient

EQUATION 6-4:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

Where:

$T_{J(RISE)}$	=	Rise in device junction temperature over the ambient temperature
P_{TOTAL}	=	Maximum device power dissipation
$R\theta_{JA}$		Thermal resistance from junction to ambient

EQUATION 6-5:

$$T_J = T_{J(RISE)} + T_A$$

Where:

T_J	=	Junction Temperature
$T_{J(RISE)}$	=	Rise in device junction temperature over the ambient temperature
T_A		Ambient temperature

6.3 Voltage Regulator

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation, as a result of ground current, is small enough to be neglected.

6.3.1 POWER DISSIPATION EXAMPLE

Package

Package Type = SOT-23A

Input Voltage

V_{IN} = 2.8V to 3.2V

LDO Output Voltages and Currents

V_{OUT} = 1.8V

I_{OUT} = 150 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = +40°C

Internal Power Dissipation

Internal Power dissipation is the product of the LDO output current times the voltage across the LDO (V_{IN} to V_{OUT}).

$P_{LDO(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$

$P_{LDO} = (3.2V - (0.97 \times 1.8V)) \times 150\ mA$

P_{LDO} = 218.1 milli-Watts

Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface mount packages. The EIA/JEDEC specification is JESD51-7, "High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages". The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, *"A Method to Determine How Much Power a SOT-23 Can Dissipate in an Application"*, (DS00792), for more information regarding this subject.

$T_{J(RISE)} = P_{TOTAL} \times Rq_{JA}$

T_{JRISE} = 218.1 milli-Watts x 336.0°C/Watt

T_{JRISE} = 73.3°C

Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below.

$T_J = T_{JRISE} + T_{A(MAX)}$

T_J = 113.3°C

Maximum Package Power Dissipation at +40°C Ambient Temperature Assuming Minimal Copper Usage.

SOT-23 (336.0°C/Watt = $R\theta_{JA}$)

$P_{D(MAX)}$ = (+125°C - 40°C) / 336°C/W

$P_{D(MAX)}$ = 253 milli-Watts

SOT-89 (153.3°C/Watt = $R\theta_{JA}$)

$P_{D(MAX)}$ = (+125°C - 40°C) / 153.3°C/W

$P_{D(MAX)}$ = 0.554 Watts

TO92 (131.9°C/Watt = $R\theta_{JA}$)

$P_{D(MAX)}$ = (+125°C - 40°C) / 131.9°C/W

$P_{D(MAX)}$ = 644 milli-Watts

6.4 Voltage Reference

The MCP1702 can be used not only as a regulator, but also as a low quiescent current voltage reference. In many microcontroller applications, the initial accuracy of the reference can be calibrated using production test equipment or by using a ratio measurement. When the initial accuracy is calibrated, the thermal stability and line regulation tolerance are the only errors introduced by the MCP1702 LDO. The low-cost, low quiescent current and small ceramic output capacitor are all advantages when using the MCP1702 as a voltage reference.

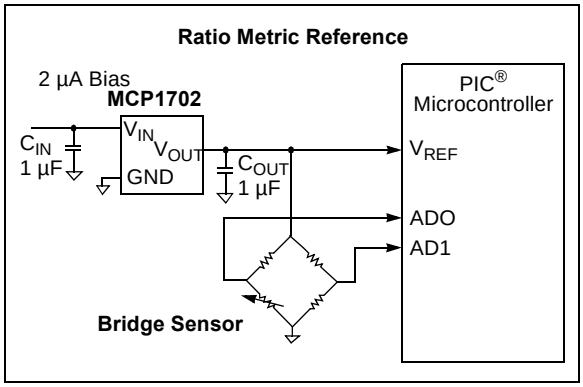


FIGURE 6-2: *Using the MCP1702 as a Voltage Reference.*

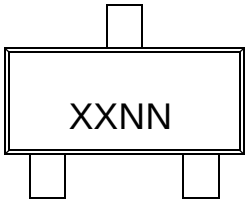
6.5 Pulsed Load Applications

For some applications, there are pulsed load current events that may exceed the specified 250 mA maximum specification of the MCP1702. The internal current limit of the MCP1702 will prevent high peak load demands from causing non-recoverable damage. The 250 mA rating is a maximum average continuous rating. As long as the average current does not exceed 250 mA, pulsed higher load currents can be applied to the MCP1702. The typical current limit for the MCP1702 is 500 mA (T_A +25°C).

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

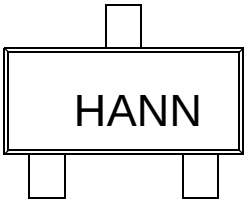
3-Pin SOT-23A



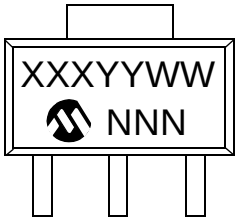
Standard			
Extended Temp			
Symbol	**Voltage ***	**Symbol**	**Voltage ***
HA	1.2	HF	3.0
HB	1.5	HG	3.3
HC	1.8	HH	4.0
HD	2.5	HJ	5.0
HE	2.8	—	—
Custom			
GA	4.5	GC	2.1
GB	2.2	GD	4.1

* Custom output voltages available upon request.
Contact your local Microchip sales office for more information.

Example:



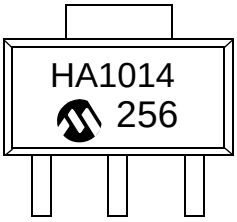
3-Lead SOT-89



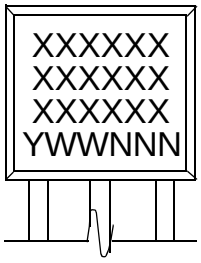
Standard			
Extended Temp			
Symbol	**Voltage ***	**Symbol**	**Voltage ***
HA	1.2	HF	3.0
HB	1.5	HG	3.3
HC	1.8	HK	3.6
HD	2.5	HH	4.0
HE	2.8	HJ	5.0
Custom			
LA	2.1	H9	4.2
LB	3.2	—	—

* Custom output voltages available upon request.
Contact your local Microchip sales office for more information.

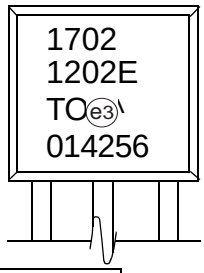
Example:



3-Lead TO-92



Example:

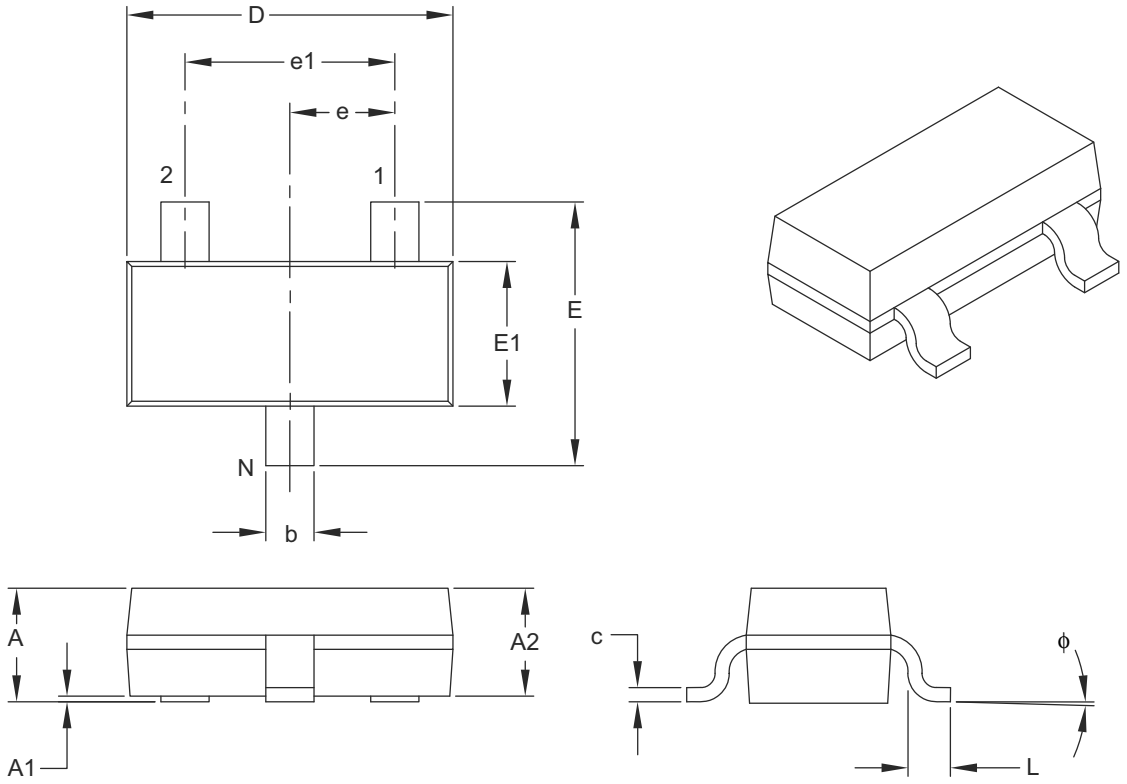


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

3-Lead Plastic Small Outline Transistor (CB) [SOT-23A]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		3	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.89	–	1.45
Molded Package Thickness	A2	0.90	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.10	–	3.00
Molded Package Width	E1	1.20	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.15	–	0.60
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.09	–	0.26
Lead Width	b	0.30	–	0.51

Notes:

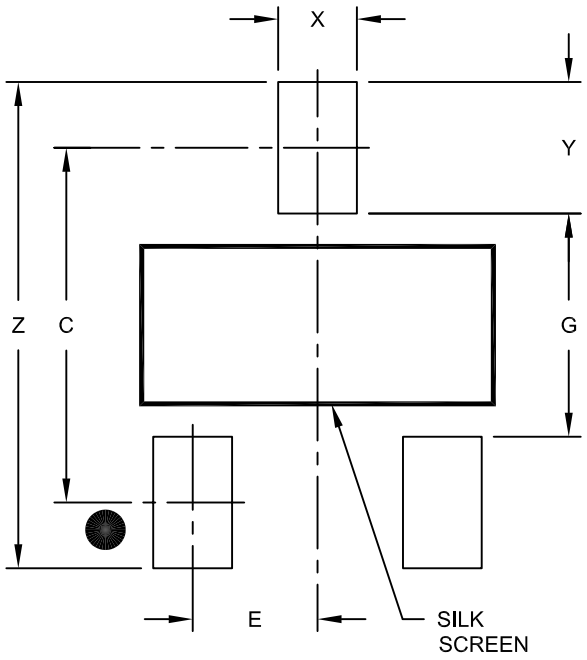
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-130B

3-Lead Plastic Small Outline Transistor (CB) [SOT-23A]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.70	
Contact Pad Width (X3)	X			0.60
Contact Pad Length (X3)	Y			1.00
Distance Between Pads	G	1.70		
Overall Width	Z			3.70

Notes:

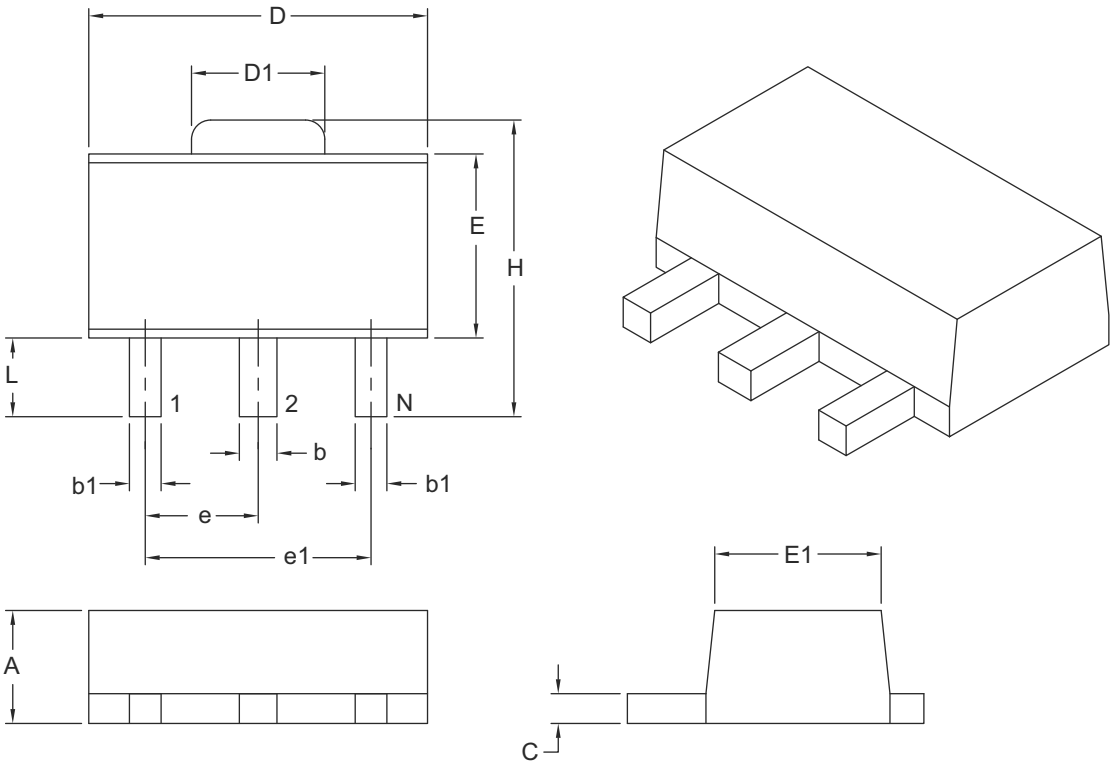
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2130A

3-Lead Plastic Small Outline Transistor Header (MB) [SOT-89]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS	
Dimension Limits		MIN	MAX
Number of Leads	N	3	
Pitch	e	1.50 BSC	
Outside Lead Pitch	e1	3.00 BSC	
Overall Height	A	1.40	1.60
Overall Width	H	3.94	4.25
Molded Package Width at Base	E	2.29	2.60
Molded Package Width at Top	E1	2.13	2.29
Overall Length	D	4.39	4.60
Tab Length	D1	1.40	1.83
Foot Length	L	0.79	1.20
Lead Thickness	c	0.35	0.44
Lead 2 Width	b	0.41	0.56
Leads 1 & 3 Width	b1	0.36	0.48

Notes:

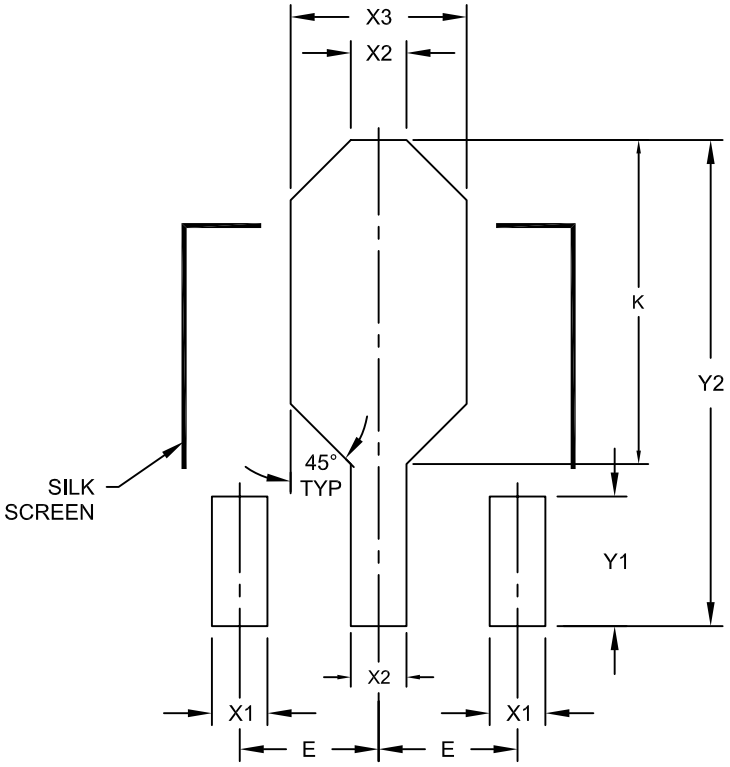
1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-029B

3-Lead Plastic Small Outline Transistor Header (MB) [SOT-89]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.50 BSC		
Contact Pads 1 & 3 Width	X1			0.48
Contact Pad 2 Width	X2			0.56
Heat Slug Pad Width	X3			1.20
Contact Pads 1 & 3 Length	Y1		1.40	
Contact 2 Pad Length	Y2			4.25
-	K	2.60		2.85

Notes:

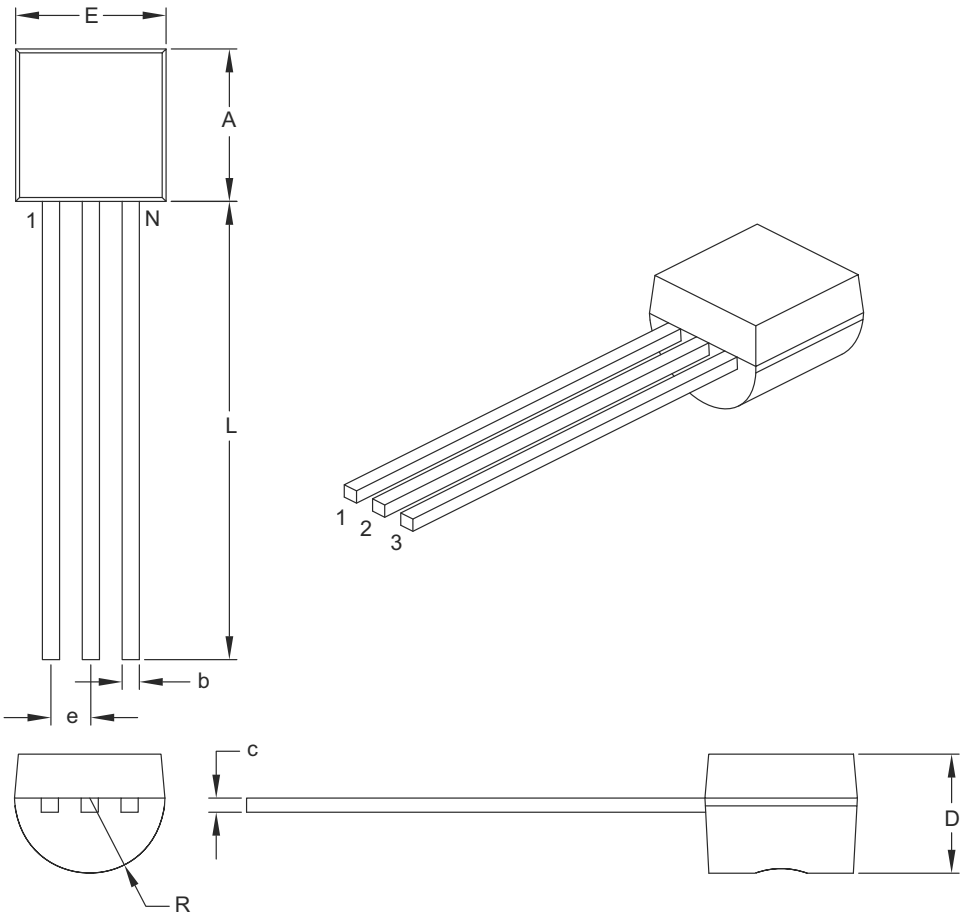
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2029A

3-Lead Plastic Transistor Outline (TO) [TO-92]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES	
Dimension Limits		MIN	MAX
Number of Pins	N	3	
Pitch	e	.050 BSC	
Bottom to Package Flat	D	.125	.165
Overall Width	E	.175	.205
Overall Length	A	.170	.210
Molded Package Radius	R	.080	.105
Tip to Seating Plane	L	.500	–
Lead Thickness	c	.014	.021
Lead Width	b	.014	.022

Notes:

1. Dimensions A and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-101B

APPENDIX A: REVISION HISTORY

Revision E (November 2010)

The following is the list of modifications:

1. Updated the Thermal Resistance Typical value for the SOT-89 package in the Junction Temperature Estimate section.

Revision D (June 2009)

The following is the list of modifications:

1. **DC Characteristics table**: Updated the V_{OUT} Temperature Coefficient's maximum value.
2. **Section 7.0 "Packaging Information"**: Updated package outline drawings.

Revision C (November 2008)

The following is the list of modifications:

1. **DC Characteristics table:** Added row to Output Voltage Regulation for 1% custom part.
2. **Temperature Specifications table:** Numerous changes to table.
3. Added Note 2 to **Temperature Specifications table**.
4. **Section 5.0 "Functional Description"**, **Section 5.2 "Output"**: Added second paragraph.
5. **Section 7.0 "Packaging Information"**: Added 1% custom part information to this section. Also, updated package outline drawings.
6. **Product Identification System**: Added 1% custom part information to this page.

Revision B (May 2007)

The following is the list of modifications:

1. All Pages: Corrected minor errors in document.
2. Page 4: Added junction-to-case information to Temperature Specifications table.
3. Page 16: Updated Package Outline Drawings in **Section 7.0 "Packaging Information"**.
4. Page 21: Updated Revision History.
5. Page 23: Corrected examples in **Product Identification System**.

Revision A (September 2006)

- Original Release of this Document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X-	XX	X	X	X/	XX
Device	Tape and Reel	Output Voltage	Feature Code	Tolerance	Temp.	Package

Device:	MCP1702: 2 µA Low Dropout Positive Voltage Regulator
Tape and Reel:	T = Tape and Reel
Output Voltage *:	12 = 1.2V “Standard” 15 = 1.5V “Standard” 18 = 1.8V “Standard” 25 = 2.5V “Standard” 28 = 2.8V “Standard” 30 = 3.0V “Standard” 33 = 3.3V “Standard” 40 = 4.0V “Standard” 50 = 5.0V “Standard” *Contact factory for other output voltage options.
Extra Feature Code:	0 = Fixed
Tolerance:	2 = 2.0% (Standard) 1 = 1.0% (Custom)
Temperature:	E = -40°C to +125°C
Package Type:	CB = Plastic Small Outline Transistor (SOT-23A) (equivalent to EIAJ SC-59), 3-lead, MB = Plastic Small Outline Transistor Header, (SOT-89), 3-lead TO = Plastic Transistor Outline (TO-92), 3-lead

Examples:

a) MCP1702T-1202E/CB: 1.2V LDO Positive Voltage Regulator, SOT-23A-3 pkg.

b) MCP1702T-1802E/MB: 1.8V LDO Positive Voltage Regulator, SOT-89-3 pkg.

c) MCP1702T-2502E/CB: 2.5V LDO Positive Voltage Regulator, SOT-23A-3 pkg.

d) MCP1702T-3002E/CB: 3.0V LDO Positive Voltage Regulator, SOT-23A-3 pkg.

e) MCP1702T-3002E/MB: 3.0V LDO Positive Voltage Regulator, SOT-89-3 pkg.

f) MCP1702T-3302E/CB: 3.3V LDO Positive Voltage Regulator, SOT-23A-3 pkg.

g) MCP1702T-3302E/MB: 3.3V LDO Positive Voltage Regulator, SOT-89-3 pkg.

h) MCP1702T-4002E/CB: 4.0V LDO Positive Voltage Regulator, SOT-23A-3 pkg.

i) MCP1702-5002E/TO: 5.0V LDO Positive Voltage Regulator, TO-92 pkg.

j) MCP1702T-5002E/CB: 5.0V LDO Positive Voltage Regulator, SOT-23A-3 pkg.

k) MCP1702T-5002E/MB: 5.0V LDO Positive Voltage Regulator, SOT-89-3 pkg.

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