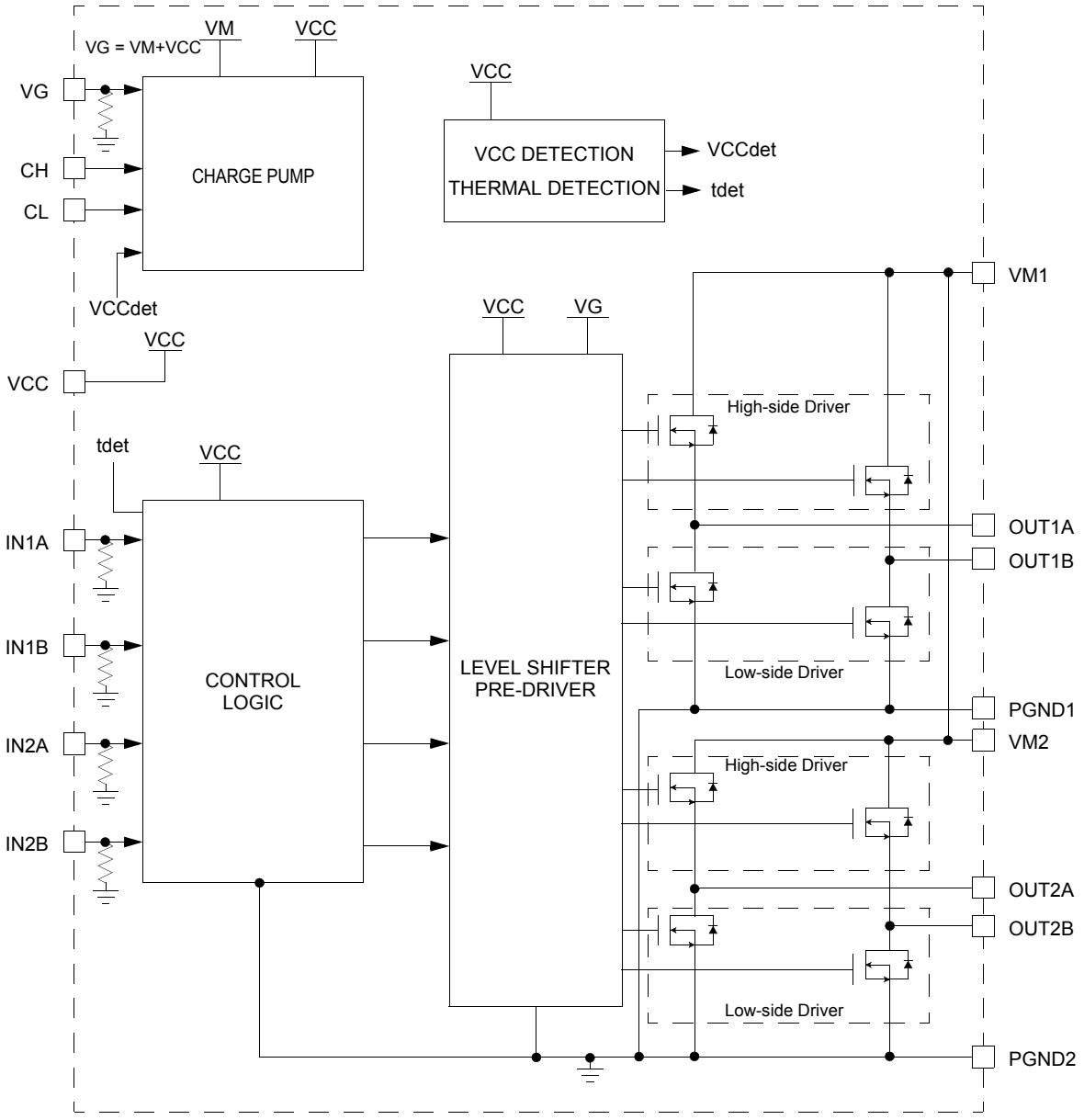
## INTERNAL BLOCK DIAGRAM




* VM1 and VM2 are connected internally. Both VM1 and VM2 must be tied together on the PCB.
PGND1 and PGND2 are connected internally. Both PGND1 and PGND2 must be tied together on the PCB.

**Figure 2. 34933 Simplified Internal Block Diagram**

# PIN CONNECTIONS

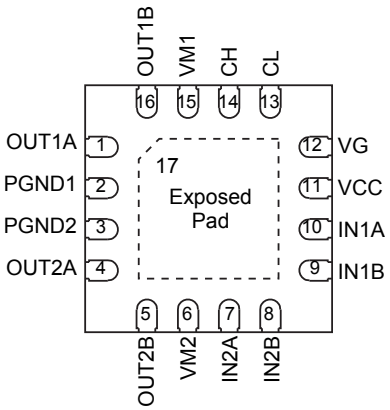



**Figure 3. 34933 Pin Connections**

**Table 1. 34933 Pin Definitions**

| Pin Number | Pin Name | Pin Function | Formal Name | Definition |
|---|---|---|---|---|
| 1 | OUT1A | Output | H-Bridge Output 1A | Output A of H-Bridge channel 1. |
| 2 | PGND1 | Power supply | Power Ground 1 | Power supply grounds for the 34933 device. Refer to the application diagram for recommended layout. |
| 3 | PGND2 | Power supply | Power Ground 2 | Power supply grounds for the 34933 device. Refer to the application diagram for recommended layout. |
| 4 | OUT2A | Output | H-Bridge Output 2A | Output A of H-Bridge channel 2 |
| 5 | OUT2B | Output | H-Bridge Output 2B | Output B of H-Bridge channel 2 |
| 6 | VM2 | Power supply | Motor Drive Power Supply 2 | Power supply pins for the 34933 motor drive circuitry. Refer to the application diagram for recommended layout. |
| 7 | IN2A | Input | Logic Input Control 2A | Logic input control of OUT2A |
| 8 | IN2B | Input | Logic Input Control 2B | Logic input control of OUT2B |
| 9 | IN1B | Input | Logic Input Control 1B | Logic input control of OUT1B |
| 10 | IN1A | Input | Logic Input Control 1A | Logic input control of OUT1A |
| 11 | VCC | Power supply | Control Logic Power Supply | Power supply for the control logic circuitry. |
| 12 | VG | Output | Charge Pump Output Capacitor | Charge pump output pin connected to an external capacitor. The $V_G$ voltage is the sum of the $V_{CC}$ and $V_M$ power supplies. |
| 13 | CL | Input/Output | Charge Pump Capacitor 1 | Low-side charge pump capacitor connection |
| 14 | CH | Input/Output | Charge Pump Capacitor 2 | High-side charge pump capacitor connection |
| 15 | VM1 | Power supply | Motor Drive Power Supply 1 | Power Supply pins for the 34933 motor drive circuitry. Refer to the application diagram for recommended layout. |
| 16 | OUT1B | Output | H-Bridge Output 1B | Output B of H-Bridge channel 1 |
| 17[(1)] | Exposed Pad | Power supply | EP | The exposed pad is connected to ground plane via the exposed pad solder pad. Note the primary purpose of the exposed pad for 34933 is thermal heat dissipation. Therefore, adequate thermal vias should be included in the PCB design. |

Notes
1. Exposed pad is used as a heat sink. Connect it to the power ground through four thermal vias where the area is wide.

# ELECTRICAL CHARACTERISTICS

## MAXIMUM RATINGS

**Table 2. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings | Symbol | Value | Unit |
|---|---|---|---|
| **ELECTRICAL RATINGS** | | | |
| Control Logic Power Supply Voltage | VCC | -0.5 to +6.0 | V |
| Motor Drive Power Supply | VM | -0.5 to +7.5 | V |
| VCC Level Pin Voltage - IN1A, IN1B, IN2A, IN2B | Vpin1 | -0.5 to +5.5 | V |
| VM Level Pin Voltage - OUT1A, OUT1B, OUT2A, OUT2B, CL | Vpin2 | -0.5 to +7.5 | V |
| VM+VCC Level Pin Voltage - CH, VG | Vpin3 | -0.5 to +13.5 | V |
| Motor Drive Maximum Load Current, $T_A$ = 85 °C | $I_{LOAD\_DC\_MD}$ | 0.7 | A |
| Motor Drive Maximum Load Current, $T_A$ = 25 °C | $I_{LOAD\_DC\_MD}$ | 1.0 | A |
| Motor Drive Maximum Peak Load Current[3] | $I_{LOAD\_PEAK\_MD}$ | 1.4 | A |
| Power Dissipation[4] | $P_D$ | 1.0 | W |
| ESD Voltage[2]<br>Human Body Model (HBM)<br>Machine Model (MM)<br>Charge Device Model (CDM) | $V_{ESD}$ | <br>±4000<br>±350<br>±1000 | V |
| **THERMAL RATINGS** | | | |
| Operating Temperature Range | $T_A$ | -20 to +85 | °C |
| Operating Junction Temperature | $T_J$ | 150 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 to +150 | °C |
| **THERMAL RESISTANCE** | | | |
| Thermal Resistance, Junction to Case[5] | $R_{\theta JC}$ | 23 | °C/W |
| Peak Package Reflow Temperature During Reflow[6], [7] | $T_{PPRT}$ | Note 7 | °C |

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω), the Machine Model (MM) ($C_{ZAP}$ = 200 pF, $R_{ZAP}$ = 0 Ω), and the Charge Device Model (CDM), Robotic ($C_{ZAP}$ = 4.0 pF).
3. Peak time is for 10 ms pulse width at 200 ms intervals. $T_A$ = 25°C.
4. $R_{\theta JA}$ = 50 °C/W, in case of 2s2p printed circuit board that defined on SEMI JEDEC JESD51- 3 and JESD51-6.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

## STATIC AND DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 3. Static and Dynamic Electrical Characteristics**

Characteristics noted under conditions, VM = 5.0 V, VCC = 3.0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{A=}$ 25 °C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | |
| Motor Drive Power Supply Voltage | $V_M$ | 2.0 | 5.0 | 7.0 | V |
| Control Logic Power Supply Voltage | $V_{CC}$ | 2.7 | 3.0 | 5.5 | V |
| Driver Quiescent Supply Current (IN1A, IN1B,IN2A, IN2B = L)<br>No Signal Input | $I_{QM}$ | -<br>- | 72<br>- | 100<br>- | uA |
| Logic Quiescent Supply Current (IN1A, IN1B, IN2A, IN2B = L)<br>No Signal Input | $I_{QVCC}$ | -<br>- | 114<br>- | 400<br>- | uA |
| Control Logic Power Supply Operating Current (IN1A, IN2A = L, IN1B, IN2B = 200kHz) | $I_{VCC}$ | - | 350 | 800 | uA |
| Charge Pump Target Voltage<br>VM = 2.0 V, VCC = 2.7 V, $I_{LOAD=}$ 0A<br>VM = 5.0 V, VCC = 3.0 V, $I_{LOAD=}$ 0A<br>VM = 7.0 V, VCC = 5.5 V, $I_{LOAD=}$ 0A | $V_G$ | <br>4.2<br>7.6<br>12.0 | <br>4.45<br>7.8<br>12.3 | <br>4.7<br>8.0<br>12.5 | V |
| Charge Pump Wake-up Time<br>Charge pump is enabled in $V_{CC} > V_{CCDET}$ | $T_{VGON}$ | - | 130 | 400 | us |
| Driver Quiescent Supply Current at VCCDET = L<br>$V_M$ = 5.0 V, $V_{CC=}$ 0 V | $I_{QM\_VCD = L}$ | - | - | 1.0 | uA |
| Charge Pump Switching Frequency | $F_{QP}$ | - | 150 | - | kHz |
| **H-BRIDGE DRIVER** | | | | | |
| H-Bridge Driver High/Low-side Driver On-Resistance 1<br>$V_{CC}$ = 2.7 V, $I_{SINK}$ = 100 mA, $T_{A=}$ 25 °C | $R_{ON1}$ | - | 0.4 | 0.45 | Ω |
| H-Bridge Driver High/Low-side Driver On-Resistance 2 (8)<br>$V_{CC}$ = 2.7 V, $I_{SINK}$ = 700 mA, $T_{A=}$ 25 °C | $R_{ON2}$ | - | 0.43 | 0.51 | Ω |
| H-Bridge Driver High/Low-side Driver On-Resistance 3 (8)<br>$V_{CC}$ = 2.7 V, $I_{SINK}$ = 700 mA, $T_{A=}$ 85 °C | $R_{ON3}$ | - | 0.51 | 0.62 | Ω |
| H-Bridge Driver High/Low-side Driver On-Resistance 4<br>$V_{CC}$ = 3.0 V, $I_{SINK}$ = 100 mA, $T_{A=}$ 25 °C | $R_{ON4}$ | - | 0.39 | 0.43 | Ω |
| H-Bridge Driver High/Low-side Driver On-Resistance 5 (8)<br>$V_{CC}$ = 3.0 V, $I_{SINK}$ = 700 mA, $T_{A=}$ 25 °C | $R_{ON5}$ | - | 0.41 | 0.48 | Ω |
| H-Bridge Driver High/Low-side Driver On-Resistance 6 (8)<br>$V_{CC}$ = 3.0 V, $I_{SINK}$ = 700 mA, $T_{A=}$ 85 °C | $R_{ON6}$ | - | 0.49 | 0.58 | Ω |
| H-Bridge Driver Output Body Diode Forward Voltage<br>$I_f$ = 100 mA | $V_F$ | - | 0.8 | 1.2 | V |
| Input Pulse Frequency (INA/B)<br>Duty of input signal = 50 % | $F_{IN}$ | - | - | 200 | kHz |

Notes
8. Guaranteed by design

**Table 3. Static and Dynamic Electrical Characteristics**

Characteristics noted under conditions, VM = 5.0 V, VCC = 3.0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **H-BRIDGE DRIVER (CONTINUED)** | | | | | |
| H-Bridge Output Propagation Delay Time for OUTA/B (H to L)<br>$R_{LOAD}$ = (1.0 kΩ) between OUTA and OUTB (refer to Figure 4) (IN1A, IN2A = L, IN1B, IN2B = 200 kHz) | $t_{PDHL}$ | - | 0.1 | 0.5 | us |
| H-Bridge Output Propagation Delay Time for OUTA/B (L to H)<br>Rload = (1.0 k Ω) between OUTA and OUTB (refer to Figure 4) (IN1A, IN2A = L, IN1B, IN2B = 200 kHz) | $t_{PDLH}$ | - | 0.1 | 0.5 | us |
| H-Bridge Output Pulse Width<br>$R_{LOAD}$ = 20 Ω between OUTA and OUTB, Input Pulse Width = 1.0 μs, 50% to 50%, $t_{PW}$: 50% to 50% (refer to Figure 5) | $t_{PW}$ | 0.7 | - | - | us |
| H-Bridge Output Propagation Delay Time (Hi-Z to H) (8)<br>$R_{LOAD}$ = 100 kΩ to 1/2*VM, $C_{LOAD}$ = 0 pF, $t_{PDZH}$ 50% to 75% | $t_{PDZH}$ | - | - | 0.5 | us |
| H-Bridge Output Propagation Delay- Time (H to Hi-Z) (8)<br>$R_{LOAD}$ = 100 kΩ to 1/2*VM, $C_{LOAD}$ = 0 pF, $t_{PDHZ}$ 75% to 50% | $t_{PDHZ}$ | - | - | 2.0 | us |
| **CONTROL LOGIC** | | | | | |
| High Level Input Voltage (IN1A, IN1B, IN2A, IN2B)<br>$V_{CC}$ = 2.7 V ~ 5.5 V | $V_{IH}$ | $V_{CC}$x0.7 | - | - | V |
| Low Level Input Voltage (IN1A, IN1B, IN2A, IN2B)<br>$V_{CC}$ = 2.7 V ~ 5.5 V | $V_{IL}$ | - | - | $V_{CC}$x0.3 | V |
| High Level Input Current (IN1A, IN1B, IN2A, IN2B)<br>$V_{TERMAINAL1}$ = 3.0 V | $I_{IH}$ | 9 | - | 20 | uA |
| Low Level Input Current (IN1A, IN1B, IN2A, IN2B)<br>$V_{CC}$ = 2.7 V to 5.5 V | $I_{IL}$ | -1.0 | - | - | uA |
| Input Pulse Rise Time (IN1A, IN1B, IN2A, IN2B)<br>$V_{CC}$ = 2.7 V to 5.5 V | $t_R$ | - | - | 1.0 | us |
| Input Pulse Fall Time (IN1A, IN1B, IN2A, IN2B)<br>$V_{CC}$ = 2.7 V to 5.5 V | $t_F$ | - | - | 1.0 | us |
| **DETECTOR** | | | | | |
| VCC Detection Voltage (refer to Figure 6) | $V_{CCDET}$ | 2.0 | 2.2 | 2.4 | V |
| VCC Detection hysteresis Voltage (refer to Figure 6) | $V_{CCDETHYS}$ | 0.05 | 0.1 | 0.3 | V |
| Thermal Detection Temperature (9) | $T_{DET}$ | 150 | 170 | 190 | °C |
| Thermal Detection Hysteresis Temperature (9) | $T_{DETHYS}$ | 10 | 20 | 30 | °C |

Notes

9. Guaranteed by design

## *TIMING DIAGRAMS*

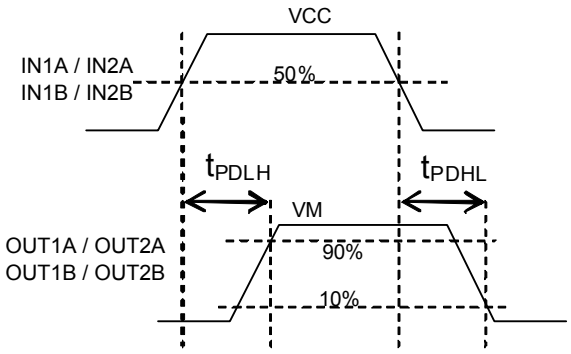



**Figure 4. $t_{PDLH}$ and $t_{PDHL}$ Timing**

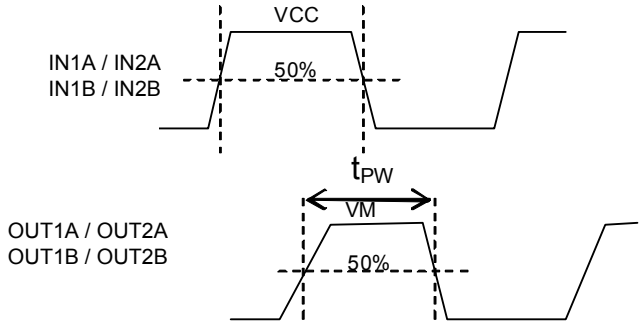



**Figure 5. $t_{PW}$ Timing**

**Table 4. Truth Table**

| | | INPUT | | OUTPUT | |
|---|---|---|---|---|---|
| Vccdet | Tdet | IN1A<br>IN2A | IN1B<br>IN2B | OUT1A<br>OUT2A | OUT1B<br>OUT2B |
| L | X | X | X | Z | Z |
| H | L | L | L | L | L |
| H | L | H | L | H | L |
| H | L | L | H | L | H |
| H | L | H | H | Z | Z |
| H | H | X | X | Z | Z |

H - High
L - Low
Z - High-impedance
X - Don't Care

Figure 6 and Figure 7 show the timing charts of input and output signals

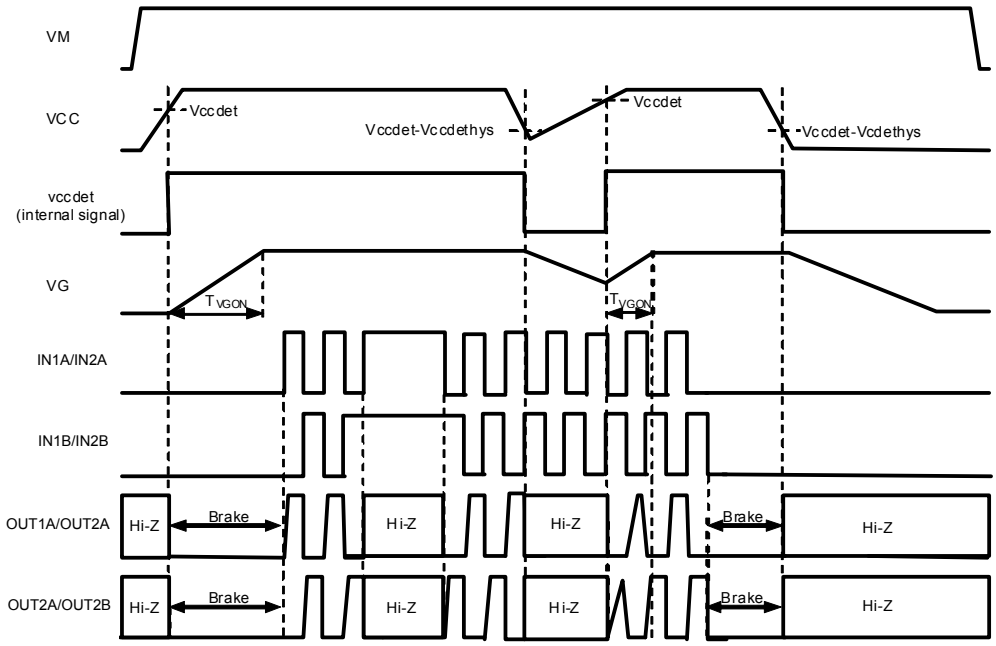



**Figure 6. Timing Chart of Input and Output Signal ($V_{CCDET}$ case)**

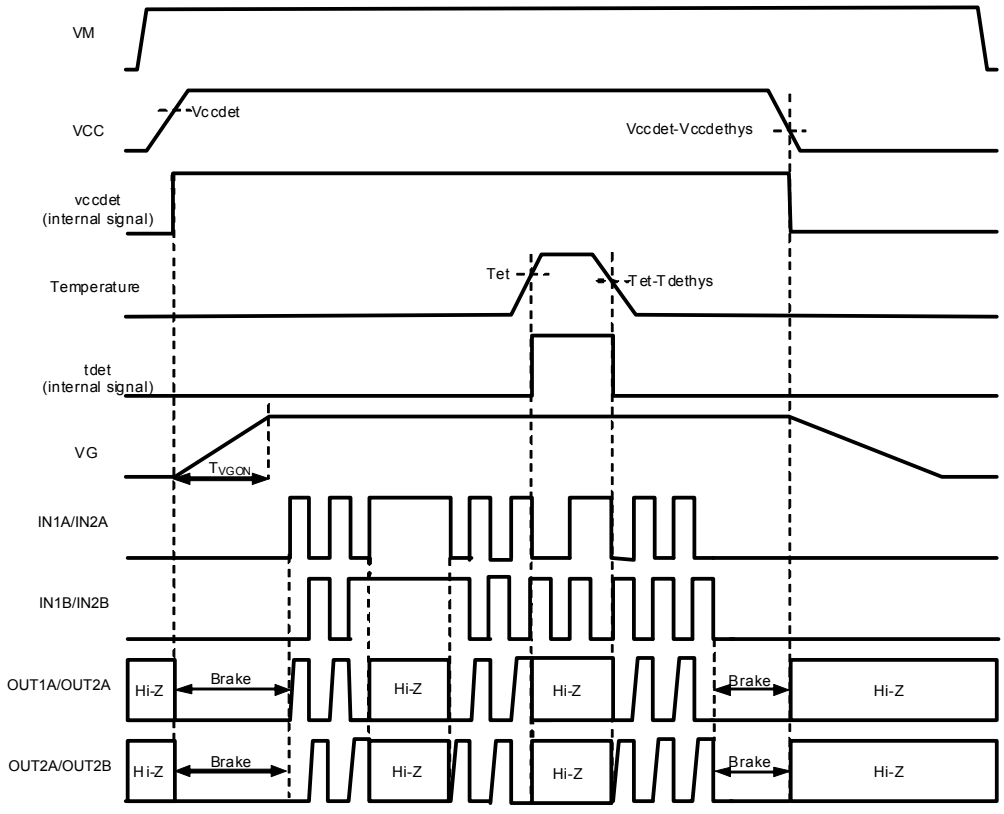



**Figure 7. Timing Chart of Input and Output Signal ($t_{DET}$ case)**

# FUNCTIONAL DESCRIPTION

## *FUNCTIONAL PIN DESCRIPTION*

### LOGIC SUPPLY (VCC)

The VCC pin carries the logic supply voltage and current into the logic sections of the IC. VCC has an under-voltage threshold. If the supply voltage drops below the under-voltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

### LOGIC INPUT CONTROL (IN1A, IN1B, IN2A, AND IN2B)

These logic input pins control each H-Bridge output. IN1A logic HIGH = OUT1A HIGH. However, if all inputs are HIGH, the output bridges are both tri-stated (refer to Table 4, Truth Table).

### H-BRIDGE OUTPUT (OUT1A, OUT1B, OUT2A, AND OUT2B)

These pins provide connection to the outputs of each of the internal H-Bridges (See Figure 2, 34933 Simplified Internal Block Diagram).

### MOTOR DRIVE POWER SUPPLY (VM1 AND VM2)

The VM pins carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the loads attached between the output pins. All VM pins must be connected together on the Printed Circuit Board (PCB).

### CHARGE PUMP (CL AND CH)

These two pins, the CL and CH, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μF.

### POWER GROUND (PGND)

Power ground pins must be tied together on the PCB and connected to the common ground plane.

### LOGIC GROUND (EXPOSED PAD)

The Exposed Pad is connected to the PCB Ground plane through vias by soldering. Note the primary purpose of the Exposed pad for 34933 is thermal heat dissipation. Therefore, adequate thermal vias should be included in the PCB design. The exposed pad should be connected to the common ground plane.

## *VOLTAGE DETECTION AND THERMAL LIMIT DETECTION*

The 34933 has the VCC Low Voltage Detection (Vccdet) and the Thermal Detection ($T_{DET}$). VCC Low Voltage Detection is designed to shutdown of IC functions when VCC becomes lower than specified voltage. Thermal Detection operates when the IC temperature exceeds specified value and stop H-Bridge operation. Table 5 shows block status of 34933 by each condition. VCC is the control logic power supply for 34933. The system begins to operate when $V_{CC}$ > $V_{CCDET}$ (Typ. 2.2 V).

**Table 5. Block Status**

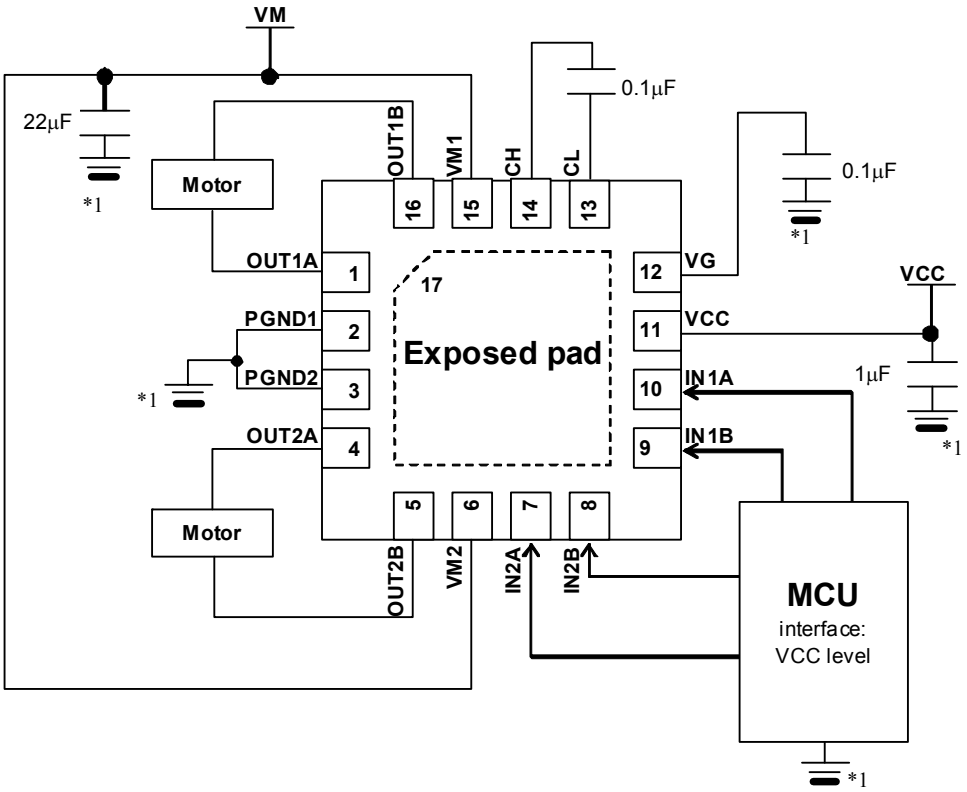
| Operation mode | Vccdet | Tdet | Charge Pump | H-Bridge Driver |
|---|---|---|---|---|
| 1 | L | X | Disable | Disable |
| 2 | H | L | Enable | Enable |
| 3 | H | H | Enable | Disable |

H - High
L - Low
X - Don't Care

# TYPICAL APPLICATION

Figure 8 shows a typical application using the 34933. The internal charge pump of this device is powered from the $V_{CC}$ supply. Therefore, care must be taken to ensure $V_{CC}$ is a high enough value to provide sufficient gate-source voltage for the high-side MOSFETs when $V_M > V_{CC}$ (e.g., $V_M$ = 5.0 V, $V_{CC}$ = 3.0 V), in order to ensure full enhancement of the high-side MOSFET channels.

The 34933 can be configured in several applications. The figure below shows the 34933 in a typical Slave Node Application.




*1 - It is recommend to use low resistance copper PCB traces between VM & VCC ground and the PGND1/PGND2 pins.

**Figure 8. Typical Application**

# PCB LAYOUT

When designing a printed circuit board (PCB), connect sufficient capacitance between power supplies (VM & VCC) and ground pins to ensure proper filtering from transients. For all high-current paths, use wide copper traces and the shortest possible distances. Note that capacitors should be placed as close to the 34933 as possible to maximize the filtering capability of each capacitor.

Additionally, care must be taken to avoid CEMF spikes induced when inductive currents accumulate at the VM supply. The typical method of snubbing inductive spikes includes connecting a Zener diode or capacitor at the supply pin (VM).

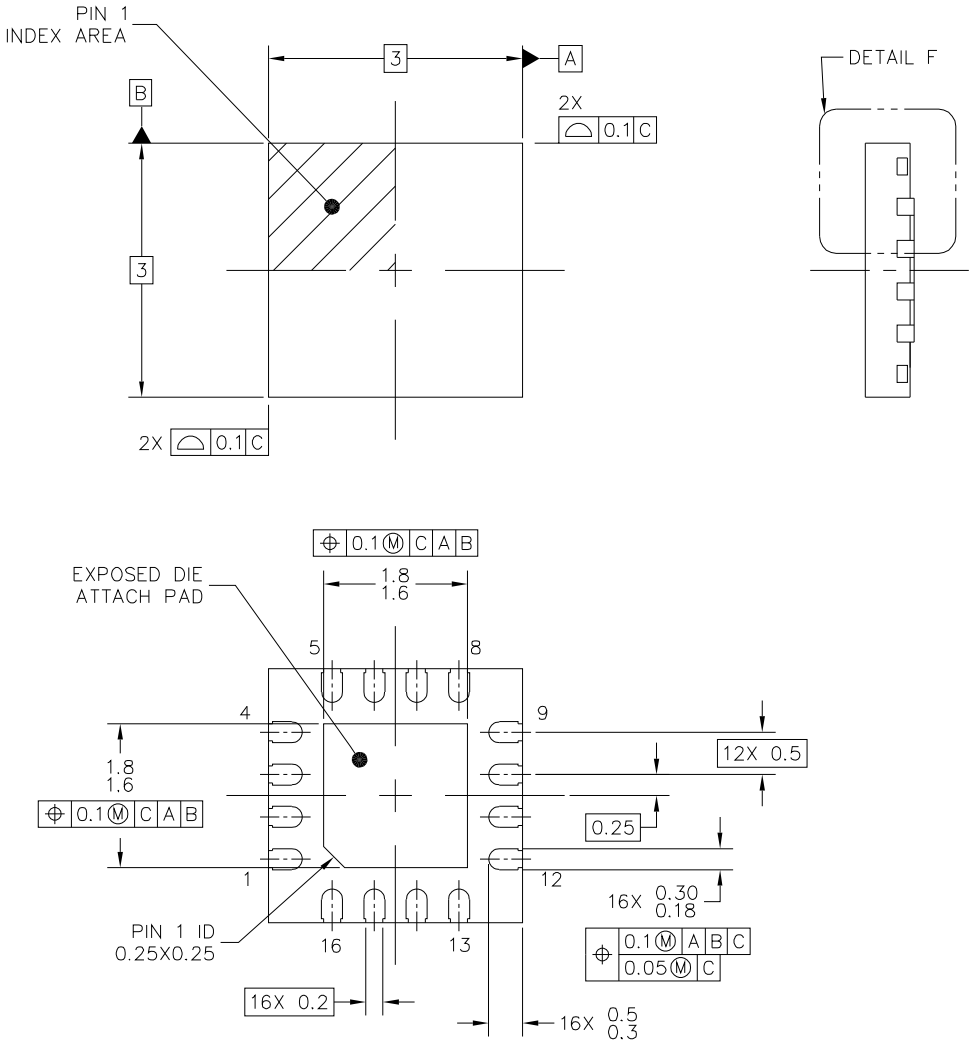
# PACKAGING

## PACKAGE DIMENSIONS

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing's document number.

**Table 6.**

| Package | Suffix | Package Outline Drawing Number |
|---|---|---|
| 16-PIN UQFN | EP | 98ASA00717D |

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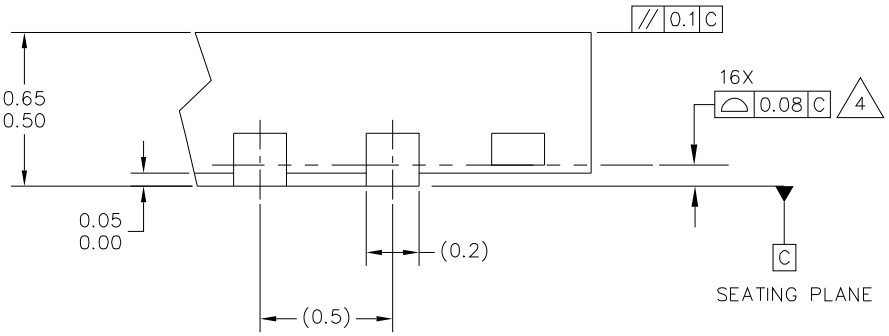
|---|---|---|
| TITLE: QFN, THERMALLY ENHANCED, 3 X 3 X 0.58, 0.5 PITCH, 16 TERMINAL | DOCUMENT NO: 98ASA00717D | REV: O |
| | STANDARD: NON-JEDEC | |
| | 21 APR 2014 | |

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| | STANDARD: NON-JEDEC | |
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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

| | | |
|---|---|---|
|  | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
| TITLE: QFN, THERMALLY ENHANCED, 3 X 3 X 0.58, 0.5 PITCH, 16 TERMINAL | DOCUMENT NO: 98ASA00717D | REV: O |
| | STANDARD: NON–JEDEC | |
| | 21 APR 2014 | |

# REVISION HISTORY

| REVISION | DATE | DESCRIPTION OF CHANGES |
|---|---|---|
| 2.0 | 7/2010 | • Initial Release. |
| | 12/2013 | • No technical changes<br>• Revised back page<br>• Updated document properties |
| 3.0 | 9/2014 | • Changed 98A to 98ASA00717D<br>• Update format |

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9/2014