ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .... -0.3V to 6V
$\overline{SHDN}$ to GND .... -0.3V to 6V
All Other Pins to GND .... -0.3V to (V_{DD} + 0.3V)
Continuous Current
  V_{DD}, GND, OUT_ .... ±750mA
IN_, $\overline{SHDN}$, BIAS, GAIN, TON .... ±20mA
OUT_ Short Circuit to GND or V_{DD} Duration .... Continuous
OUT+ to OUT- Short Circuit Duration .... Continuous
Continuous Power Dissipation (T_A = +70°C)
  WLP (derate 11.9mW/°C above +70°C) 848mW
Junction Temperature .... +150°C
Operating Temperature Range .... -40°C to +85°C
Storage Temperature Range .... -65°C to +150°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
  Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 94°C/W
  Junction-to-Case Thermal Resistance (θ_{JC}) .... 41°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.7V, V_{GND} = 0V, $\overline{SHDN}$ = V_{DD}, GAIN = V_{DD} (0dB), C_{BIAS} = 0.1µF, C_{IN} = 0.47µF, no load: R_{IN} = R_F = 10kΩ (MAX98309), T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR test		2.5		5.5	V
Undervoltage Lockout	UVLO	V_{DD} falling			1.8	2.3	V
Quiescent Supply Current	I_{VDD}	$\overline{SHDN}$ = V_{DD}	V_{DD} = 3.7V		1.2		mA
			V_{DD} = 5V		1.9	1.8	
Shutdown Supply Current	I_{VDD_SD}	$V_{\overline{SHDN}}$ = 0V, T_A = +25°C			2	3	µA
Turn-On Time	t_{ON}	MAX98309 shutdown to full operation	TON = GND		10	22.8	ms
			TON = V_{DD}		100		
		MAX98310 shutdown to full operation			5.7	11.5	
Gain	A_V	MAX98310	GAIN = V_{DD}	-0.25	0	+0.25	dB
			GAIN = GND	2.75	3	3.25	
			GAIN = unconnected	5.75	6	6.25	
			GAIN = BIAS	8.75	9	9.25	
Gain Selection Threshold		MAX98310	GAIN = V_{DD}	0.80 x V_{DD}			V
			GAIN = GND			0.05 x V_{DD}	
			GAIN = unconnected	0.16 x V_{DD}		0.24 x V_{DD}	
			GAIN = BIAS	0.35 x V_{DD}		0.69 x V_{DD}	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.7V, V_{GND} = 0V, $\overline{SHDN}$ = V_{DD}, GAIN = V_{DD} (0dB), C_{BIAS} = 0.1μF, C_{IN} = 0.47μF, no load: R_{IN} = R_F = 10kΩ (MAX98309), T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Input Resistance	R_{INDIFF}	MAX98309, $\overline{SHDN}$ = V_{DD}			1000		kΩ
		MAX98310	GAIN = 0dB		38.2		
			GAIN = 3dB		31.7		
			GAIN = 6dB		25.5		
Input Bias Current	I_{INBIAS}	MAX98309/MAX98310, $\overline{SHDN}$ = V_{DD}				±1	μA
Shutdown Input Bias Current	I_{INBIAS_SHDN}	$\overline{SHDN}$ = GND, IN_ = V_{DD} or IN_ = GND		-5		+5	μA
Output Offset Voltage	V_{OS}	T_A = +25°C (Note 3)			±0.2	±1	mV
Click-and-Pop Level	K_{CP}	R_L = 8Ω, 32 samples per second, A-weighted, T_A = +25°C (Notes 3, 4)	Into shutdown		-66		dBV
			Out of shutdown		-66		
Common-Mode Bias Voltage	V_{BIAS}	Voltage at BIAS		0.475 x V_{DD}	0.5 x V_{DD}	0.525 x V_{DD}	V
Input Common-Mode Voltage Range	V_{CM}	Inferred from CMRR test		0.5		V_{DD} - 0.6	V
Common-Mode Rejection Ratio	CMRR	MAX98310/MAX98310	Guaranteed over input common-mode voltage range	-50	-76		dB
			f_{IN} = 1kHz, R_L = 8Ω + 33μH		-62		
Power-Supply Rejection Ratio	PSRR	DC 2.5V to 5.5V		73	93		dB
		V_{RIPPLE} = 200mV_{P-P} (Note 3)	f_{IN} = 217Hz		90		
			f_{IN} = 1kHz		90		
			f_{IN} = 10kHz		72		
Output Power	P_{OUT}	V_{DD} = 3.7V, 1% THD+N	R_L = 8Ω + 68μH		0.750		W
			R_L = 4Ω + 33μH		1.2		
		V_{DD} = 3.7V, 10% THD+N	R_L = 8Ω + 68μH		0.9		
			R_L = 4Ω + 33μH		1.5		
		V_{DD} = 5V, 1% THD+N (Note 5)	R_L = 8Ω + 68μH		1.4		
			R_L = 4Ω + 33μH, thermally limited		2.1		
		V_{DD} = 5V, 10% THD+N (Note 5)	R_L = 8Ω + 68μH		1.7		
			R_L = 4Ω + 33μH, thermally limited		2.7		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.7V, V_{GND} = 0V, $\overline{SHDN}$ = V_{DD}, GAIN = V_{DD} (0dB), C_{BIAS} = 0.1µF, C_{IN} = 0.47µF, no load: R_{IN} = R_F = 10kΩ (MAX98309), T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

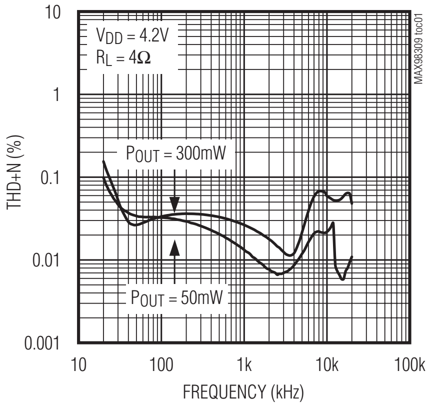
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz, BW = 22Hz to 22kHz	R_L = 8Ω + 68µH, P_{OUT} = 375mW		0.008		%
			R_L = 4Ω + 33µH, P_{OUT} = 750mW	0.06	0.02		
		f_{IN} = 6kHz, BW = 22Hz to 22kHz	R_L = 8Ω + 68µH, P_{OUT} = 375mW		0.01		
Signal-to-Noise Ratio	SNR	A-weighted, V_{DD} = 5V, P_{OUT} = 1.4W, R_L = 8Ω + 33µH			110		dB
Output Noise Voltage	V_N	A-weighted (Note 3)			9		µV
Overcurrent Protection Threshold					2		A
Thermal-Protection Threshold					+160		°C
Thermal-Protection Hysteresis					15		°C
Maximum Capacitive Load Drive	C_L	Bridge-tied load capacitance			500		pF
LOGIC INPUT ($\overline{SHDN}$, TON) (MAX98309)							
Input Logic-High	V_{IH}	1.8V logic compliant		1.4			V
Input Logic-Low	V_{IL}	1.8V logic compliant				0.4	V
Input Leakage Current High	I_{IH}	T_A = +25°C				1	µA
Input Leakage Current Low	I_{IL}	T_A = +25°C				1	µA

Note 2: All specifications are 100% tested at T_A = +25°C; temperature limits are guaranteed by design.
Note 3: Inputs AC-coupled to GND.
Note 4: Mode transitions controlled by $\overline{SHDN}$.
Note 5: Thermally limited by package.

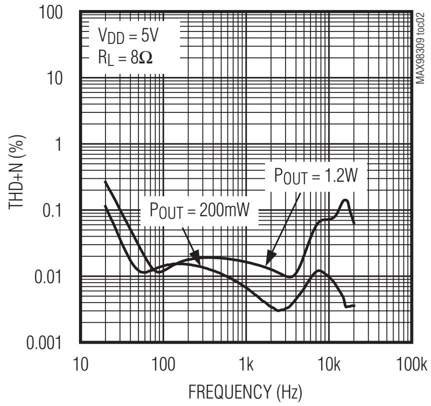
Typical Operating Characteristics

(V_{DD} = 3.7V, V_{GND} = 0V, $\overline{SHDN}$ = V_{DD}, GAIN = GND (R_F = R_{IN} = 10kΩ), C_{BIAS} = 0.1µF, C_{IN} = 1µF, no load, unless otherwise noted.)

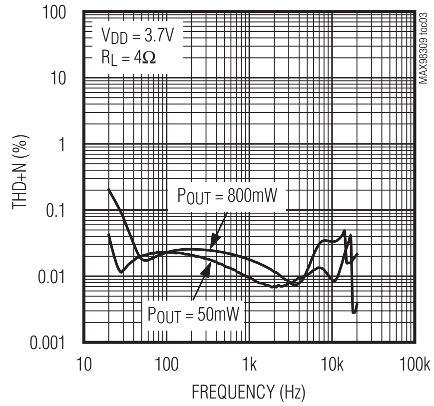
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



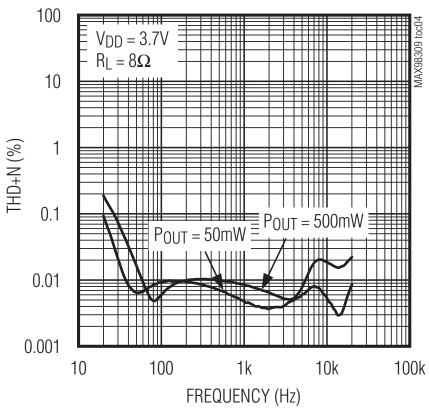
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



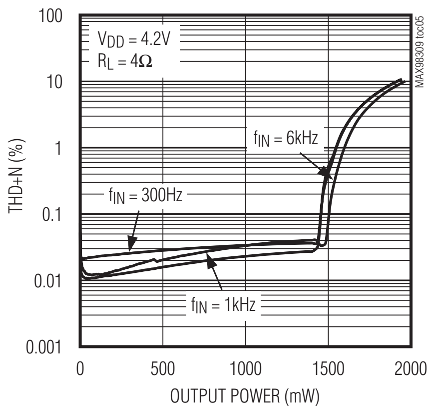
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



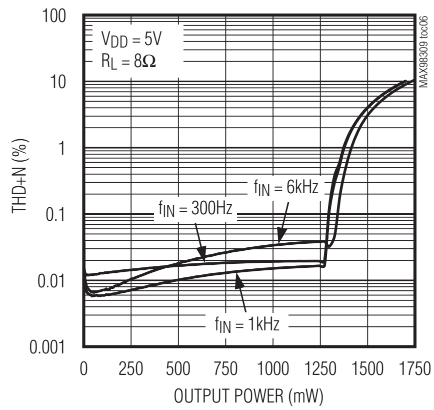
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



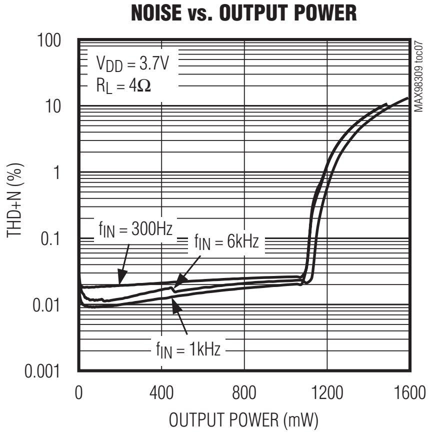
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



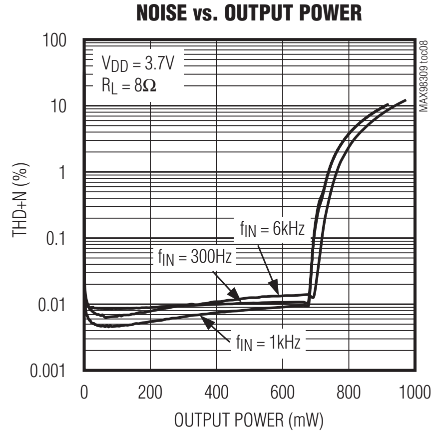
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



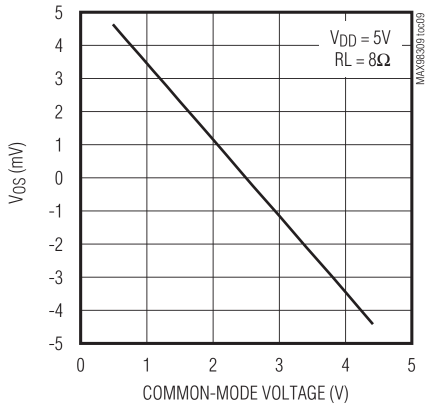
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



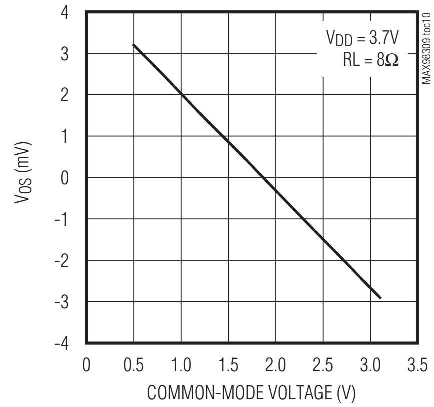
Typical Operating Characteristics (continued)

(V_{DD} = 3.7V, V_{GND} = 0V, $\overline{SHDN}$ = V_{DD}, GAIN = GND (R_F = R_{IN} = 10kΩ), C_{BIAS} = 0.1µF, C_{IN} = 1µF, no load, unless otherwise noted.)

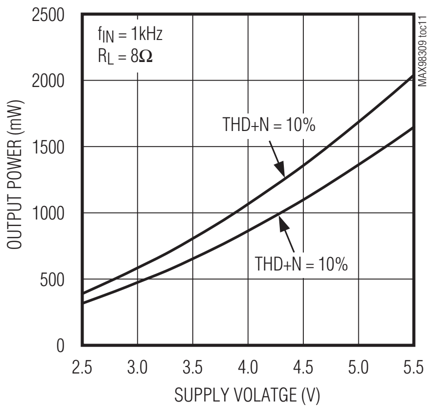
OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



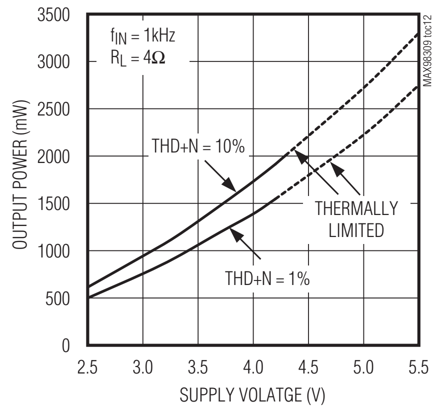
OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



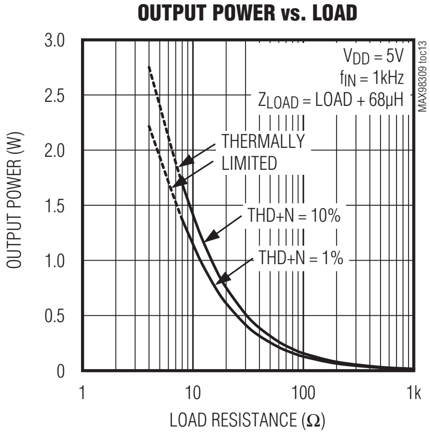
OUTPUT POWER vs. SUPPLY VOLTAGE



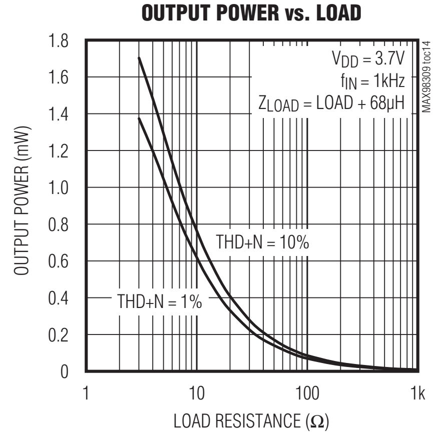
OUTPUT POWER vs. SUPPLY VOLTAGE



OUTPUT POWER vs. LOAD



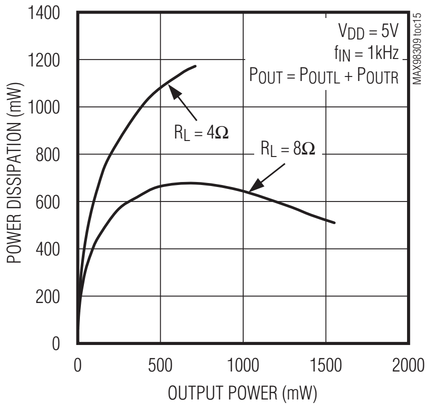
OUTPUT POWER vs. LOAD



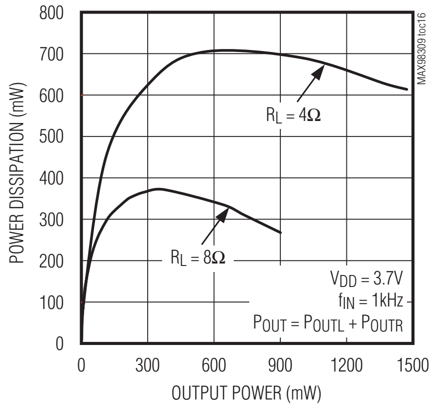
Typical Operating Characteristics (continued)

(V_{DD} = 3.7V, V_{GND} = 0V, $\overline{SHDN}$ = V_{DD}, GAIN = GND (R_F = R_{IN} = 10kΩ), C_{BIAS} = 0.1µF, C_{IN} = 1µF, no load, unless otherwise noted.)

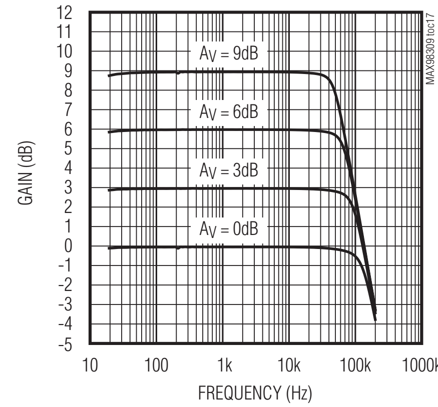
POWER DISSIPATION vs. OUTPUT POWER



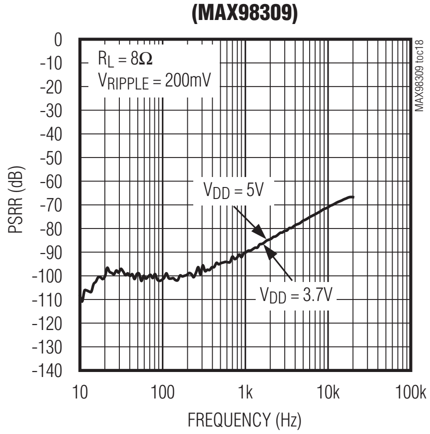
POWER DISSIPATION vs. OUTPUT POWER



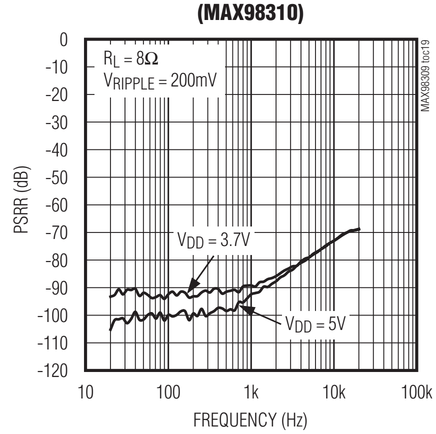
GAIN vs. FREQUENCY (MAX98310)



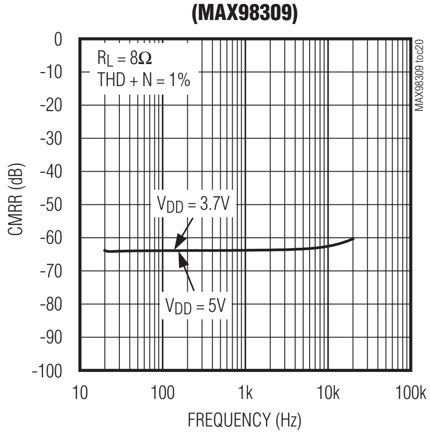
PSRR vs. FREQUENCY (MAX98309)



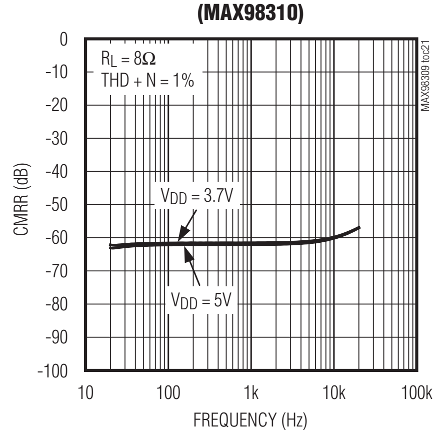
PSRR vs. FREQUENCY (MAX98310)



CMRR vs. FREQUENCY (MAX98309)



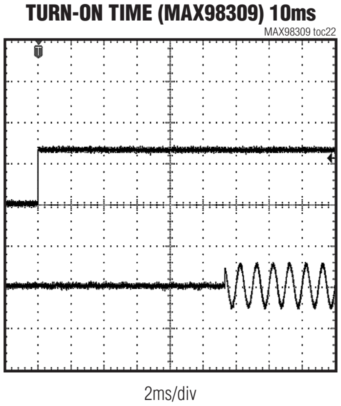
CMRR vs. FREQUENCY (MAX98310)



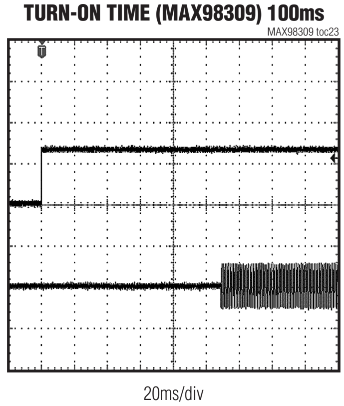
Typical Operating Characteristics (continued)

(V_{DD} = 3.7V, V_{GND} = 0V, $\overline{SHDN}$ = V_{DD}, GAIN = GND (R_F = R_{IN} = 10kΩ), C_{BIAS} = 0.1µF, C_{IN} = 1µF, no load, unless otherwise noted.)

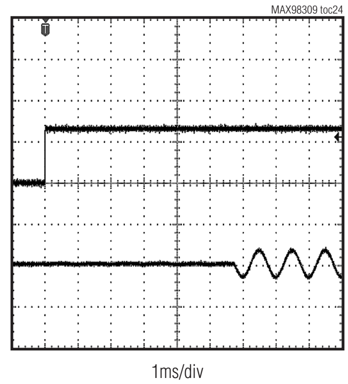
TURN-ON TIME (MAX98309) 10ms



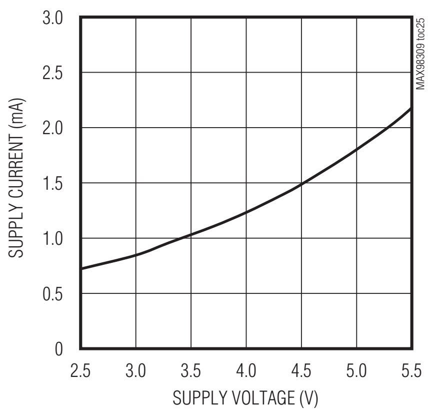
TURN-ON TIME (MAX98309) 100ms



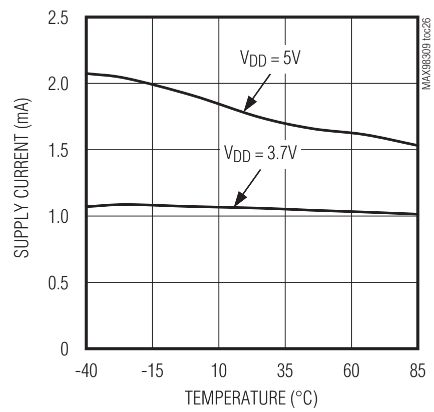
TURN-ON TIME MAX98310



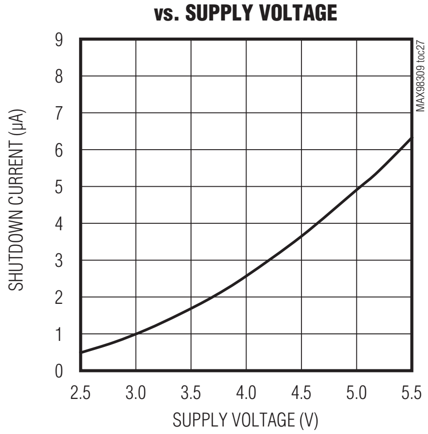
SUPPLY CURRENT vs. SUPPLY VOLTAGE



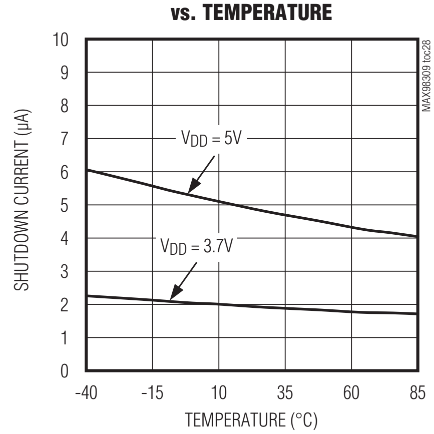
SUPPLY CURRENT vs. TEMPERATURE



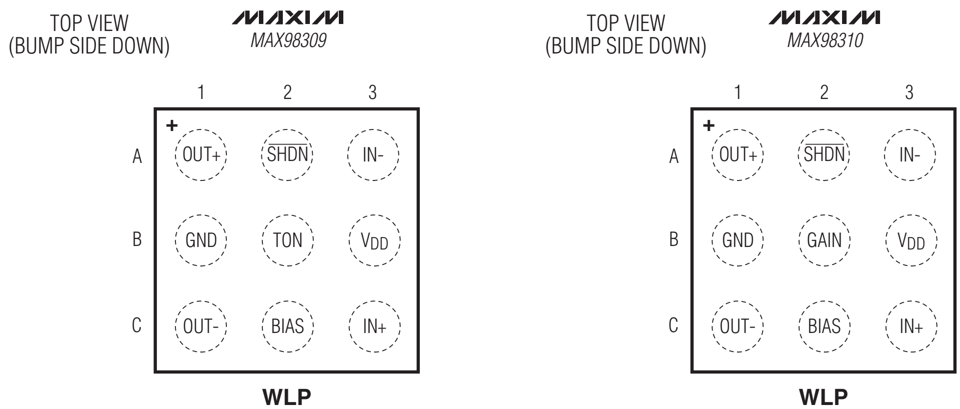
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. TEMPERATURE



Pin Configurations



Pin Descriptions

PIN		NAME	FUNCTION
MAX98309	MAX98310		
A1	A1	OUT+	Amplifier Positive Output
A2	A2	$\overline{SHDN}$	Active-Low Shutdown Input. Connect to GND to place the IC into shutdown. Connect to V_{DD} for normal operation.
A3	A3	IN-	Inverting Audio Input
B1	B1	GND	Ground
B2	—	TON	Turn-On Time Selection. Connect TON to GND for a 10ms turn-on time. Connect TON to V_{DD} for a 100ms turn on time.
—	B2	GAIN	Gain Select Input. See Table 1 for gain settings.
B3	B3	V_{DD}	Power Supply Input. Connect a 1µF capacitor from V_{DD} to GND.
C1	C1	OUT-	Amplifier Negative Output
C2	C2	BIAS	Common-Mode DC Bias Bypass. Connect a 0.1µF (min) capacitor to GND.
C3	C3	IN+	Noninverting Audio Input

Mono 1.4W Class AB Audio Amplifiers

Detailed Description

The MAX98309/MAX98310 mono 1.4W Class AB audio amplifiers offer low quiescent current while maintaining excellent SNR and low 0.008% THD+N. Both ICs feature excellent 90dB PSRR and state-of-the-art click-and-pop suppression.

The ICs are offered with an internally fixed 0dB, 3dB, 6dB, and 9dB gain (MAX98310) or an externally set gain (MAX98309) through external resistors.

The MAX98309 features a 10ms or 100ms pin-selectable turn-on time, while the MAX98310 has a preset 5ms turn-on time.

Bias

The ICs operate from a single 2.5V to 5.5V power supply and feature an internally generated common-mode bias voltage of $V_{DD}/2$ reference to ground. BIAS provides both click-and-pop suppression and sets the DC bias level for the audio outputs. Choose the value of the bypass capacitor as described in the *BIAS Capacitor* section. Do not connect external loads to BIAS as this can affect the overall performance.

Turn-On Time

The MAX98309 external gain amplifier features a selectable turn-on time for optimized click-and-pop performance. Connect TON to GND for a 10ms turn-on time. Connect TON to V_{DD} for a 100ms turn-on time. The MAX98310 has a preset 5ms turn-on time.

Shutdown Mode

The ICs feature a 1.8µA low-power shutdown mode that reduces quiescent current consumption. When the active-low shutdown mode is entered, the ICs' internal bias circuitry is disabled, the amplifier outputs go high impedance, and BIAS is driven to GND.

Click-and-Pop Suppression

The ICs feature Maxim's industry-leading click-and-pop suppression circuitry. During startup, the amplifier common-mode bias voltage ramps to the DC bias point. When entering shutdown, the amplifier outputs are high impedance between both outputs. This scheme minimizes the energy present in the audio band.

Applications Information

BTL Amplifier

The ICs are designed to drive a load differentially, a configuration referred to as bridge-tied load, or BTL. The BTL configuration (Figure 1) offers advantages over the single-ended configuration, where one side of the load is connected to ground. Driving the load differentially doubles the output voltage compared to a single-ended amplifier under similar conditions.

Substituting 2 x $V_{OUT(P-P)}$ for $V_{OUT(P-P)}$ into the following equations yields four times the output power due to doubling of the output voltage:

$$V_{RMS} = \frac{V_{OUT(P-P)}}{2\sqrt{2}}$$

$$P_{OUT} = \frac{V_{RMS}{}^2}{R_L}$$

Because the differential outputs are biased at midsupply, there is no net DC voltage across the load. This eliminates the need for DC-blocking capacitors required for single-ended amplifiers. These capacitors can be large, expensive, consume board space, and degrade low-frequency performance.

Power Dissipation and Heatsinking

Under normal operating conditions, the ICs dissipate a significant amount of power. The maximum power dissipation is given in the *Absolute Maximum Ratings* or can be calculated by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in C/W as specified in the *Absolute Maximum Ratings*.

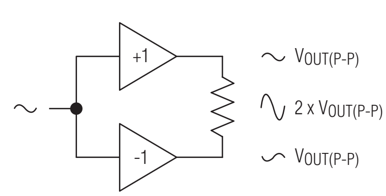


Figure 1. BTL Configuration

The increase in power delivered by the BTL configuration directly results in an increase in internal power dissipation over the single-ended configuration. The maximum internal power dissipation for a given V_{DD} and load is given by the following equation:

$$P_{D(MAX)} = \frac{2V_{DD}^2}{\pi^2 R_L}$$

If the internal power dissipation for a given application exceeds the maximum allowed for a given package, reduce power dissipation by increasing the ground plane heatsinking capability and the size of the traces to the device. See the *Layout and Grounding* section. Other methods for reducing power dissipation are to reduce V_{DD}, increase load impedance, decrease ambient temperature, reduce gain, or reduce input signal.

Thermal-overload protection limits total power dissipation in the MAX98309/MAX98310. When the junction temperature exceeds +160°C, the thermal protection circuitry disables the amplifier. Operation returns to normal once the die cools by 15°C.

Amplifier Gain

Fixed Differential Gain (MAX98310)

The MAX98310 features four internally fixed differential gain options selectable by GAIN (Table 1). This simplifies design, decreases required application footprint size, and eliminates external gain-setting resistors.

External Differential Gain (MAX98309)

The MAX98309 features an external gain option. Resistors R_F and R_{IN}. See the *Simplified Block Diagram* and set the gain of the amplifier as follows:

$$A_V = \frac{R_F}{R_{IN}}$$

where A_V is the desired voltage gain. Hence, an R_{IN} of 10kΩ and an R_F of 20kΩ yields a gain of 2V/V or 6dB. R_F can be either fixed or variable, allowing the use of a digitally controlled potentiometer to alter the gain under software control.

Table 1. Fixed Differential Gain

GAIN CONNECTION	GAIN (dB)
V_{DD}	0
GND	3
Unconnected	6
BIAS	9

Input Filter

The fully differential amplifier inputs can be biased at voltages other than midsupply. The common-mode feedback circuit adjusts for input bias, ensuring the outputs are still biased at midsupply. Input capacitors are not required as long as the input voltage is within the specified common-mode range listed in the *Electrical Characteristics* table.

If input capacitors are used, input capacitor C_{IN}, in conjunction with the input resistor R_{IN}, forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Setting f_{-3dB} too high affects the low-frequency response of the amplifier. Use capacitors with adequately low voltage coefficients, such as X7R ceramic capacitors with a high voltage rating. Capacitors with higher voltage coefficients result in increased distortion at low frequencies.

BIAS Capacitor

BIAS is the output of the internally generated V_{DD}/2 bias voltage. The BIAS bypass capacitor, C_{BIAS}, improves PSRR and THD+N by reducing power supply and other noise sources at the common-mode bias node, and also generates the clickless/popless startup DC bias waveform for the speaker amplifiers. Bypass BIAS with a 0.1µF capacitor to GND. Larger values of C_{BIAS} (up to 1µF) improve PSRR.

Supply Bypassing

Proper power-supply bypassing ensures low-noise, low-distortion performance. Connect a 1µF ceramic capacitor from V_{DD} to GND. Add additional bulk capacitance as required by the application. Locate the bypass capacitor as close as possible to the device.

Layout and Grounding

Good PCB layout is essential for optimizing performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance and route heat away from the device. Good grounding improves audio performance, and prevents any digital switching noise from coupling into the audio signal.

Ordering Information

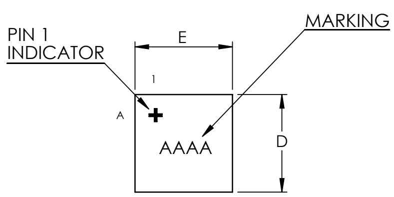
PART	TEMP RANGE	GAIN	PIN-PACKAGE	TOP MARK
MAX98309EWL+	-40°C to +85°C	External	9 WLP	+AIY
MAX98310EWL+	-40°C to +85°C	Fixed	9 WLP	+AIZ

+Denotes a lead(Pb)-free/RoHS-compliant package.

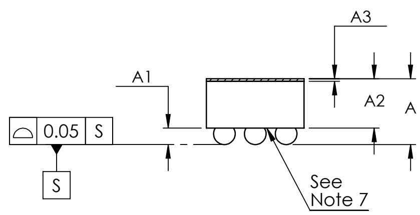
Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 WLP (0.3mm pitch)	W91D1+1	21-0486	Refer to Application Note 1891



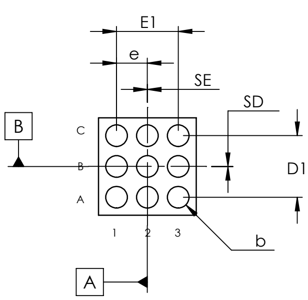
TOP VIEW



SIDE VIEW

COMMON DIMENSIONS		
A	0.64	±0.05
A1	0.16	±0.03
A2	0.48	REF
A3	0.025	BASIC
b	0.21	±0.03
D1	0.60	BASIC
E1	0.60	BASIC
e	0.30	BASIC
SD	0.00	BASIC
SE	0.00	BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W91D1+1	0.95	0.98	0.95	0.98	NONE



BOTTOM VIEW

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

-DRAWING NOT TO SCALE-

TITLE	PACKAGE OUTLINE 9 BUMPS, WLP PKG. 0.3mm PITCH		
APPROVAL	DOCUMENT CONTROL NO. 21-0486	REV. B	1/1

Mono 1.4W Class AB Audio Amplifiers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—

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