1:10 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} 4.1V
Inputs (CLK_, $\overline{CLK\_}$, CLKSEL) ..... V_{EE} - 0.3V to V_{CC} + 0.3V
CLK_ to $\overline{CLK\_}$ ..... ±3.0V
Continuous Output Current 50mA
Surge Output Current 100mA
V_{BB} Sink/Source Current ..... ±0.65mA
Junction-to-Ambient Thermal Resistance in Still Air
7mm x 7mm LQFP ..... +90°C/W
Junction-to-Ambient Thermal Resistance with 500 LFPM Airflow
7mm x 7mm LQFP ..... +60°C/W
Junction-to-Case Thermal Resistance
7mm x 7mm LQFP ..... +12°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
ESD Protection
Human Body Model (CLKSEL, CLK_, $\overline{CLK\_}$, Q_, $\overline{Q\_}$, V_{BB}) 2kV
Soldering Temperature (10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, CLKSEL = high or low, unless otherwise noted.) (Notes 1–4)

PARAMETER	SYMBOL	CONDITIONS		-40°C		+25°C		+85°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
SINGLE-ENDED INPUT (CLKSEL)										
Input High Voltage	V_{IH}	Internal V_{BB} threshold	MAX9311	V_{CC} - 1.23	V_{CC}	V_{CC} - 1.23	V_{CC}	V_{CC} - 1.23	V_{CC}	V
			MAX9313	V_{CC} - 1.165	V_{CC}	V_{CC} - 1.165	V_{CC}	V_{CC} - 1.165	V_{CC}	
Input Low Voltage	V_{IL}	Internal V_{BB} threshold	MAX9311	V_{EE}	V_{CC} - 1.62	V_{EE}	V_{CC} - 1.62	V_{EE}	V_{CC} - 1.62	V
			MAX9313	V_{EE}	V_{CC} - 1.475	V_{EE}	V_{CC} - 1.475	V_{EE}	V_{CC} - 1.475	
Input High Current	I_{IH}				150		150		150	µA
Input Low Current	I_{IL}			-10	+10	-10	+10	-10	+10	µA
DIFFERENTIAL INPUTS (CLK_, $\overline{CLK\_}$)										
Single-Ended Input High Voltage	V_{IH}	V_{BB} connected to $\overline{CLK\_}$ (V_{IL} for V_{BB} connected to CLK_), Figure 1	MAX9311	V_{CC} - 1.23	V_{CC}	V_{CC} - 1.23	V_{CC}	V_{CC} - 1.23	V_{CC}	V
			MAX9313	V_{CC} - 1.165	V_{CC}	V_{CC} - 1.165	V_{CC}	V_{CC} - 1.165	V_{CC}	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - V_{EE} = +2.25V to +3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, CLKSEL = high or low, unless otherwise noted.) (Notes 1–4)

PARAMETER	SYMBOL	CONDITIONS		-40°C MIN	-40°C MAX	+25°C MIN	+25°C MAX	+85°C MIN	+85°C MAX	UNITS
Single-Ended Input Low Voltage	V_{IL}	V_{BB} connected to $\overline{CLK\_}$ (V_{IH} for V_{BB} connected to CLK_), Figure 1	MAX9311	V_{EE}	V_{CC} - 1.62	V_{EE}	V_{CC} - 1.62	V_{EE}	V_{CC} -1.62	V
			MAX9313	V_{EE}	V_{CC} - 1.475	V_{EE}	V_{CC} - 1.475	V_{EE}	V_{CC} -1.475	
High Voltage of Differential Input	V_{IHD}			V_{EE} +1.2	V_{CC}	V_{EE} + 1.2	V_{CC}	V_{EE} +1.2	V_{CC}	V
Low Voltage of Differential Input	V_{ILD}			V_{EE}	V_{CC} - 0.095	V_{EE}	V_{CC} - 0.095	V_{EE}	V_{CC} - 0.095	V
Differential Input Voltage	V_{IHD} - V_{ILD}	For V_{CC} - V_{EE} < 3.0V		0.095	V_{CC} - V_{EE}	0.095	V_{CC} - V_{EE}	0.095	V_{CC} - V_{EE}	V
		For V_{CC} - V_{EE} ≥ 3.0V		0.095	3.0	0.095	3.0	0.095	3.0	
Input High Current	I_{IH}				150		150		150	µA
CLK_ Input Low Current	I_{ILCLK}			-10	+10	-10	+10	-10	+10	µA
$\overline{CLK\_}$ Input Low Current	I_{ILCLK}			-150		-150		-150		µA
OUTPUTS (Q_, $\overline{Q\_}$)										
Single-Ended Output High Voltage	V_{OH}	Figure 1		V_{CC} - 1.025	V_{CC} - 0.900	V_{CC} - 1.025	V_{CC} - 0.900	V_{CC} - 1.025	V_{CC} - 0.900	V
Single-Ended Output Low Voltage	V_{OL}	Figure 1		V_{CC} - 1.93	V_{CC} - 1.695	V_{CC} - 1.93	V_{CC} - 1.695	V_{CC} - 1.93	V_{CC} - 1.695	V
Differential Output Voltage	V_{OH} - V_{OL}	Figure 1		670	950	670	950	670	950	mV
REFERENCE (V_{BB})										
Reference Voltage Output (Note 5)	V_{BB}	I_{BB} = ±0.5mA	MAX9311	V_{CC} - 1.525	V_{CC} - 1.325	V_{CC} - 1.525	V_{CC} - 1.325	V_{CC} - 1.525	V_{CC} - 1.325	V
			MAX9313	V_{CC} - 1.38	V_{CC} - 1.26	V_{CC} - 1.38	V_{CC} - 1.26	V_{CC} - 1.38	V_{CC} - 1.26	
POWER SUPPLY										
Supply Current (Note 6)	I_{EE}				75		82		95	mA

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 2.25V to 3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, input frequency = 1.5GHz, input transition time = 125ps (20% to 80%), CLKSEL = high or low, V_{IHD} = V_{EE} + 1.2V to V_{CC}, V_{ILD} = V_{EE} to V_{CC} - 0.15V, V_{IHD} - V_{ILD} = 0.15V to the smaller of 3V or V_{CC} - V_{EE}, unless otherwise noted. Typical values are at V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} -1V, V_{ILD} = V_{CC} -1.5V.) (Note 7)

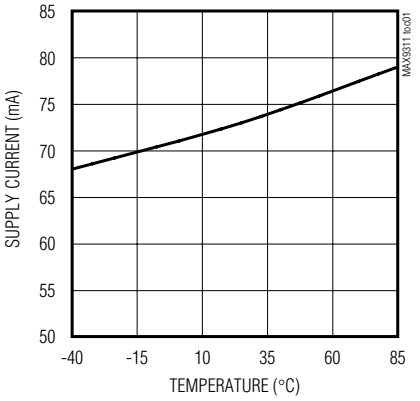
PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MA	MIN	TYP	MAX	
Differential Input-to-Output Delay	t_{PLHD}, t_{PHLD}	Figure 2	220	321	380	220	312	410	260	322	400	ps
Output-to-Output Skew (Note 8)	t_{SKOO}			12	46		12	46		10	35	ps
Part-to-Part Skew (Note 9)	t_{SKPP}			30	160		30	190		30	140	ps
Added Random Jitter (Note 10)	t_{RJ}	f_{IN} = 1.5GHz, Clock pattern		1.2	2.5		1.2	2.5		1.2	2.5	ps (RMS)
		f_{IN} = 3.0GHz, Clock pattern		1.2	2.6		1.2	2.6		1.2	2.6	
Added Deterministic Jitter (Note 10)	t_{DJ}	3Gbps, 2^{23} -1 PRBS pattern		80	95		80	95		80	95	ps (p-p)
Switching Frequency	f_{MAX}	V_{OH} - V_{OL} ≥ 350mV, Clock pattern, Figure 2	2.0			2.0	3.0		2.0			GHz
		V_{OH} - V_{OL} ≥ 500mV, Clock pattern, Figure 2	1.5			1.5			1.5			
Output Rise/Fall Time (20% to 80%)	t_R, t_F	Figure 2	100	112	140	100	116	140	100	121	140	ps

Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: Single-ended input operation using V_{BB} is limited to V_{CC} - V_{EE} = 3.0V to 3.8V for the MAX9311 and V_{CC} - V_{EE} = 2.7V to 3.8V for the MAX9313.
Note 4: DC parameters production tested at T_A = +25°C. Guaranteed by design and characterization over the full operating temperature range.
Note 5: Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.
Note 6: All pins open except V_{CC} and V_{EE}.
Note 7: Guaranteed by design and characterization. Limits are set at ±6 sigma.
Note 8: Measured between outputs of the same part at the signal crossing points for a same-edge transition.
Note 9: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.
Note 10: Device jitter added to the input signal.

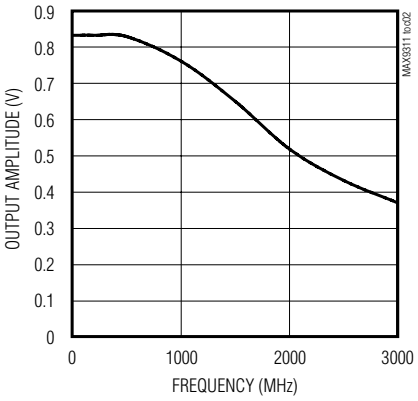
Typical Operating Characteristics

(V_{CC} = +3.3V, V_{EE} = 0, V_{IHD} = V_{CC} - 0.95V, V_{ILD} = V_{CC} - 1.25V, input transition time = 125ps (20% to 80%), f_{IN} = 1.5GHz, outputs loaded with 50Ω to V_{CC} - 2V, T_A = +25°C, unless otherwise noted.)

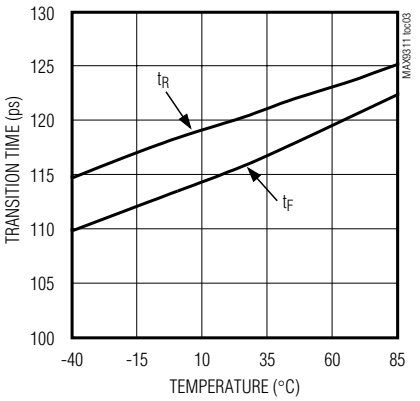
SUPPLY CURRENT (I_{EE}) vs. TEMPERATURE



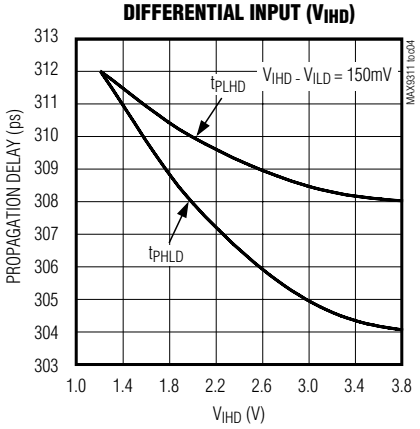
OUTPUT AMPLITUDE (V_{OH} - V_{OL}) vs. FREQUENCY



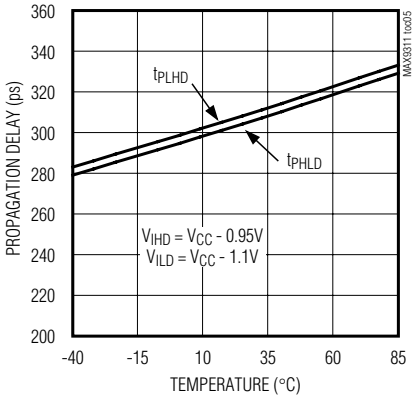
TRANSITION TIME vs. TEMPERATURE



PROPAGATION DELAY vs. HIGH VOLTAGE OF DIFFERENTIAL INPUT (V_{IHD})



PROPAGATION DELAY vs. TEMPERATURE



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Pin Description

PIN	NAME	FUNCTION
1, 9, 16, 25, 32	V_{CC}	Positive Supply Voltage. Bypass from V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	CLKSEL	Clock Select Input (Single-Ended). Drive low to select the CLK0, $\overline{CLK0}$ input. Drive high to select the CLK1, $\overline{CLK1}$ input. The CLKSEL threshold is V_{BB}. If CLKSEL is not driven by a logic signal, use a 1kΩ pulldown to V_{EE} to select CLK0, $\overline{CLK0}$, or a 1kΩ pullup to V_{CC} to select CLK1, $\overline{CLK1}$.
3	CLK0	Noninverting Differential Clock Input 0. Internal 75kΩ pulldown resistor.
4	$\overline{CLK0}$	Inverting Differential Clock Input 0. Internal 75kΩ pullup and pulldown resistors.
5	V_{BB}	Reference Output Voltage. Connect to the inverting or noninverting clock input to provide a reference for single-ended operation. When used, bypass with a 0.01µF ceramic capacitor to V_{CC}; otherwise, leave open.
6	CLK1	Noninverting Differential Clock Input 1. Internal 75kΩ pulldown resistor.
7	$\overline{CLK1}$	Inverting Differential Clock Input 1. Internal 75kΩ pullup and pulldown resistors.
8	V_{EE}	Negative Supply Voltage
10	$\overline{Q9}$	Inverting Q9 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
11	Q9	Noninverting Q9 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
12	$\overline{Q8}$	Inverting Q8 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
13	Q8	Noninverting Q8 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
14	$\overline{Q7}$	Inverting Q7 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
15	Q7	Noninverting Q7 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
17	$\overline{Q6}$	Inverting Q6 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
18	Q6	Noninverting Q6 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
19	$\overline{Q5}$	Inverting Q5 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
20	Q5	Noninverting Q5 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
21	$\overline{Q4}$	Inverting Q4 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
22	Q4	Noninverting Q4 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
23	$\overline{Q3}$	Inverting Q3 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
24	Q3	Noninverting Q3 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
26	$\overline{Q2}$	Inverting Q2 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
27	Q2	Noninverting Q2 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
28	$\overline{Q1}$	Inverting Q1 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
29	Q1	Noninverting Q1 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
30	$\overline{Q0}$	Inverting Q0 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
31	Q0	Noninverting Q0 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.

Detailed Description

The MAX9311/MAX9313 are low skew, 1-to-10 differential drivers designed for clock and data distribution.

A 2:1 mux selects between the two differential inputs, CLK0, $\overline{CLK0}$ and CLK1, $\overline{CLK1}$. The 2:1 mux is switched by the single-ended CLKSEL input. A logic low selects the CLK0, $\overline{CLK0}$ input. A logic high selects the CLK1, $\overline{CLK1}$ input. The logic threshold for CLKSEL is set by an internal V_{BB} voltage reference. The CLKSEL input can be driven to V_{CC} and V_{EE} or by a single-ended LVPECL/LVECL signal. The selected input is reproduced at 10 differential outputs.

For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock or data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply.

The differential inputs can be configured to accept single-ended inputs when operating at approximately V_{CC} - V_{EE} = +3.0V to +3.8V for the MAX9311 or V_{CC} - V_{EE} = +2.7V to +3.8V for the MAX9313. This is accomplished by connecting the on-chip reference voltage, V_{BB}, to an input as a reference. For example, the differential CLK0, $\overline{CLK0}$ input is converted to a noninverting, single-ended input by connecting V_{BB} to $\overline{CLK0}$ and connecting the single-ended input to CLK0. Similarly, an inverting input is obtained by connecting V_{BB} to CLK0 and connecting the single-ended input to $\overline{CLK0}$. With a differential input configured as single-ended (using V_{BB}), the single-ended input can be driven to V_{CC} and V_{EE} or with a single-ended LVPECL/LVECL signal.

When a differential input is configured as a single-ended input (using V_{BB}), the approximate supply range is V_{CC} - V_{EE} = +3.0V to +3.8V for the MAX9311 and V_{CC} - V_{EE} = +2.7V to +3.8V for the MAX9313. This is because one of the inputs must be V_{EE} + 1.2V or higher for proper operation of the input stage. V_{BB} must be at least V_{EE} + 1.2V because it becomes the high-level input when the other (single-ended) input swings below it. Therefore, minimum V_{BB} = V_{EE} + 1.2V.

The minimum V_{BB} output for the MAX9311 is V_{CC} - 1.525V and the minimum V_{BB} output for the MAX9313 is V_{CC} - 1.38V. Substituting the minimum V_{BB} output for each device into V_{BB} = V_{EE} + 1.2V results in a minimum supply of 2.725V for the MAX9311 and 2.58V for the MAX9313. Rounding up to standard supplies gives the single-ended operating supply ranges of V_{CC} - V_{EE} = 3.0V to 3.8V for the MAX9311 and V_{CC} - V_{EE} = 2.7V to 3.8V for the MAX9313.

When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC}. If the V_{BB} reference is not used, it can be left open. The V_{BB} reference can source or sink 0.5mA, which is sufficient to drive two inputs. Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.

The maximum magnitude of the differential input from CLK_ to $\overline{CLK\_}$ is 3.0V or V_{CC} - V_{EE}, whichever is less. This limit also applies to the difference between any reference voltage input and a single-ended input.

The differential inputs have bias resistors that drive the outputs to a differential low when the inputs are open. The inverting inputs ($\overline{CLK0}$ and $\overline{CLK1}$) are biased with a 75kΩ pullup to V_{CC} and a 75kΩ pulldown to V_{EE}. The noninverting inputs (CLK0 and CLK1) are biased with a 75kΩ pulldown to V_{EE}. The single-ended CLKSEL input does not have a bias resistor. If not driven, pull CLKSEL up or down with a 1kHz resistor (see *Pin Description*).

Specifications for the high and low voltages of a differential input (V_{IHD} and V_{ILD}) and the differential input voltage (V_{IHD} - V_{ILD}) apply simultaneously (V_{ILD} cannot be higher than V_{IHD}).

Output levels are referenced to V_{CC} and are considered LVPECL or LVECL, depending on the level of the V_{CC} supply. With V_{CC} connected to a positive supply and V_{EE} connected to GND, the outputs are LVPECL. The outputs are LVECL when V_{CC} is connected to GND and V_{EE} is connected to a negative supply.

A single-ended input of at least V_{BB} ±95mV or a differential input of at least 95mV switches the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics* table.

Applications Information

Supply Bypassing

Bypass V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close to the device as possible, with the 0.01µF value capacitor closest to the device. Use multiple parallel vias for low inductance. When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC} (if the V_{BB} reference is not used, it can be left open).

Traces

Input and output trace characteristics affect the performance of the MAX9311/MAX9313. Connect each signal of a differential input or output to a 50Ω characteristic impedance trace. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Reduce skew within a

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differential pair by matching the electrical length of the traces.

Output Termination

Terminate outputs through 50Ω to V_{CC} - 2V or use an equivalent Thevenin termination. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if Q0 is used as a single-ended output, terminate both Q0 and $\overline{Q0}$.

Chip Information

TRANSISTOR COUNT: 250

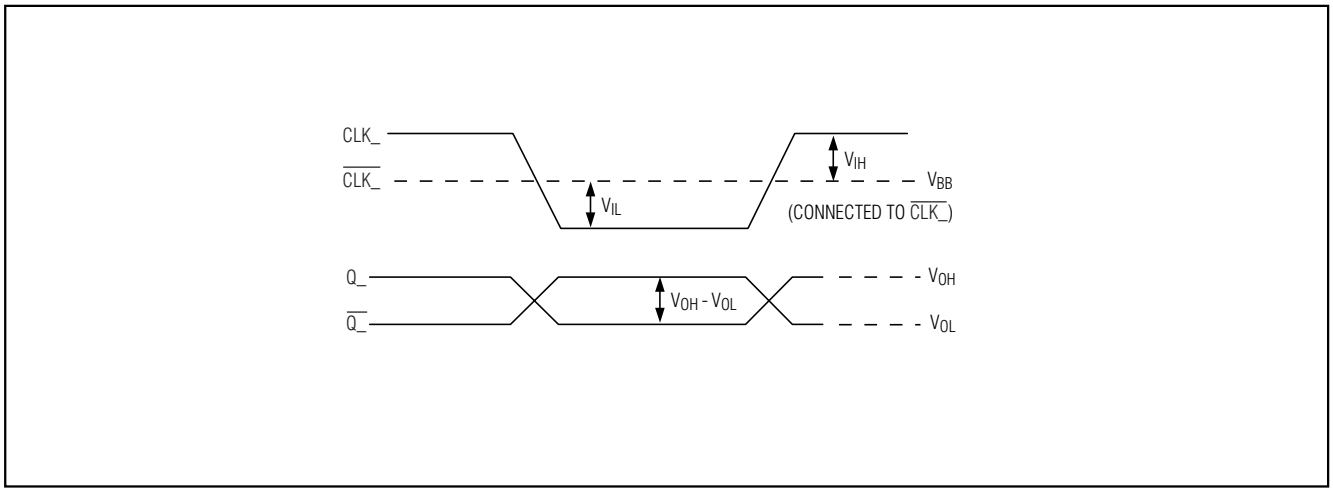

Figure 1. Switching with Single-Ended Input

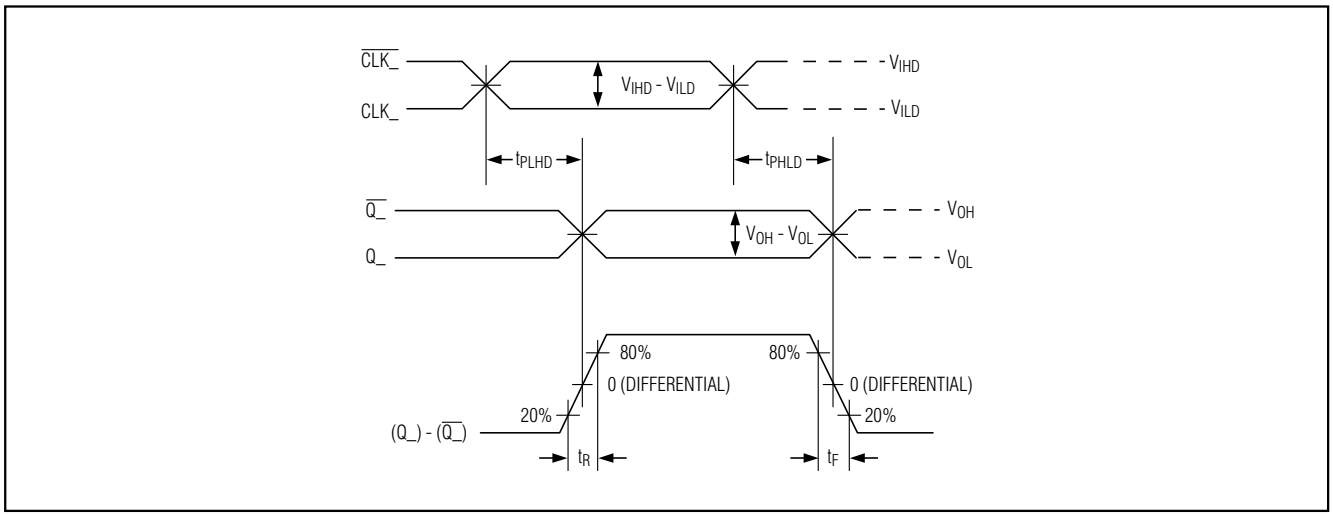

Figure 2. Differential Transition Time and Propagation Delay Timing Diagram

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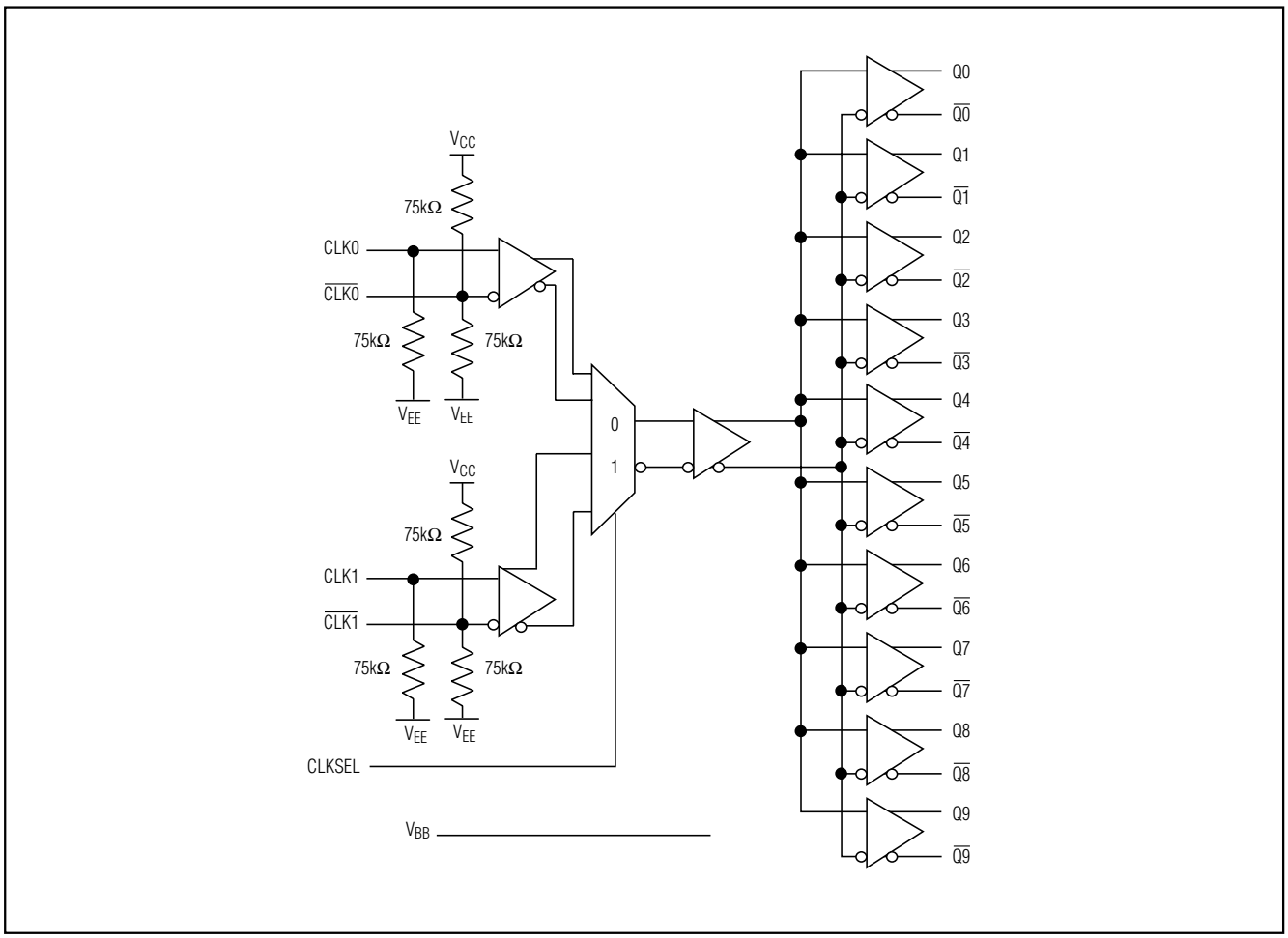
Functional Diagram



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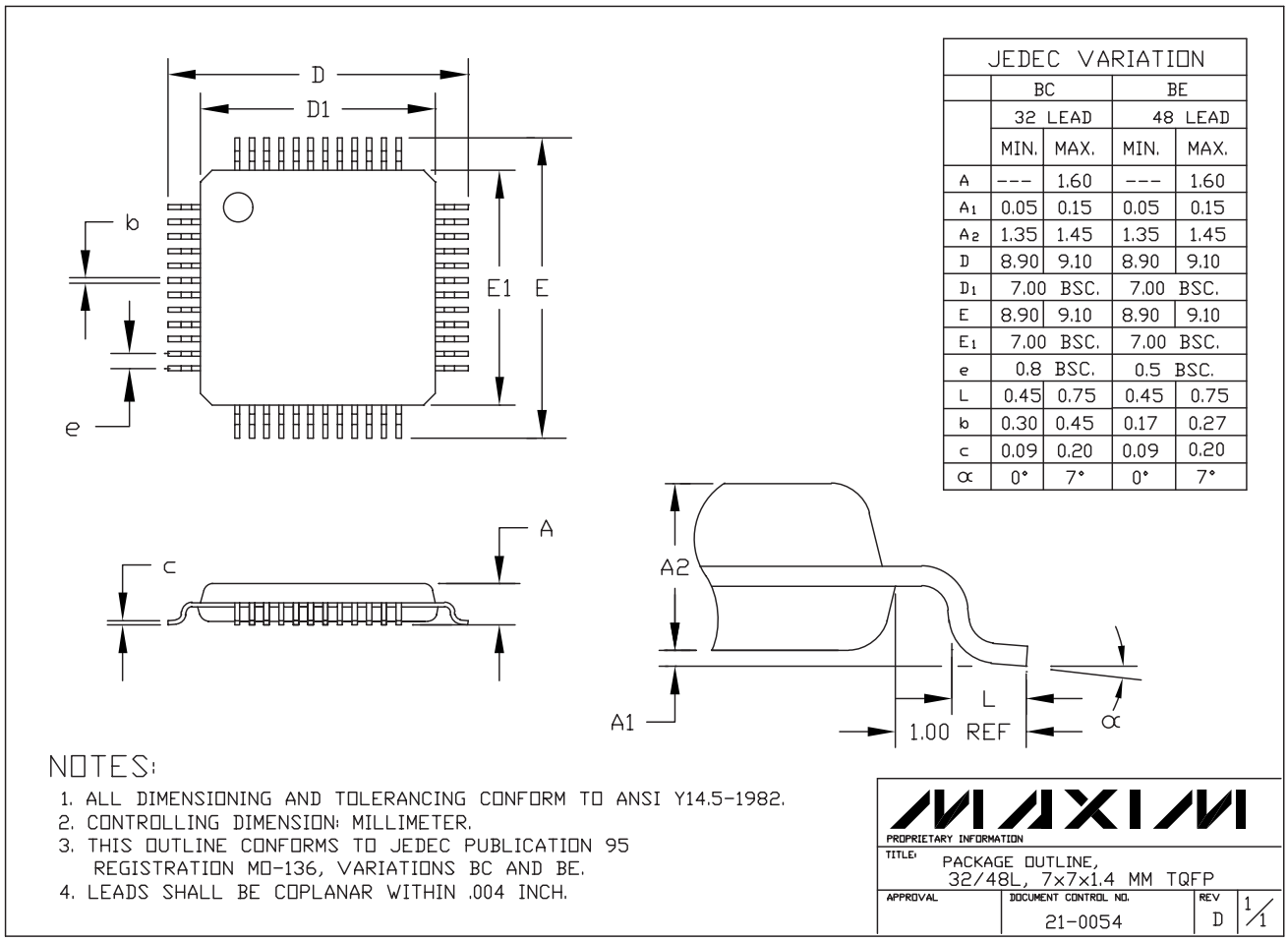
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



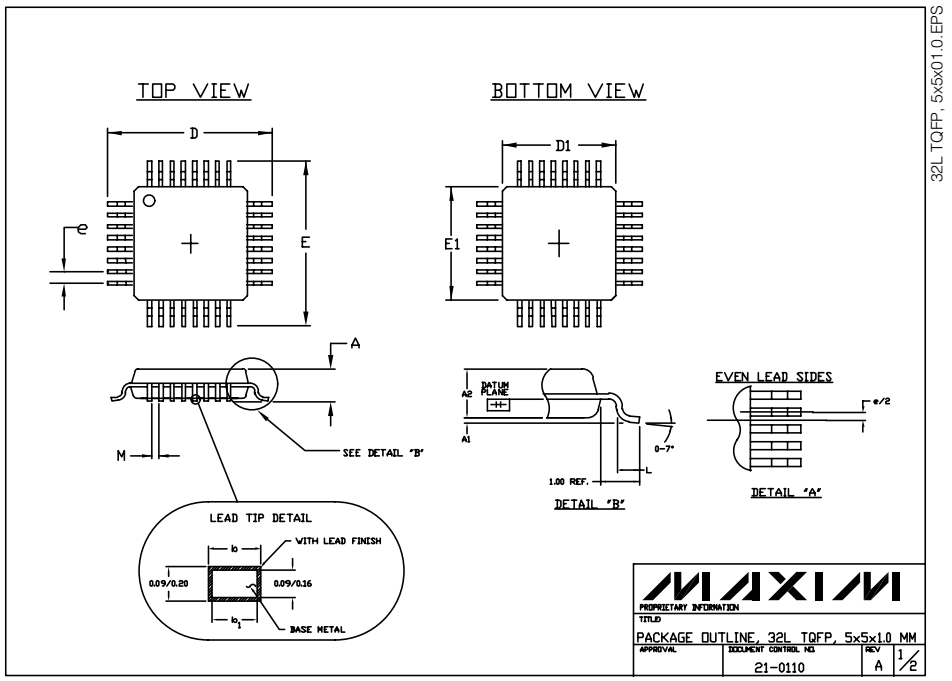
JEDEC VARIATION				
	BC		BE	
	32 LEAD		48 LEAD	
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	7.00 BSC.		7.00 BSC.	
E	8.90	9.10	8.90	9.10
E_1	7.00 BSC.		7.00 BSC.	
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
c	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°

32/48L TQFP EPS

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

32L TQFP, 5x5x01.0.EPS



NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MO-136.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

	JEDEC VARIATIONS	
	DIMENSIONS IN MILLIMETERS	
	AA	
	5x5x1.0 MM	
	MIN.	MAX.
A	~~	1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	7.00 BSC.	
D_1	5.00 BSC.	
E	7.00 BSC.	
E_1	5.00 BSC.	
L	0.45	0.75
M	0.15	~~
N	32	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23

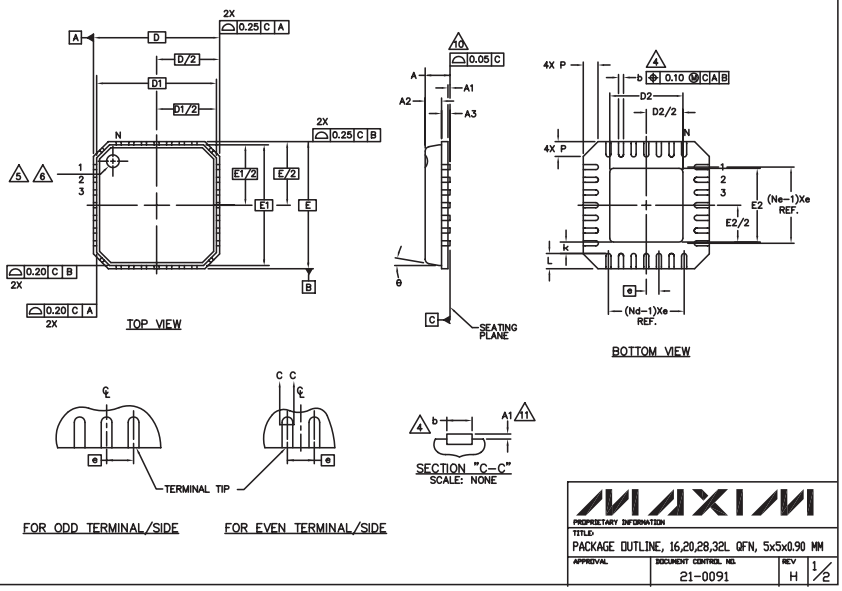
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 32L TQFP, 5x5x1.0 MM
APPROVAL
DOCUMENT CONTROL NO.
21-0110
REV
A
2/2

1:10 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

32L QFN.EPS



COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°		12°	0°		12°	0°		12°	0°		12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM
APPROVAL
DOCUMENT CONTROL NO. 21-0091
REV H
2/2

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