## Absolute Maximum Ratings

Terminal Voltage (with respect to GND)
- $V_{CC}$ ..... -0.3V to +6V
- $V_{VBATT}$ ..... -0.3V to +6V
- All Other Inputs ..... -0.3V to ($V_{OUT}$ + 0.3V)

Input Current
- $V_{CC}$ Peak ..... 1.0A
- $V_{CC}$ Continuous ..... 250mA
- VBATT Peak ..... 250mA
- VBATT Continuous ..... 25mA
- GND, BATT ON ..... 100mA
- All Other Outputs ..... 25mA

Continuous Power Dissipation ($T_A$ = +70°C)
- TSSOP (derate 6.70mW/°C above +70°C) ..... 533mW
- Narrow SO (derate 8.70mW/°C above +70°C) ..... 696mW
- Wide SO (derate 9.52mW/°C above +70°C) ..... 762mW
- Plastic DIP (derate 10.53mW/°C above +70°C) ..... 842mW
- CERDIP (derate 10.00mW/°C above +70°C) ..... 800mW

Operating Temperature Ranges
- MAX69_AC_ _/MAX800_C_ _ ..... 0°C to +70°C
- MAX69_AE_ _/MAX800_E_ _ ..... -40°C to +85°C
- MAX69_AMJE ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10s) ..... +300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Electrical Characteristics

(MAX691A, MAX800L: $V_{CC}$ = +4.75V to +5.5V; MAX693A, MAX800M: $V_{CC}$ = +4.5V to +5.5V; $V_{VBATT}$ = 2.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

| PARAMETER | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Operating Voltage Range, $V_{CC}$, $V_{VBATT}$ (Note 1) | | | | 0 | | 5.5 | V |
| $V_{OUT}$ Output | $V_{CC}$ = 4.5V | $I_{OUT}$ = 25mA | | $V_{CC}$ - 0.05 | $V_{CC}$ - 0.02 | | V |
| | | $I_{OUT}$ = 250mA | MAX69_AC | $V_{CC}$ - 0.3 | $V_{CC}$ - 0.2 | | |
| | | | MAX69_AE, MAX800_C/E | $V_{CC}$ - 0.35 | $V_{CC}$ - 0.2 | | |
| | | | MAX69_A/M | $V_{CC}$ - 0.40 | | | |
| | | $I_{OUT}$ = 210mA | MAX69_AC/AE, MAX800_C/E | $V_{CC}$ - 0.3V | $V_{CC}$ - 0.17 | | |
| $V_{CC}$-to-$V_{OUT}$ On-Resistance | $V_{CC}$ = 4.5V | MAX69_AC, MAX800_C | | | 0.8 | 1.2 | Ω |
| | | MAX69_AE, MAX800_E | | | 0.8 | 1.4 | |
| | | MAX69_A/M | | | 0.8 | 1.6 | |
| $V_{OUT}$ in Battery-Backup Mode | $V_{VBATT}$ = 4.5V, $I_{OUT}$ = 20mA | | | $V_{VBATT}$ - 0.3 | | | V |
| | $V_{VBATT}$ = 2.8V, $I_{OUT}$ = 10mA | | | $V_{VBATT}$ - 0.25 | | | |
| | $V_{VBATT}$ = 2.0V, $I_{OUT}$ = 5mA | | | $V_{VBATT}$ - 0.15 | | | |
| VBATT-to-$V_{OUT}$ On-Resistance | $V_{VBATT}$ = 4.5V | | | | | 15 | Ω |
| | $V_{VBATT}$ = 2.8V | | | | | 25 | |
| | $V_{VBATT}$ = 2.0V | | | | | 30 | |
| Supply Current in Normal Operating Mode (excludes $I_{OUT}$) | $V_{CC}$ > $V_{VBATT}$ - 1V | | | | 30 | 100 | µA |
| Supply Current in Battery-Backup Mode (excludes $I_{OUT}$) (Note 2) | $V_{CC}$ < $V_{VBATT}$ - 1.2V, $V_{VBATT}$ = 2.8V | $T_A$ = +25°C | | | 0.04 | 1 | µA |
| | | $T_A$ = $T_{MIN}$ + $T_{MIN}$ | | | | 5 | |
| VBATT Standby Current (Note 3) | $V_{VBATT}$ + 0.2V ≤ VCC | $T_A$ = +25°C | | -0.1 | | 0.02 | µA |
| | | $T_A$ = $T_{MIN}$ + $T_{MIN}$ | | -1.0 | | 0.02 | |
| Battery Switchover Threshold | Power-up | | | $V_{VBATT}$ + 0.3 | | | V |
| | Power-down | | | $V_{VBATT}$ - 0.3 | | | |



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## Electrical Characteristics (continued)

(MAX691A, MAX800L: $V_{CC}$ = +4.75V to +5.5V; MAX693A, MAX800M: $V_{CC}$ = +4.5V to +5.5V; $V_{VBATT}$ = 2.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Battery Switchover Hysteresis | | | 60 | | mV |
| BATT ON Output Low Voltage | $I_{SINK}$ = 3.2mA | | 0.1 | 0.4 | V |
| | $I_{SINK}$ = 25mA | | 0.7 | 1.5 | |
| BATT ON Output Short-Circuit Current | Sink current | | 60 | 100 | mA |
| | Source current | 1 | 15 | 100 | µA |
| **RESET AND WATCHDOG TIMER** | | | | | |
| Reset Threshold Voltage | MAX691A, MAX800L | 4.50 | 4.65 | 4.75 | V |
| | MAX693A, MAX800M | 4.25 | 4.40 | 4.50 | |
| | MAX800L, $T_A$ = +25°C, $V_{CC}$ falling | 4.55 | | 4.70 | |
| | MAX800M, $T_A$ = +25°C, $V_{CC}$ falling | 4.30 | | 4.45 | |
| Reset Threshold Hysteresis | | | 15 | | mV |
| $V_{CC}$ to RESET Delay | Power-down | | 80 | | µs |
| $\overline{\text{LOW LINE}}$-to-$\overline{\text{RESET}}$ Delay | | | 800 | | ns |
| Reset Active Timeout Period, Internal Oscillator | Power-up | 140 | 200 | 280 | ms |
| Reset Active Timeout Period, External Clock (Note 4) | Power-up | | 2048 | | Clock Cycles |
| Watchdog Timeout Period, Internal Oscillator | Long period | 1.0 | 1.6 | 2.25 | sec |
| | Short period | 70 | 100 | 140 | ms |
| Watchdog Timeout Period, External Clock (Note 4) | Long period | | 4096 | | Clock Cycles |
| | Short period | | 1024 | | |
| Minimum Watchdog Input Pulse Width | $V_{IL}$ = 0.8V, $V_{IH}$ = 0.75 x $V_{CC}$ | 100 | | | ns |
| $\overline{\text{RESET}}$ Output Voltage | $I_{SINK}$ = 50µA, $V_{CC}$ = 1V, VBATT = 0V, $V_{CC}$ falling | | 0.004 | 0.3 | V |
| | $I_{SINK}$ = 3.2mA, $V_{CC}$ = 4.25V | | 0.1 | 0.4 | |
| | $I_{SOURCE}$ = 1.6mA, $V_{CC}$ = 5V | 3.5 | | | |
| $\overline{\text{RESET}}$ Output Short-Circuit Current | Output source current | | 7 | 20 | mA |
| RESET Output Voltage Low (Note 5) | $I_{SINK}$ = 3.2mA | 0.1 | 0.4 | | V |
| $\overline{\text{LOW LINE}}$ Output Voltage | $I_{SINK}$ = 3.2mA, $V_{CC}$ = 4.25V | | | 0.4 | V |
| | $I_{SOURCE}$ = 1µA, $V_{CC}$ = 5V | 3.5 | | | |
| $\overline{\text{LOW LINE}}$ Output Short-Circuit Current | Output source current | 1 | 15 | 100 | µA |
| $\overline{\text{WDO}}$ Output Voltage | $I_{SINK}$ = 3.2mA | | | 0.4 | |
| | $I_{SOURCE}$ = 500µA, $V_{CC}$ = 5V | 3.5 | | | |
| $\overline{\text{WDO}}$ Output Short-Circuit Current | Output source current | | 3 | 10 | mA |
| WDI Threshold Voltage (Note 6) | $V_{IH}$ | 0.75 x $V_{CC}$ | | | V |
| | $V_{IL}$ | | | 0.8 | |
| WDI Input Current | WDI = 0V | -50 | -10 | | µA |
| | WDI = $V_{OUT}$ | | 20 | 50 | |



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## Electrical Characteristics (continued)

(MAX691A, MAX800L: $V_{CC}$ = +4.75V to +5.5V; MAX693A, MAX800M: $V_{CC}$ = +4.5V to +5.5V; $V_{VBATT}$ = 2.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **POWER-FAIL COMPARATOR** | | | | | |
| PFI Input Threshold | MAX69_AC/AE/AM, $V_{CC}$ = 5V | 1.2 | 1.25 | 1.3 | V |
| | MAX800_C/E, $V_{CC}$ = 5V | 1.225 | 1.25 | 1.275 | |
| PFI Leakage Current | | | ±0.01 | ±25 | nA |
| $\overline{PFO}$ Output Voltage | $I_{SINK}$ = 3.2mA | | | 0.4 | V |
| | $I_{SOURCE}$ = 1µA, $V_{CC}$ = 5V | 3.5 | | | |
| $\overline{PFO}$ Output Short-Circuit Current | Output source current | 1 | 15 | 100 | µA |
| PFI-to-PFO Delay | $V_{IN}$ = -20mV, $V_{OD}$ = 15mV | | 25 | | µs |
| | $V_{IN}$ = 20mV, $V_{OD}$ = 15mV | | 60 | | |
| **CHIP-ENABLE GATING** | | | | | |
| $\overline{CE}$ IN Leakage Current | Disable mode | | ±0.005 | ±1 | µA |
| $\overline{CE}$ IN-to- $\overline{CE}$ OUT Resistance (Note 7) | Enable mode | | 75 | 150 | Ω |
| $\overline{CE}$ OUT Short-Circuit Current (Reset Active) | Disable mode, $\overline{CE}$ OUT = 0V | 0.1 | 0.75 | 2.0 | mA |
| $\overline{CE}$ IN-to- $\overline{CE}$ OUT Propagation Delay (Note 8) | 50Ω source impedance driver, $C_{LOAD}$ = 50pF | | 6 | 10 | ns |
| $\overline{CE}$ OUT Output-Voltage High (Reset Active) | $V_{CC}$ = 5V, $I_{OUT}$ = -100µA | 3.5 | | | V |
| | $V_{CC}$ = 0V, VBATT = 2.8V, $I_{OUT}$ = 1µA | 2.7 | | | |
| RESET-to-$\overline{CE}$ OUT Delay | Power-down | | 12 | | µs |
| **INTERNAL OSCILLATOR** | | | | | |
| OSC IN Leakage Current | OSC SEL = 0V | | 0.10 | ±5 | µA |
| OSC IN Input Pullup Current | OSC SEL = $V_{OUT}$ or floating, OSC IN = 0V | | 10 | 100 | µA |
| OSC SEL Input Pullup Current | OSC SEL = 0V | | 10 | 100 | µA |
| OSC IN Frequency Range | OSC SEL = 0V | | 50 | | kHz |
| OSC IN External Oscillator Threshold Voltage | $V_{IH}$ | $V_{OUT}$ - 0.3 | $V_{OUT}$ - 0.6 | | V |
| | $V_{IL}$ | | 3.65 | 2.00 | |
| OSC IN Frequency with External Capacitor | OSC SEL = 0V, COSC = 47pF | | 100 | | kHz |

**Note 1:** Either $V_{CC}$ or VBATT can go to 0V, if the other is greater than 2.0V.

**Note 2:** The supply current drawn by the MAX691A/MAX800L/MAX800M from the battery excluding $I_{OUT}$ typically goes to 10µA when (VBATT - 1V) < $V_{CC}$ < VBATT. In most applications, this is a brief period as $V_{CC}$ falls through this region.

**Note 3:** "+" = battery-discharging current, "--" = battery-charging current.

**Note 4:** Although presented as typical values, the number of clock cycles for the reset and watchdog timeout periods are fixed and do not vary with process or temperature.

**Note 5:** RESET is an open-drain output and sinks current only.

**Note 6:** WDI is internally connected to a voltage divider between $V_{OUT}$ and GND. If unconnected, WDI is driven to 1.6V (typ), disabling the watchdog function.

**Note 7:** The chip-enable resistance is tested with $V_{CC}$ = +4.75V for the MAX691A/MAX800L and $V_{CC}$ = +4.5V for the MAX693A/MAX800M. $\overline{CE}$ IN = $\overline{CE}$ OUT = $V_{CC}$/2.

**Note 8:** The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.



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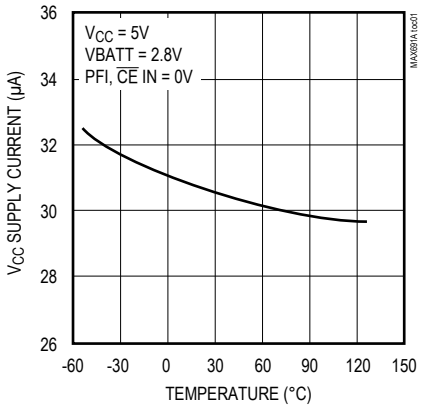
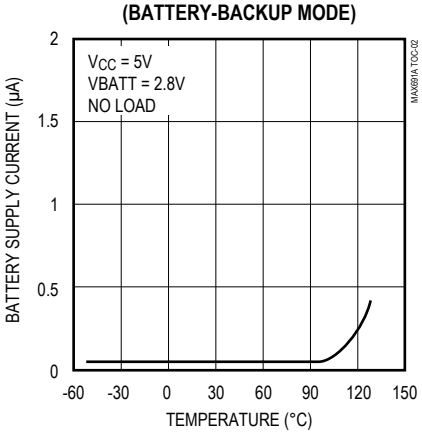
## Typical Operating Characteristics

($T_A$ = +25°C, unless otherwise noted.)

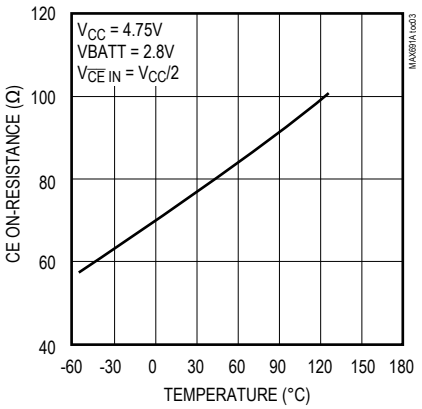
**$V_{CC}$ SUPPLY CURRENT vs. TEMPERATURE (NORMAL OPERATING MODE)**



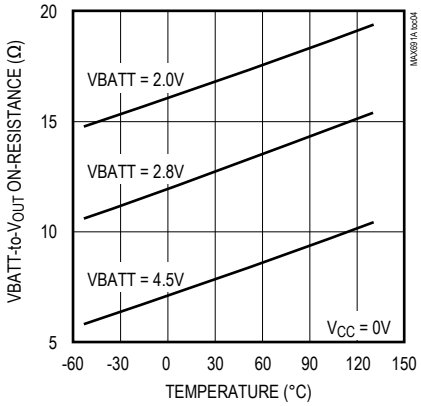

**BATTERY SUPPLY CURRENT vs. TEMPERATURE (BATTERY-BACKUP MODE)**



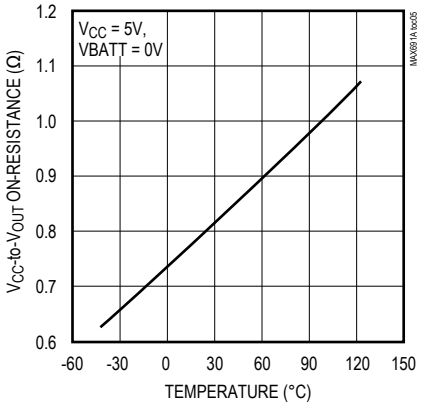

**CHIP-ENABLE ON-RESISTANCE vs. TEMPERATURE**



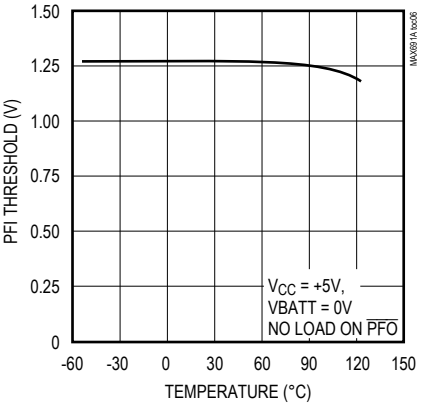

**VBATT to $V_{OUT}$ ON-RESISTANCE vs. TEMPERATURE**



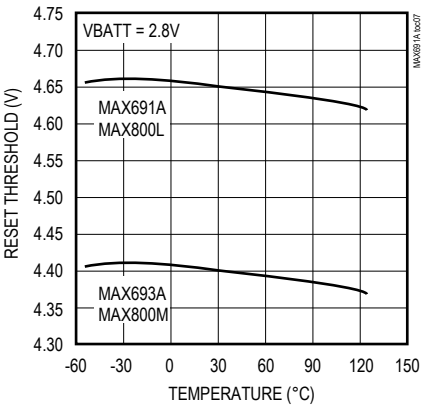

**$V_{CC}$ to $V_{OUT}$ ON-RESISTANCE vs. TEMPERATURE**



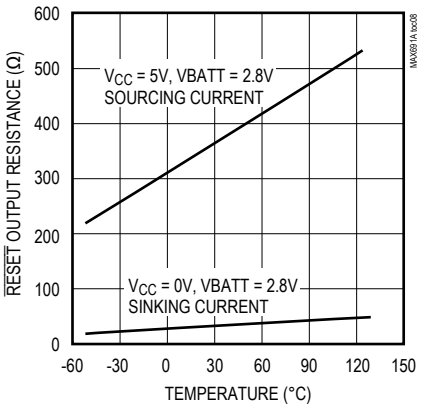

**PFI THRESHOLD vs. TEMPERATURE**



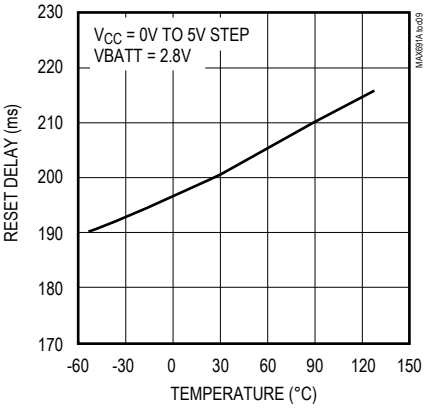

**RESET THRESHOLD vs. TEMPERATURE**




**$\overline{\text{RESET}}$ OUTPUT RESISTANCE vs. TEMPERATURE**




**RESET DELAY vs. TEMPERATURE**



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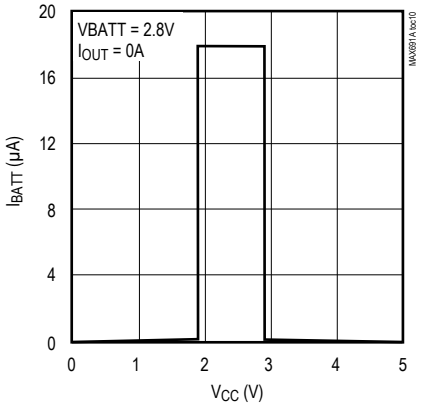
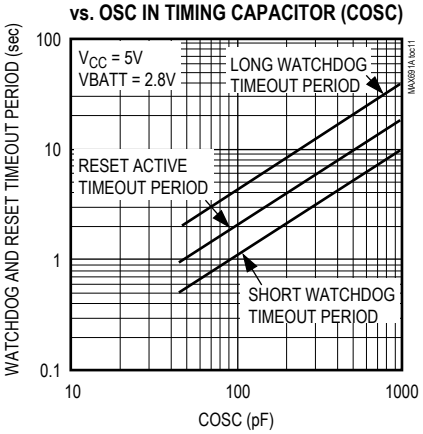
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

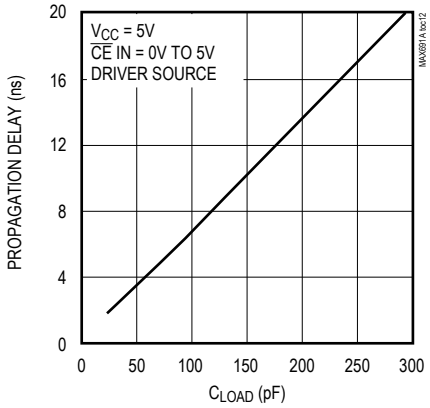
**BATTERY CURRENT vs. INPUT SUPPLY VOLTAGE**



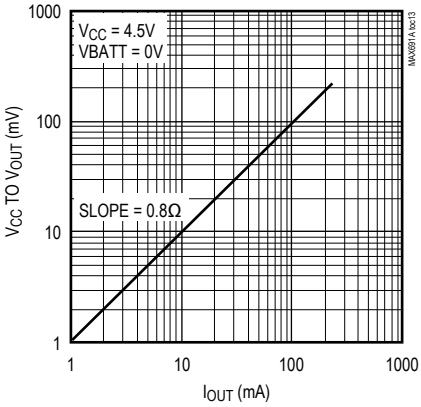

**WATCHDOG AND RESET TIMEOUT PERIOD vs. OSC IN TIMING CAPACITOR (COSC)**



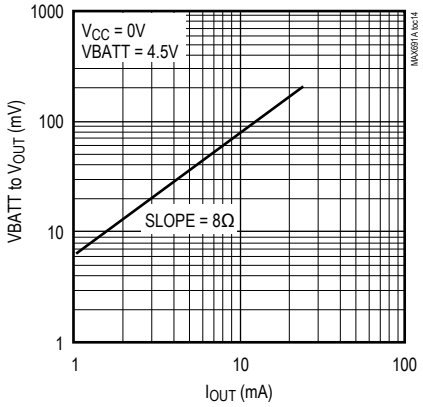

**CHIP-ENABLE PROPAGATION DELAY vs. $\overline{CE}$ OUT LOAD CAPACITANCE**



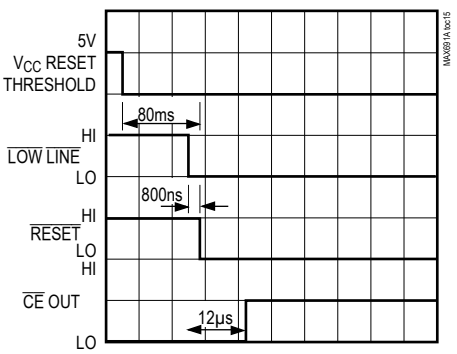

**$V_{CC}$ TO $V_{OUT}$ vs. OUTPUT CURRENT (NORMAL OPERATING MODE)**




**VBATT TO $V_{OUT}$ vs. OUTPUT CURRENT (BATTERY-BACKUP MODE)**




**$V_{CC}$ TO $\overline{LOW\ LINE}$ AND $\overline{CE}$ OUT DELAY**



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## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | VBATT | Battery-Backup Input. Connect to external battery or capacitor and charging circuit. If backup battery is not used, connect to GND. |
| 2 | $V_{OUT}$ | Output Supply Voltage. When $V_{CC}$ is greater than VBATT and above the reset threshold, $V_{OUT}$ connects to $V_{CC}$. When $V_{CC}$ falls below VBATT and is below the reset threshold, $V_{OUT}$ connects to VBATT. Connect a 0.1µF capacitor from $V_{OUT}$ to GND. Connect $V_{OUT}$ to $V_{CC}$ if no backup battery is used. |
| 3 | $V_{CC}$ | Input Supply Voltage, 5V Input. |
| 4 | GND | Ground. 0V reference for all signals. |
| 5 | BATT ON | Battery-On Output. When $V_{OUT}$ switches to VBATT, BATT ON goes high. When $V_{OUT}$ switches to $V_{CC}$, BATT ON goes low. Connect the base of a PNP through a current-limiting resistor to BATT ON for $V_{OUT}$ current require- ments greater than 250mA. |
| 6 | $\overline{\text{LOW LINE}}$ | $\overline{\text{LOW LINE}}$ output goes low when $V_{CC}$ falls below the reset threshold. It returns high as soon as $V_{CC}$ rises above the reset threshold. |
| 7 | OSC IN | External Oscillator Input. When OSC SEL is unconnected or driven high, a 10µA pull-up connects from $V_{OUT}$ to OSC IN, the internal oscillator sets the reset and watchdog timeout periods, and OSC IN selects between fast and slow watchdog timeout periods. When OSC SEL is driven low, the reset and watchdog timeout periods may be set either by a capacitor from OSC IN to ground or by an external clock at OSC IN (Figure 3). |
| 8 | OSC SEL | Oscillator Select. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset delay and watchdog timeout period. When OSC SEL is low, the external oscillator input (OSC IN) is enabled (Table 1). OSC SEL has a 10µA internal pull-up. |
| 9 | PFI | Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low. When PFI is not used, connect PFI to GND or $V_{OUT}$. |
| 10 | $\overline{\text{PFO}}$ | Power-Fail Output. This is the output of the power-fail comparator. $\overline{\text{PFO}}$ goes low when PFI is less than 1.25V. This is an uncommitted comparator, and has no effect on any other internal circuitry. |
| 11 | WDI | Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog time- out period, $\overline{\text{WDO}}$ goes low and reset is asserted for the reset timeout period. $\overline{\text{WDO}}$ remains low until the next tran- sition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between $V_{OUT}$ and GND, which sets it to mid-supply when left unconnected. |
| 12 | $\overline{\text{CE}}$ OUT | Chip-Enable Output. $\overline{\text{CE}}$ OUT goes low only when $\overline{\text{CE}}$ IN is low and $V_{CC}$ is above the reset threshold. If CE IN is low when reset is asserted, $\overline{\text{CE}}$ OUT will stay low for 15µs or until $\overline{\text{CE}}$ IN goes high, whichever occurs first. |
| 13 | $\overline{\text{CE}}$ IN | Chip-Enable Input. The input to chip-enable gating circuit. If $\overline{\text{CE}}$ IN is not used, connect $\overline{\text{CE}}$ IN to GND or $V_{OUT}$. |
| 14 | $\overline{\text{WDO}}$ | Watchdog Output. If WDI remains high or low longer than the watchdog timeout period, $\overline{\text{WDO}}$ goes low and reset is asserted for the reset timeout period. $\overline{\text{WDO}}$ returns high on the next transition at WDI. $\overline{\text{WDO}}$ remains high if WDI is unconnected. |
| 15 | $\overline{\text{RESET}}$ | $\overline{\text{RESET}}$ Output goes low whenever $V_{CC}$ falls below the reset threshold. $\overline{\text{RESET}}$ will remain low typically for 200ms after $V_{CC}$ crosses the reset threshold on power-up. |
| 16 | RESET | RESET is an active-high output. It is open drain, and the inverse of $\overline{\text{RESET}}$. |

## Detailed Description

### $\overline{\text{RESET}}$ and RESET Outputs

The MAX691A/MAX693A/MAX800L/MAX800M's $\overline{\text{RESET}}$ and RESET outputs ensure that the µP (with reset inputs asserted either high or low) powers up in a known state, and prevents code-execution errors during power-down or brownout conditions.

The $\overline{\text{RESET}}$ output is active low, and typically sinks 3.2mA at 0.1V saturation voltage in its active state. When deas-serted, $\overline{\text{RESET}}$ sources 1.6mA at typically $V_{OUT}$ - 0.5V. RESET output is open drain, active high, and typically sinks 3.2mA with a saturation voltage of 0.1V. When no backup battery is used, $\overline{\text{RESET}}$ output is guaranteed to be valid down to $V_{CC}$ = 1V, and an external 10kΩ pulldown resistor on $\overline{\text{RESET}}$ insures that it will be valid with $V_{CC}$ down to GND (Figure 1). As $V_{CC}$ goes below 1V, the gate drive to the $\overline{\text{RESET}}$ output switch reduces accordingly, increasing the $R_{DS(ON)}$ and the saturation voltage. The 10kΩ pulldown resistor insures the parallel combination of switch plus resistor is around 10kΩ and the output saturation voltage is below 0.4V while sinking 40µA. When using a 10kΩ external pulldown resistor, the high state for $\overline{\text{RESET}}$ output with $V_{CC}$ = 4.75V will be 4.5V typical.



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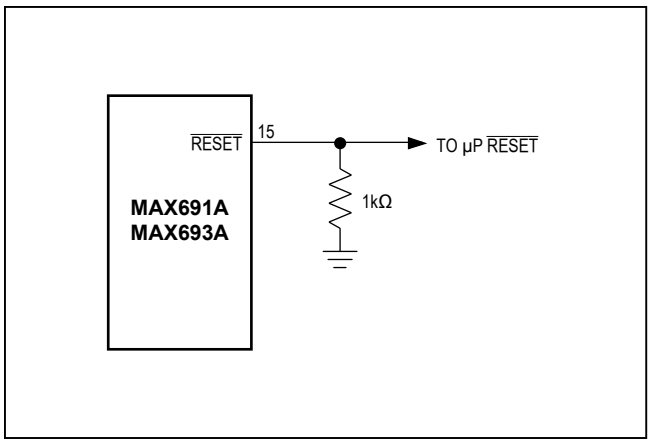


*Figure 1. Adding an external pulldown resistor ensures $\overline{RESET}$ is valid with $V_{CC}$ down to GND.*

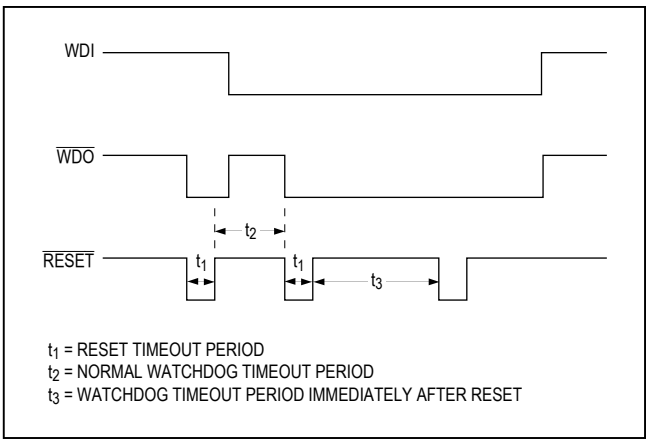


*Figure 2. Watchdog Timeout Period and Reset Active Time*

For battery voltages ≥ 2V connected to VBATT, RESET and $\overline{RESET}$ remain valid for $V_{CC}$ from 0V to 5.5V.

RESET and $\overline{RESET}$ are asserted when $V_{CC}$ falls below the reset threshold (4.65V for the MAX691A/MAX800L, 4.4V for the MAX693A/MAX800M) and remain asserted for 200ms typ after $V_{CC}$ rises above the reset threshold on power-up (Figure 5). The devices' batteryswitchover comparator does not affect reset assertion. However, both reset outputs are asserted in batterybackup mode since $V_{CC}$ must be below the reset threshold to enter this mode.

## Watchdog Function

The watchdog monitors µP activity via the Watchdog Input (WDI). If the µP becomes inactive, $\overline{RESET}$ and RESET are asserted. To use the watchdog function, connect WDI to a bus line or µP I/O line. If WDI remains high or low for longer than the watchdog timeout period (1.6s nominal), $\overline{WDO}$, RESET, and $\overline{RESET}$ are asserted (see RESET and $\overline{RESET}$ Outputs section, and the Watchdog Output discussion on this page).

### Watchdog Input

A change of state (high to low, low to high, or a minimum 100ns pulse) at the WDI during the watchdog period resets the watchdog timer. The watchdog default timeout is 1.6s.

To disable the watchdog function, leave WDI floating. An internal resistor network (100kΩ equivalent impedance at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When $V_{CC}$ is below the reset threshold, the watchdog function is disabled and WDI is disconnected from its internal resistor network, thus becoming high impedance.

### Watchdog Output

The Watchdog Output ($\overline{WDO}$) remains high if there is a transition or pulse at WDI during the watchdog timeout period. The watchdog function is disabled and $\overline{WDO}$ is a logic high when $V_{CC}$ is below the reset threshold, battery-backup mode is enabled, or WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watchdog timeout period, RESET and $\overline{RESET}$ are asserted for the reset timeout period (200ms typical). $\overline{WDO}$ goes low and remains low until the next transition at WDI (Figure 2). If WDI is held high or low indefinitely, RESET and $\overline{RESET}$ will generate 200ms pulses every 1.6s. $\overline{WDO}$ has a 2 x TTL output characteristic.

### Selecting an Alternative Watchdog and Reset Timeout Period

The OSC SEL and OSC IN inputs control the watchdog and reset timeout periods. Floating OSC SEL and OSC IN or tying them both to $V_{OUT}$ selects the nominal 1.6s watchdog timeout period and 200ms reset timeout period. Connecting OSC IN to GND and floating or connecting OSC SEL to $V_{OUT}$ selects the 100ms normal watchdog timeout delay and 1.6s delay immediately after reset. The reset timeout delay remains 200ms (Figure 2). Select alternative timeout periods by connecting OSC SEL to GND and connecting a capacitor between OSC IN and GND, or by externally driving OSC IN (Table 1 and Figure 3). OSC IN is internally connected to a ±100nA (typ) current source that charges and discharges the timing capacitor to create the oscillator frequency, which sets the reset and watch-



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## Table 1. Reset Pulse Width and Watchdog Timeout Selections

| OSC SEL | OSC IN | WATCHDOG TIMEOUT PERIOD | | RESET TIMEOUT PERIOD |
|---|---|---|---|---|
| | | NORMAL | IMMEDIATELY AFTER RESET | |
| Low | External Clock Input | 1024 clks | 4096 clks | 2048 clks |
| Low | External Capacitor | (600/47pF x C)ms | (2.4/47pF x C)sec | (1200/47pF x C)ms |
| Floating | Low | 100ms | 1.6s | 200ms |
| Floating | Floating | 1.6s | 1.6s | 200ms |

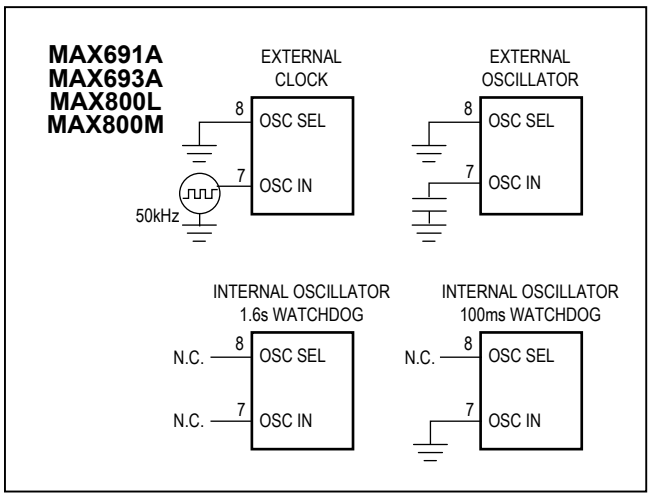


*Figure 3. Oscillator Circuits*

dog timeout periods (see Connecting a Timing Capacitor at OSC IN in the Applications Information section).

## Chip-Enable Signal Gating

The MAX691A/MAX693A/MAX800L/MAX800M provide internal gating of chip-enable (CE) signals to prevent erroneous data from being written to CMOS RAM in the event of a power failure. During normal operation, the CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. All these parts use a series transmission gate from $\overline{CE}$ IN to $\overline{CE}$ OUT (Figure 4).

The 10ns max CE propagation delay from $\overline{CE}$ IN to $\overline{CE}$ OUT enables the parts to be used with most µPs.

### Chip-Enable Input

The Chip-Enable Input ($\overline{CE}$ IN) is high impedance (disabled mode) while RESET and $\overline{RESET}$ are asserted.

During a power-down sequence where $V_{CC}$ falls below the reset threshold or a watchdog fault, $\overline{CE}$ IN assumes a high-impedance state when the voltage at $\overline{CE}$ IN goes high or 15µs after reset is asserted, whichever occurs first (Figure 5).

During a power-up sequence, $\overline{CE}$ IN remains high impedance, regardless of $\overline{CE}$ IN activity, until reset is deasserted following the reset timeout period.

In the high-impedance mode, the leakage currents into this terminal are ±1µA max over temperature. In the low-impedance mode, the impedance of $\overline{CE}$ IN appears as a 75Ω resistor in series with the load at $\overline{CE}$ OUT.

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to $\overline{CE}$ IN and the capacitive loading on the Chip-Enable Output ($\overline{CE}$ OUT) (see Chip-Enable Propagation Delay vs. $\overline{CE}$ OUT Load Capacitance in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point of $\overline{CE}$ IN to the 50% point of $\overline{CE}$ OUT using a 50Ω driver and 50pF of load capacitance (Figure 6). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT, and use a low output-impedance driver.

### Chip-Enable Output

In the enabled mode, the impedance of $\overline{CE}$ OUT is equivalent to 75Ω in series with the source driving $\overline{CE}$ IN. In the disabled mode, the 75Ω transmission gate is off and $\overline{CE}$ OUT is actively pulled to $V_{OUT}$. This source turns off when the transmission gate is enabled.

## $\overline{LOW}$ $\overline{LINE}$ Output

$\overline{LOW}$ $\overline{LINE}$ is the buffered output of the reset threshold comparator. $\overline{LOW}$ $\overline{LINE}$ typically sinks 3.2mA at 0.1V. For normal operation ($V_{CC}$ above the $\overline{LOW}$ $\overline{LINE}$ threshold), $\overline{LOW}$ $\overline{LINE}$ is pulled to $V_{OUT}$.

## Power-Fail Comparator

The power-fail comparator is an uncommitted comparator that has no effect on the other functions of the IC. Common uses include low-battery indication (Figure 7), and early power-fail warning (see *Typical Operating Circuit*).



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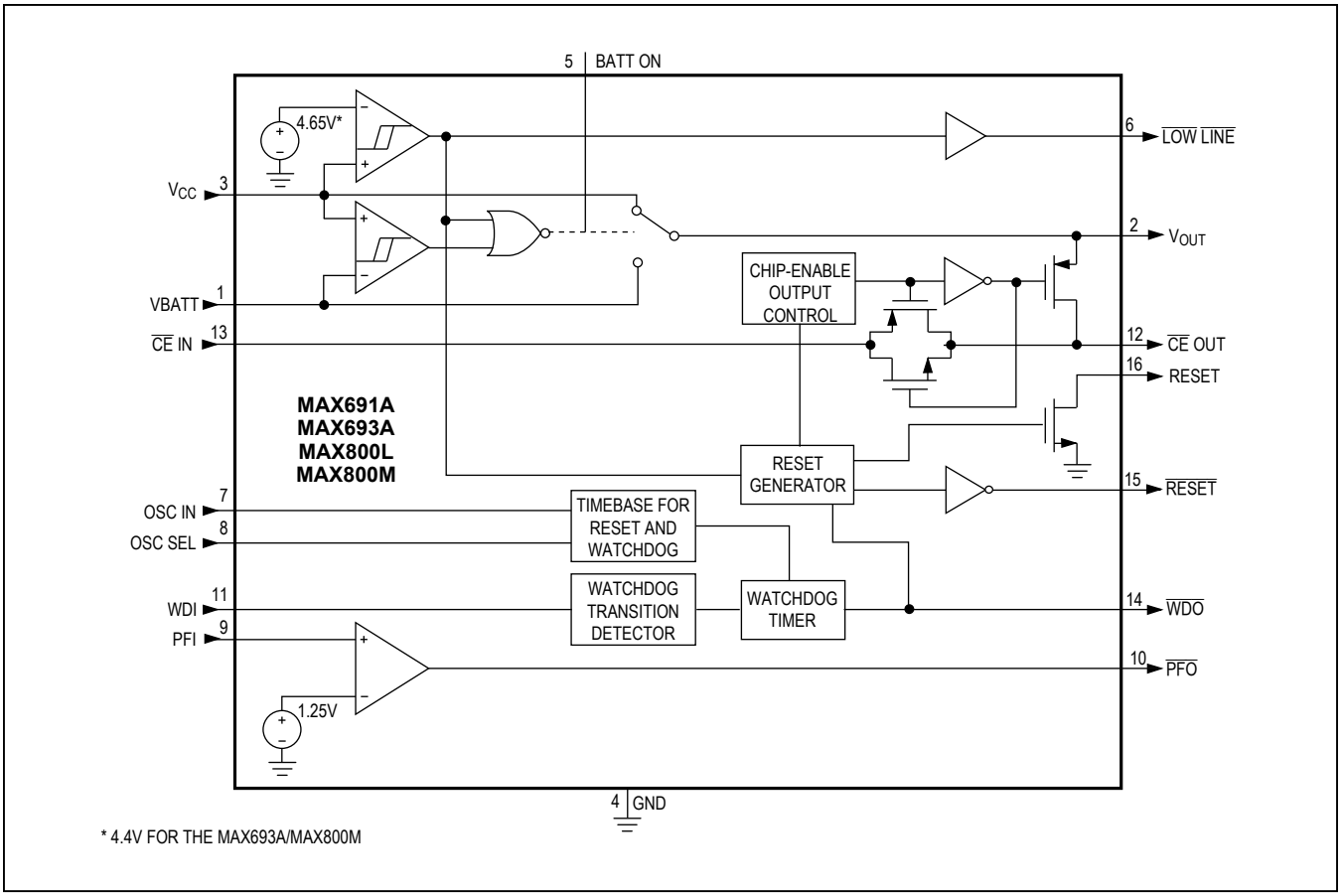


*Figure 4. MAX691A/MAX693A/MAX800L/MAX800M Block Diagram*

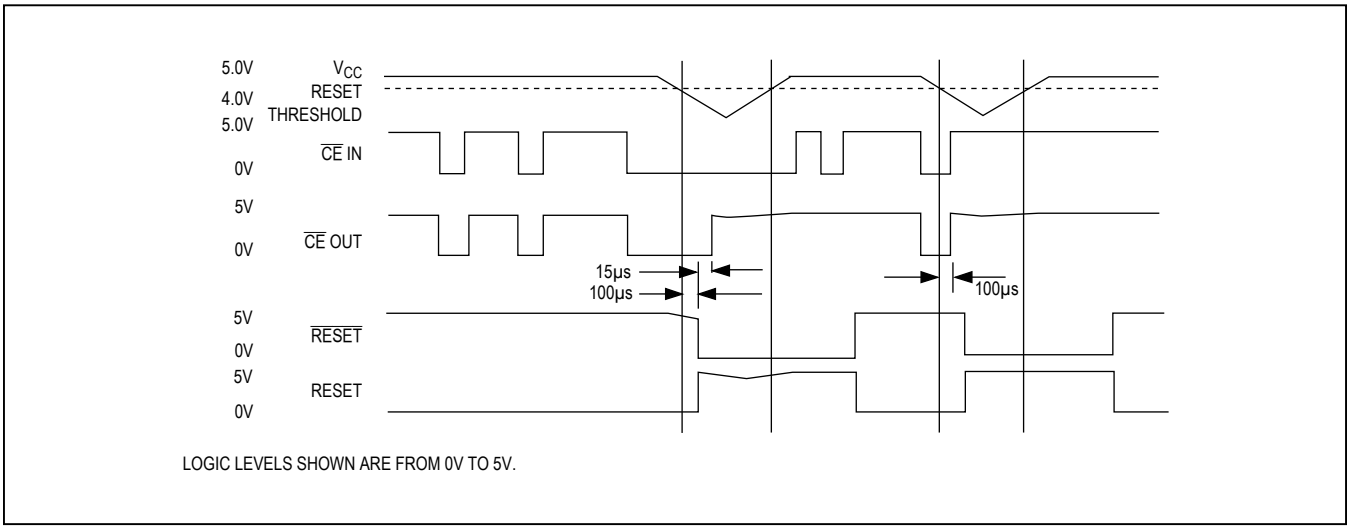


*Figure 5. Reset and Chip-Enable Timing*



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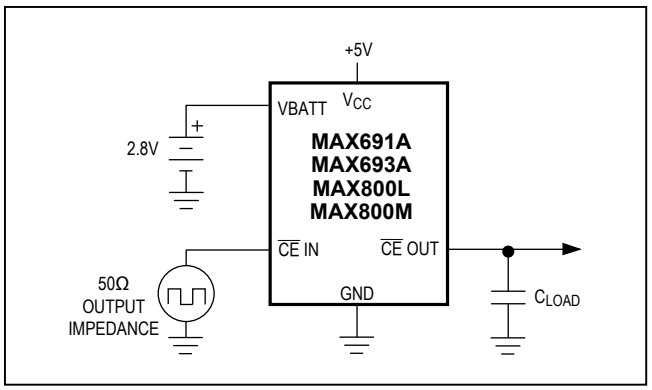


*Figure 6. CE Propagation Delay Test Circuit*

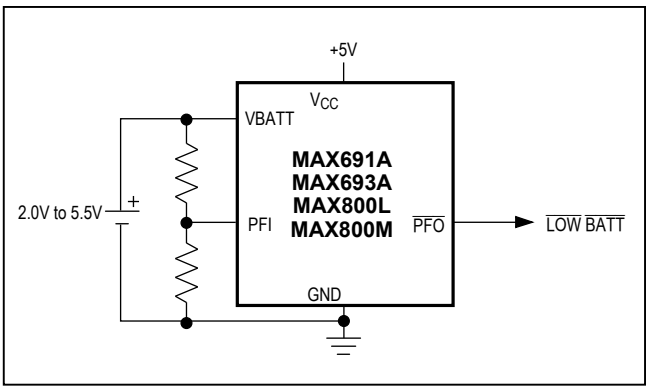


*Figure 7. Low-Battery Indicator*

## Table 2. Input and Output Status in Battery-Backup Mode

| PIN | NAME | STATUS |
|---|---|---|
| 1 | VBATT | Supply current is 1µA max. |
| 2 | $V_{OUT}$ | $V_{OUT}$ is connected to VBATT through an internal PMOS switch. |
| 3 | $V_{CC}$ | Battery switchover comparator monitors $V_{CC}$ for active switchover. |
| 4 | GND | GND 0V, 0V reference for all signals. |
| 5 | BATT ON | Logic high. The open-circuit output is equal to $V_{OUT}$. |
| 6 | $\overline{\text{LOWLINE}}$ | Logic low* |
| 7 | OSC IN | OSC IN is ignored. |
| 8 | OSC SEL | OSC SEL is ignored. |
| 9 | PFI | The power-fail comparator remains active in the battery-backup mode for $V_{CC}$ ≥ VBATT - 1.2V typ. |
| 10 | $\overline{\text{PFO}}$ | The power-fail comparator remains active in the battery-backup mode for $V_{CC}$ ≥ VBATT - 1.2V typ. Below this volt- age, PFO is forced low. |
| 11 | WDI | Watchdog is ignored. |
| 12 | $\overline{\text{CE}}$ OUT | Logic high. The open-circuit voltage is equal to $V_{OUT}$. |
| 13 | $\overline{\text{CE}}$ IN | High impedance |
| 14 | $\overline{\text{WDO}}$ | Logic high. The open-circuit voltage is equal to $V_{OUT}$. |
| 15 | $\overline{\text{RESET}}$ | Logic low* |
| 16 | RESET | High impedance* |

**$V_{CC}$ must be below the reset threshold to enter battery-back-up mode.*

### Power-Fail Input

Power-Fail Input (PFI) is the input to the power-fail comparator. It has a guaranteed input leakage of ±25nA max over temperature. The typical comparator delay is 25µs from $V_{IL}$ to $V_{OL}$ (power failing), and 60µs from $V_{IH}$ to $V_{OH}$ (power being restored). If PFI is not used, connect it to ground.

### Power-Fail Output

The Power-Fail Output ($\overline{\text{PFO}}$) goes low when PFI goes below 1.25V. It typically sinks 3.2mA with a saturation voltage of 0.1V. With PFI above 1.25V, $\overline{\text{PFO}}$ is actively pulled to $V_{OUT}$.

### Battery-Backup Mode

Two conditions are required to switch to battery-backup mode: 1) $V_{CC}$ must be below the reset threshold, and 2) $V_{CC}$ must be below VBATT. Table 2 lists the status of the inputs and outputs in battery-backup mode.

### Battery-On Output

The Battery-On (BATT ON) output indicates the status of the internal $V_{CC}$/battery-switchover comparator, which controls the internal $V_{CC}$ and VBATT switches. For $V_{CC}$ greater than VBATT (ignoring the small hysteresis effect), BATT ON typically sinks 3.2mA at 0.1V saturation voltage. In battery-backup mode, this terminal sources approximately 10µA from $V_{OUT}$. Use BATT ON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher-current applications (see Typical Operating Circuit).

### Input Supply Voltage

The Input Supply Voltage ($V_{CC}$) should be a regulated 5V. $V_{CC}$ connects to $V_{OUT}$ via a parallel diode and a large PMOS switch. The switch carries the entire cur-rent



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load for currents less than 250mA. The parallel diode carries any current in excess of 250mA. Both the switch and the diode have impedances less than 1Ω each. The maximum continuous current is 250mA, but power-on transients may reach a maximum of 1A.

### Battery-Backup Input

The Battery-Backup Input (VBATT) is similar to the $V_{CC}$ input except the PMOS switch and parallel diode are much smaller. Accordingly, the on-resistances of the diode and the switch are each approximately 10Ω. Continuous current should be limited to 25mA and peak currents (only during power-up) limited to 250mA. The reverse leakage of this input is less than 1µA over temperature and supply voltage (Figure 8).

### Output Supply Voltage

The Output Supply Voltage ($V_{OUT}$) pin is internally connected to the substrate of the IC and supplies current to the external system and internal circuitry. All opencircuit outputs will, for example, assume the $V_{OUT}$ voltage in their high states rather than the $V_{CC}$ voltage. At the maximum source current of 250mA, $V_{OUT}$ will typically be 200mV below $V_{CC}$. Decouple this terminal with a 0.1µF capacitor.

## Applications Information

The MAX691A/MAX693A/MAX800L/MAX800M are not short-circuit protected. Shorting $V_{OUT}$ to ground, other than power-up transients such as charging a decoupling capacitor, destroys the device.

All open-circuit outputs swing between $V_{OUT}$ and GND rather than $V_{CC}$ and GND.

If long leads connect to the chip inputs, insure that these leads are free from ringing and other conditions that would forward bias the chip's protection diodes.

There are three distinct modes of operation:

1) Normal operating mode with all circuitry powered up. Typical supply current from $V_{CC}$ is 35µA while only leakage currents flow from the battery.
2) Battery-backup mode where $V_{CC}$ is typically within 0.7V below VBATT. All circuitry is powered up and the supply current from the battery is typically less than 60µA.
3) Battery-backup mode where $V_{CC}$ is less than VBATT by at least 0.7V. VBATT supply current is 1µA max.

### Using SuperCap or MaxCap with the MAX691A/MAX693A/MAX800L/MAX800M

VBATT has the same operating voltage range as $V_{CC}$, and the battery switchover threshold voltages are typically ±30mV centered at VBATT, allowing use of a SuperCap and a simple charging circuit as a backup source (Figure 9).

If $V_{CC}$ is above the reset threshold and VBATT is 0.5V above $V_{CC}$, current flows to $V_{OUT}$ and $V_{CC}$ from VBATT until the voltage at VBATT is less than 0.5V above $V_{CC}$. For example, with a SuperCap connected to VBATT and through a diode to $V_{CC}$, if $V_{CC}$ quickly changes from 5.4V to 4.9V, the capacitor discharges through $V_{OUT}$ and $V_{CC}$ until VBATT reaches 5.1V typ. Leakage current through the SuperCap charging diode and the internal power diode eventually discharges the SuperCap to $V_{CC}$. Also, if $V_{CC}$ and VBATT start from 0.1V above the reset thresh-

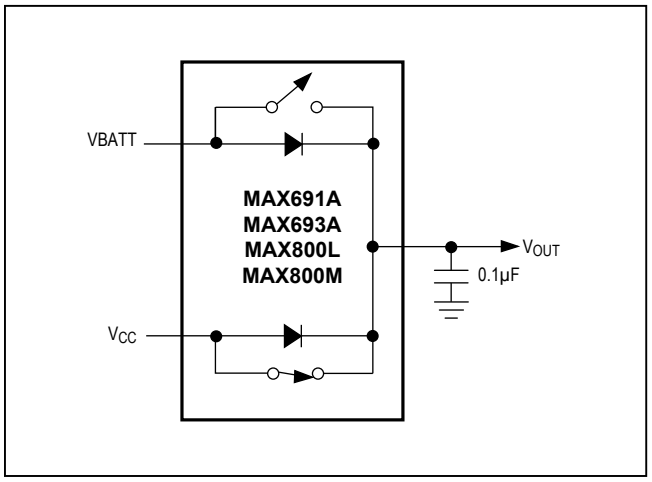


*Figure 8. $V_{CC}$ and VBATT to VOUT Switch*

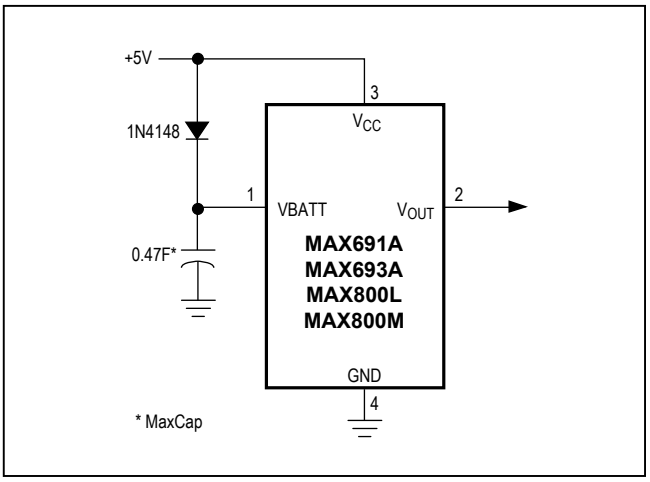


*Figure 9. SuperCap or MaxCap on VBATT*



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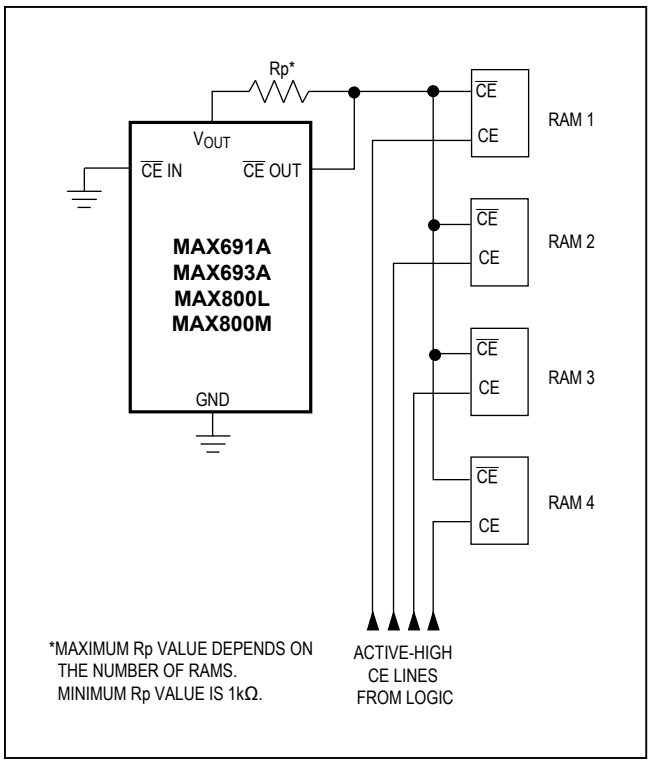


*Figure10. Alternate CE Gating*

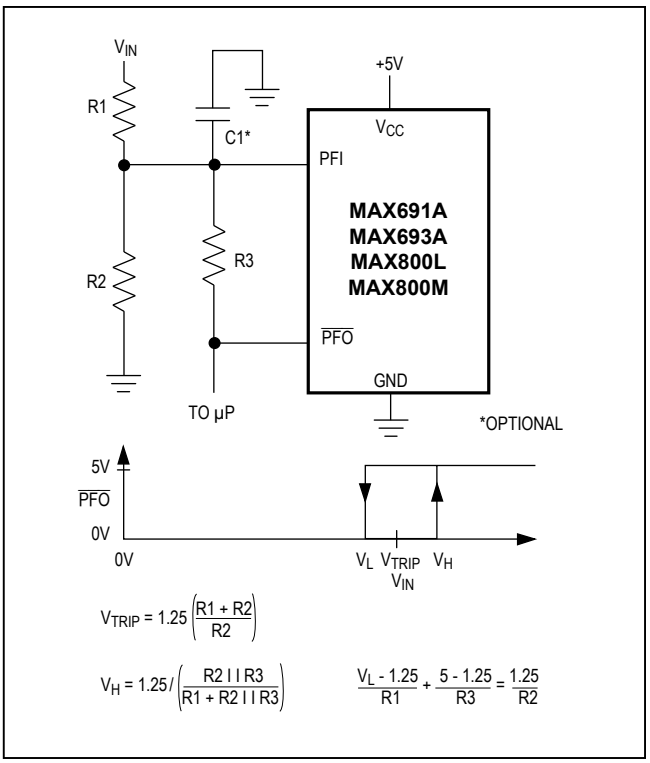


*Figure 11. Adding Hysteresis to the Power-Fail Comparator*

old and power is lost at $V_{CC}$, the SuperCap on VBATT discharges through $V_{CC}$ until VBATT reaches the reset threshold; then the battery-backup mode is initiated and the current through $V_{CC}$ goes to zero.

## Using Separate Power Supplies for VBATT and $V_{CC}$

If using separate power supplies for $V_{CC}$ and VBATT, VBATT must be less than 0.3V above $V_{CC}$ when $V_{CC}$ is above the reset threshold. As described in the previous section, if VBATT exceeds this limit and power is lost at $V_{CC}$, current flows continuously from VBATT to $V_{CC}$ via the VBATT-to-$V_{OUT}$ diode and the $V_{OUT}$-to-$V_{CC}$ switch until the circuit is broken (Figure 8).

## Alternate Chip-Enable Gating

Using memory devices with both CE and $\overline{CE}$ inputs allows the CE loop to be bypassed. To do this, connect $\overline{CE}$ IN to ground, pull up $\overline{CE}$ OUT to $V_{OUT}$, and connect $\overline{CE}$ OUT to the $\overline{CE}$ input of each memory device (Figure 10). The CE input of each part then connects directly to the chip-select logic, which does not have to be gated.

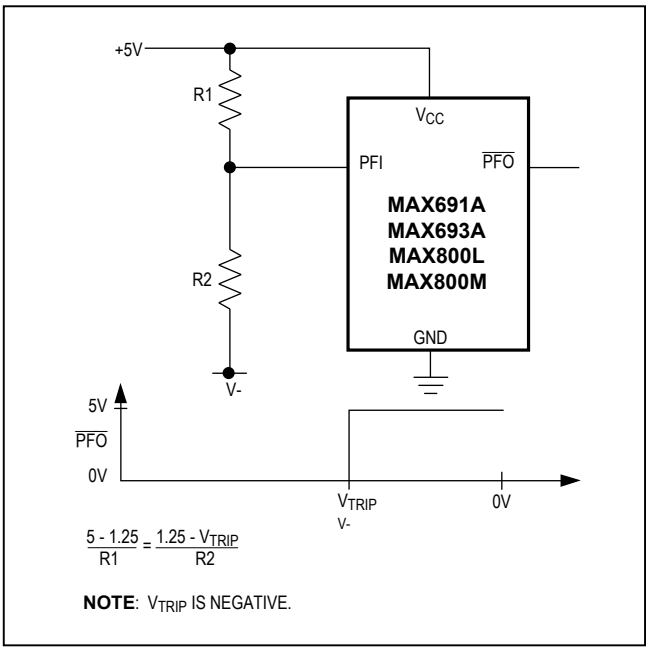


*Figure 12. Monitoring a Negative Voltage*



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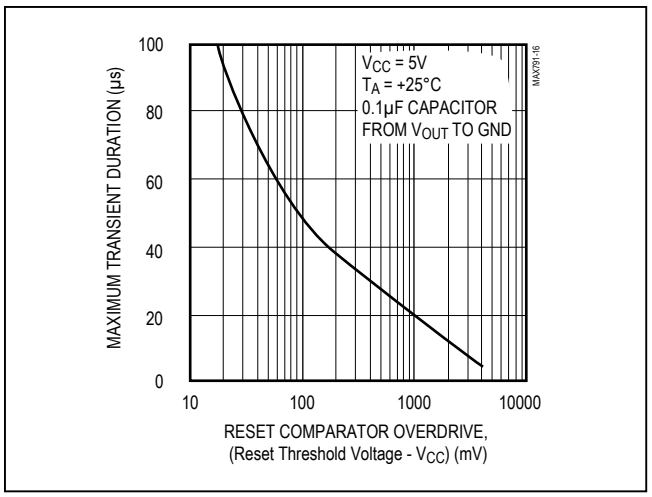


*Figure 13. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdriv*

## Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of $\overline{PFO}$ when $V_{IN}$ is near the power-fail comparator trip point. Figure 11 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when $V_{IN}$ falls to the desired trip point ($V_{TRIP}$). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds noise rejection.

## Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 12's circuit. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage drops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the $V_{CC}$ voltage, and resistors R1 and R2.

## Backup-Battery Replacement

The backup battery may be disconnected while $V_{CC}$ is above the reset threshold. No precautions are necessary to avoid spurious reset pulses.

## Negative-Going $V_{CC}$ Transients

While issuing resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration, negative-going $V_{CC}$ transients (glitches). It is usually undesirable to reset the µP when $V_{CC}$ experiences only small glitches.

Figure 13 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are **not** generated. The graph was produced using negativegoing $V_{CC}$ pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going $V_{CC}$ transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a $V_{CC}$ transient that goes 100mV below the reset threshold and lasts for 40µs or less will not cause a reset pulse to be issued.

A 100nF bypass capacitor mounted close to the $V_{CC}$ pin provides additional transient immunity.

## Connecting a Timing Capacitor at OSC IN

When OSC SEL is connected to ground, OSC IN disconnects from its internal 10µA (typ) pullup and is internally connected to a ±100nA current source. When a capacitor is connected from OSC IN to ground (to select alternative reset and watchdog timeout periods), the current source charges and discharges the timing capacitor to create the oscillator that controls the reset and watchdog timeout period. To prevent timing errors or oscillator startup prob-



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lems, minimize external current leakage sources at this pin, and locate the capacitor as close to OSC IN as possible. The sum of PC-board leakage plus OSC capacitor leakage must be small compared to ±100nA.

## Maximum $V_{CC}$ Fall Time

The $V_{CC}$ fall time is limited by the propagation delay of the battery switchover comparator and should not exceed 0.03V/µs. A standard rule of thumb for filter capacitance on most regulators is on the order of 100µF per amp of current. When the power supply is shut off or the main battery is disconnected, the associated initial $V_{CC}$ fall rate is just the inverse or 1A/100µF = 0.01V/µs. The $V_{CC}$ fall rate decreases with time as $V_{CC}$ falls exponentially, which more than satisfies the maximum fall-time requirement.

## Watchdog Software Considerations

A way to help the watchdog timer keep a closer watch on software execution involves setting and resetting the watchdog input at different points in the program, rather than “pulsing” the watchdog input high-low-high or low-high-low. This technique avoids a “stuck” loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out. Figure 14 shows an example flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should “hang” in any subroutine, the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

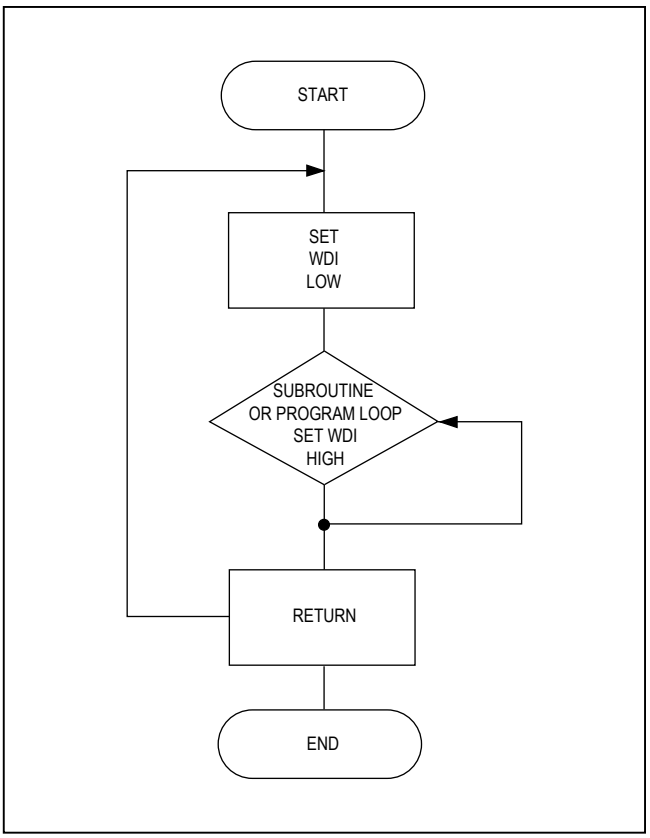


*Figure 14. Watchdog Flow Diagram*



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## Ordering Information (continued)

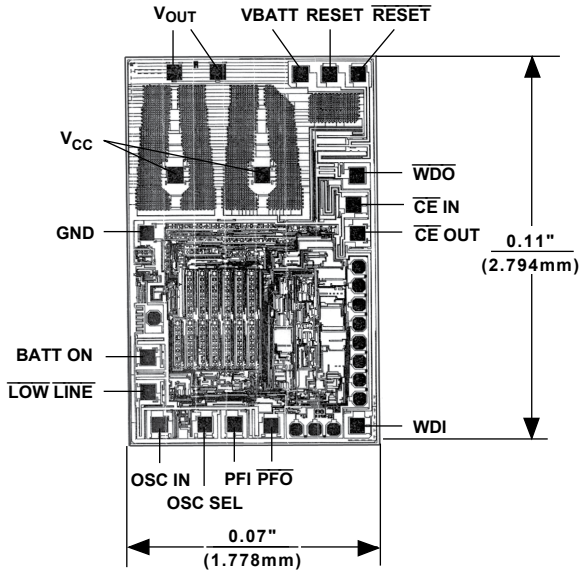
| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX691AEJE | -40°C to +85°C | 16 CERDIP |
| MAX691AMJE | -55°C to +125°C | 16 CERDIP** |
| MAX691AMSE/PR | -55°C to +125°C | 16 Wide SO** |
| MAX691AMSE/PR-T | -55°C to +125°C | 16 Wide SO** |
| **MAX693A**CUE | -0°C to +70°C | 16 TSSOP |
| MAX693ACSE | -0°C to +70°C | 16 Narrow SO |
| MAX693ACWE | -0°C to +70°C | 16 Wide SO |
| MAX693ACPE | -0°C to +70°C | 16 Plastic DIP |
| MAX693AC/D | -0°C to +70°C | Dice* |
| MAX693AEUE | -40°C to +85°C | 16 TSSOP |
| MAX693AESE | -40°C to +85°C | 16 Narrow SO |
| MAX693AEWE | -40°C to +85°C | 16 Wide SO |
| MAX693AEPE | -40°C to +85°C | 16 Plastic DIP |
| MAX693AEJE | -40°C to +85°C | 16 CERDIP |
| MAX693AMJE | -55°C to +125°C | 16 CERDIP |
| **MAX800L**CUE | -0°C to +70°C | 16 TSSOP |
| MAX800LCSE | -0°C to +70°C | 16 Narrow SO |
| MAX800LCPE | -0°C to +70°C | 16 Plastic DIP |
| MAX800LEUE | -40°C to +85°C | 16 TSSOP |
| MAX800LESE | -40°C to +85°C | 16 Narrow SO |
| MAX800LEPE | -40°C to +85°C | 16 Plastic DIP |
| **MAX800M**CUE | -0°C to +70°C | 16 TSSOP |
| MAX800MCSE | -0°C to +70°C | 16 Narrow SO |
| MAX800MCPE | -0°C to +70°C | 16 Plastic DIP |
| MAX800MEUE | -40°C to +85°C | 16 TSSOP |
| MAX800MESE | -40°C to +85°C | 16 Narrow SO |
| MAX800MEPE | -40°C to +85°C | 16 Plastic DIP |

**Dice are specified at $T_A$ = +25°C, DC parameters only.*

***Contact factory for availability and processing to MIL-STD-883B.*

*Devices in PDIP, SO and TSSOP packages are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering. Lead free not available for CERDIP package.*

## Chip Topography




SUBSTRATE CONNECTED TO $V_{OUT}$

## Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PKG CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 16 TSSOP | U16-1 | 21-0066 | 90-0117 |
| 16 CERDIP | J16-3 | 21-0045 | — |
| 16 Narrow SO | S16-3 | 21-0041 | 90-0097 |
| 16 Plastic DIP | P16-1 | 21-0043 | — |
| 16 Wide SO | W16-1 | 21-0042 | 90-0107 |



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## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 09/92 | Initial release | — |
| 1 | 12/92 | Update *Electrical Characteristics* table. | 2, 3, 4 |
| 2 | 5/93 | Update *Electrical Characteristics* table, Tables 1 and 2. | 2, 3, 4, 9, 11 |
| 3 | 12/93 | Update *Electrical Characteristics* table. | 2, 3, 4 |
| 4 | 3/94 | Update *Electrical Characteristics* table. | 2, 3, 4 |
| 5 | 8/94 | Correction to Figure 4. | 10 |
| 6 | 1/95 | Update to new revision and correct errors. | — |
| 7 | 12/96 | Update *Electrical Characteristics* table. | 2, 3, 4 |
| 8 | 12/99 | Updated *Ordering Information*, *Pin Configuration*, *Absolute Maximum Ratings*, and *Package Information*. | 1, 2, 16 |
| 9 | 4/02 | Corrected *Ordering Information*. | 1 |
| 10 | 11/05 | Added lead-free information. | 1, 16 |
| 11 | 8/08 | Updated *Ordering Information*. | 1, 16 |
| 12 | 9/14 | No /V OPNs; removed automotive reference from *Applications* section; updated *Package Information* table | 1, 16 |
| 13 | 11/17 | Updated *Electrical Characteristics* table | 2 |

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