SOT23, Low-Power µP Supervisory Circuits with Battery Backup and Chip-Enable Gating

ABSOLUTE MAXIMUM RATINGS

Terminal Voltages (with respect to GND)
V_{CC}, BATT, OUT .....-0.3V to +6V
$\overline{RESET}$ (open drain), RESET (open drain) .....-0.3V to +6V
BATT ON, $\overline{RESET}$ (push-pull), RESET IN,
WDI, $\overline{CE}$ IN, $\overline{CE}$ OUT .....-0.3V to (V_{OUT} + 0.3V)
$\overline{MR}$ .....-0.3V to (V_{CC} + 0.3V)
Input Current
V_{CC} Peak 1A
V_{CC} Continuous 250mA
BATT Peak 250mA
BATT Continuous 40mA
GND 75mA

Output Current
OUT .....Short-Circuit Protected for up to 10s
RESET, $\overline{RESET}$, BATT ON, $\overline{CE}$ OUT 20mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 8.75mW/°C above +70°C).....700mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Lead (Pb)-free packages.....+260°C
Packages containing lead (Pb).....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.4V to +5.5V, V_{BATT} = +3.0V, $\overline{CE}$ IN = V_{CC}, reset not asserted, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 2)	V_{CC}, V_{BATT}	No load		0		5.5	V
Supply Current (Excluding I_{OUT})	I_{CC}	No load, V_{CC} > V_{TH}	V_{CC} = 2.8V		10	30	µA
			V_{CC} = 3.6V		12	35	
			V_{CC} = 5.5V		15	50	
Supply Current in Battery-Backup Mode (Excluding I_{OUT})	I_{BACK}	V_{BATT} = 2.8V, V_{CC} = 0V	T_A = +25°C			1	µA
			T_A = -40°C to +85°C			3	
BATT Standby Current	I_{BATT}	5.5V > V_{CC} > (V_{BATT} + 0.2V)	T_A = +25°C	-0.10		+0.02	µA
			T_A = -40°C to +85°C	-1.00		+0.05	
V_{CC} to OUT On-Resistance	R_{ON}	V_{CC} = 4.75V, I_{OUT} = 150mA				3.1	Ω
		V_{CC} = 3.15V, I_{OUT} = 65mA				3.7	
		V_{CC} = 2.38V, I_{OUT} = 25mA				4.6	
Output Voltage in Battery-Backup Mode	V_{OUT}	V_{BATT} = 4.5V, I_{OUT} = 20mA		V_{BATT} - 0.2			V
		V_{BATT} = 3.0V, I_{OUT} = 10mA		V_{BATT} - 0.15			
		V_{BATT} = 2.25V, I_{OUT} = 5mA		V_{BATT} - 0.15			
Battery-Switchover Threshold (V_{CC} - V_{BATT})	V_{SW}	V_{CC} < V_{TH}	Power-up		20		mV
			Power-down		-20		
Reset Threshold	V_{TH}	MAX636__KA46		4.50	4.63	4.75	V
		MAX636__KA44		4.25	4.38	4.50	
		MAX636__KA31		3.00	3.08	3.15	
		MAX636__KA29		2.85	2.93	3.00	
		MAX636__KA26		2.55	2.63	2.70	
		MAX636__KA23		2.25	2.32	2.38	
V_{CC} Falling Reset Delay	t_{RD}	V_{CC} falling at 10V/ms			20		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.4V to +5.5V, V_{BATT} = +3.0V, $\overline{CE}$ IN = V_{CC}, reset not asserted, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reset Active Timeout Period	t_{RP}			150		280	ms
$\overline{RESET}$ Output Voltage	V_{OL}	Reset asserted, V_{BATT} = 0V	I_{SINK} = 1.6mA, $V_{CC} \geq$ 2.1V			0.3	V
			I_{SINK} = 100µA, $V_{CC} \geq$ 1.2V			0.4	
	V_{OH}	Reset not asserted (MAX636_L only)	I_{SOURCE} = 500µA, $V_{CC} \geq V_{TH(MAX)}$	0.8 × V_{CC}			
RESET Output Voltage	V_{OL}	Reset not asserted	I_{SINK} = 1.6mA, $V_{CC} \geq V_{TH\ (MAX)}$			0.3	V
	V_{OH}	Reset not asserted, V_{BATT} = 0V (MAX636_H only) (Note 3)	I_{SOURCE} = 1mA, $V_{CC} \geq$ 1.8V	0.7 × V_{CC}			
			I_{SOURCE} = 200µA, $V_{CC} \geq$ 1.2V	0.8 × V_{CC}			
$\overline{RESET}$ Output Leakage Current	I_{LKG}	MAX636_P and MAX636_H only				1	µA
MANUAL RESET (MAX6365 only)							
$\overline{MR}$ Input Voltage	V_{IL}					0.3 × V_{CC}	V
	V_{IH}			0.7 × V_{CC}			
Pullup Resistance				20			kΩ
Minimum Pulse Width				1			µs
Glitch Immunity		V_{CC} = 3.3V			100		ns
$\overline{MR}$ to Reset Delay		V_{CC} = 3.3V			120		ns
WATCHDOG (MAX6366 only)							
Watchdog Timeout Period	t_{WD}			1.00	1.65	2.25	s
Minimum WDI Input Pulse Width	t_{WDI}			100			ns
WDI Input Voltage	V_{IL}					0.3 × V_{CC}	V
	V_{IH}			0.7 × V_{CC}			
WDI Input Current				-1.0		1.0	µA
BATT ON (MAX6367 only)							
Output Voltage	V_{OL}	I_{SINK} = 3.2mA, V_{BATT} = 2.1V				0.4	V
Output Short-Circuit Current		Sink current, V_{CC} = 5V			60		mA
		Source current, $V_{BATT} \geq$ 2V		10	30	100	µA

SOT23, Low-Power µP Supervisory Circuits with Battery Backup and Chip-Enable Gating

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.4V to +5.5V, V_{BATT} = +3.0V, $\overline{CE}$ IN = V_{CC}, reset not asserted, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

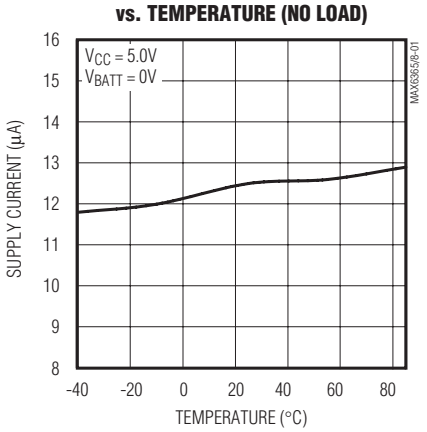
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESET IN (MAX6368 only)							
RESET IN Threshold	V_{RTH}			1.185	1.235	1.285	V
RESET IN Leakage Current					±0.01	±25	nA
RESET IN to Reset Delay		V_{OD} = 50mV, RESET IN falling			1.5		µs
CHIP-ENABLE GATING							
$\overline{CE}$ IN Leakage Current		Reset asserted				±1	µA
$\overline{CE}$ IN to $\overline{CE}$ OUT Resistance		Reset not asserted (Note 4)			20	100	Ω
$\overline{CE}$ OUT Short-Circuit Current		Reset asserted, $V_{\overline{CE}\ OUT}$ = 0V			0.75	2.0	mA
$\overline{CE}$ IN to $\overline{CE}$ OUT Propagation Delay		50Ω source, C_{LOAD} = 6365 50pF	V_{CC} = 4.75V		1.5	7	ns
			V_{CC} = 3.15V		2	9	
$\overline{CE}$ OUT Output Voltage High		V_{CC} = 5V, $V_{CC} \geq V_{BATT}$, I_{SOURCE} = 100µA		0.8 × V_{CC}			V
		V_{CC} = 0V, $V_{BATT} \geq$ 2.2V, I_{SOURCE} = 1µA		V_{BATT} - 0.1			
Reset-to-$\overline{CE}$ OUT Delay					12		µs

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 2: V_{BATT} can be 0V anytime, or V_{CC} can go down to 0V if V_{BATT} is active (except at startup).
Note 3: RESET is pulled up to OUT. Specifications apply for OUT = V_{CC} or OUT = BATT.
Note 4: The chip-enable resistance is tested with V_{CC} = $V_{TH(MAX)}$ and $V_{\overline{CE}\ IN}$ = V_{CC}/2.

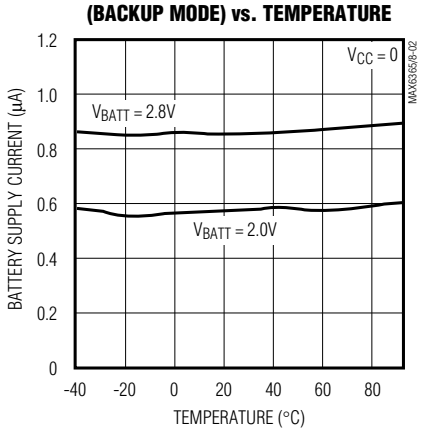
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

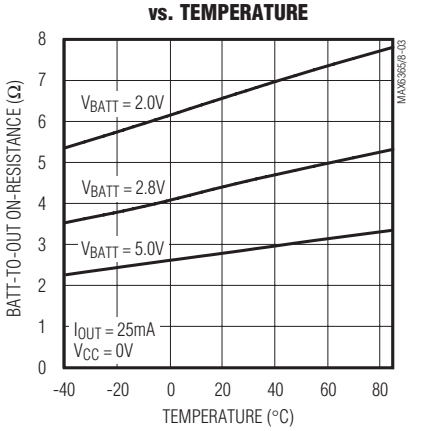
SUPPLY CURRENT vs. TEMPERATURE (NO LOAD)



BATTERY SUPPLY CURRENT (BACKUP MODE) vs. TEMPERATURE



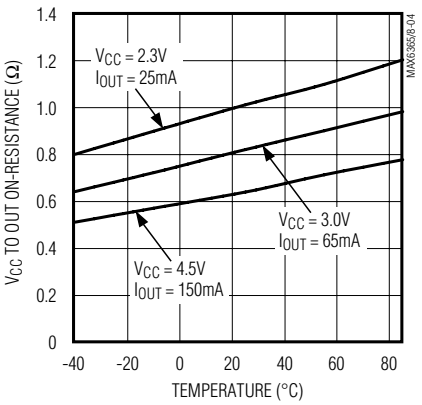
BATT-TO-OUT ON-RESISTANCE vs. TEMPERATURE



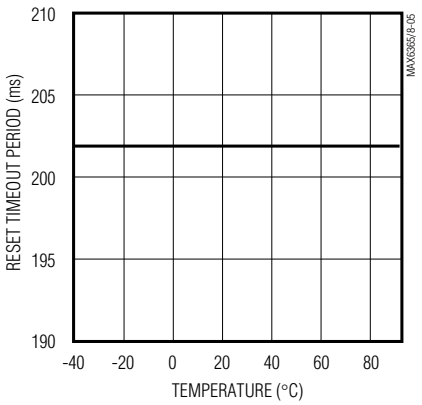
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

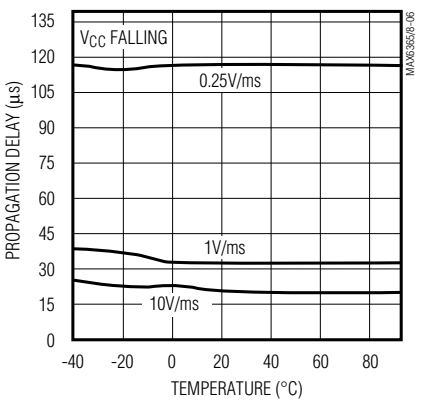
V_{CC} TO OUT ON-RESISTANCE vs. TEMPERATURE



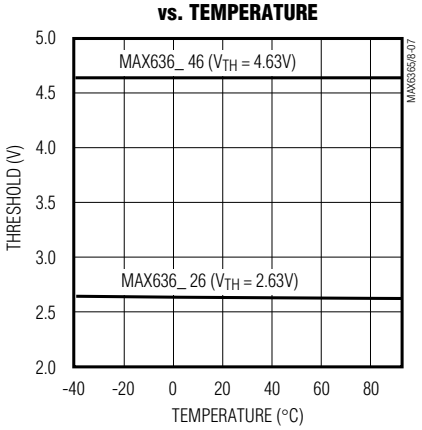
RESET TIMEOUT PERIOD vs. TEMPERATURE



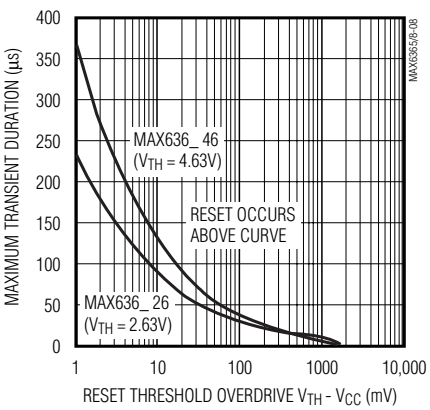
V_{CC} TO $\overline{RESET}$ PROPAGATION DELAY vs. TEMPERATURE



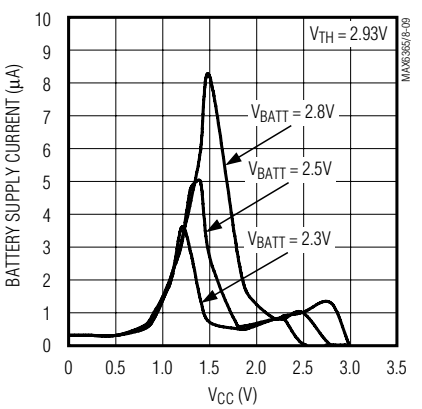
RESET THRESHOLD vs. TEMPERATURE



MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



BATTERY SUPPLY CURRENT vs. SUPPLY VOLTAGE

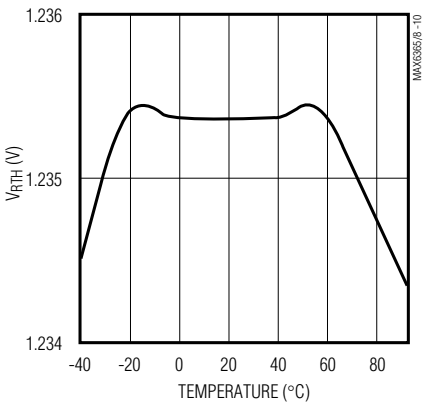


SOT23, Low-Power µP Supervisory Circuits with Battery Backup and Chip-Enable Gating

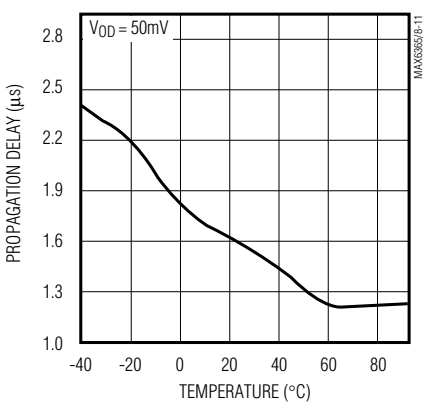
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

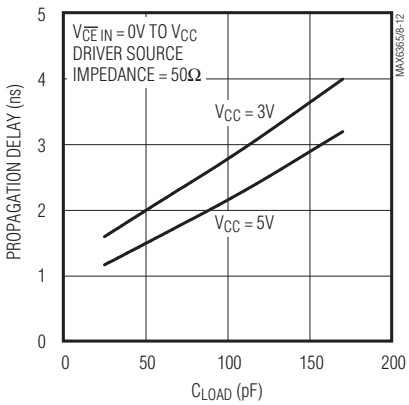
MAX6368
RESET IN THRESHOLD vs. TEMPERATURE



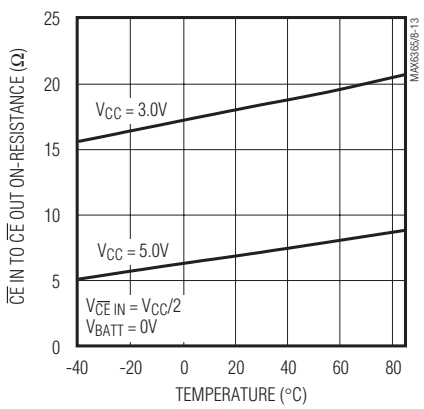
MAX6368
RESET IN TO RESET PROPAGATION DELAY vs. TEMPERATURE



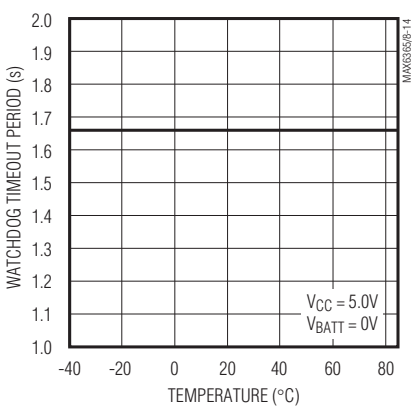
CHIP-ENABLE PROPAGATION DELAY vs. $\overline{CE}$ OUT LOAD CAPACITANCE



$\overline{CE}$ IN TO $\overline{CE}$ OUT ON-RESISTANCE vs. TEMPERATURE



MAX6366
WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE

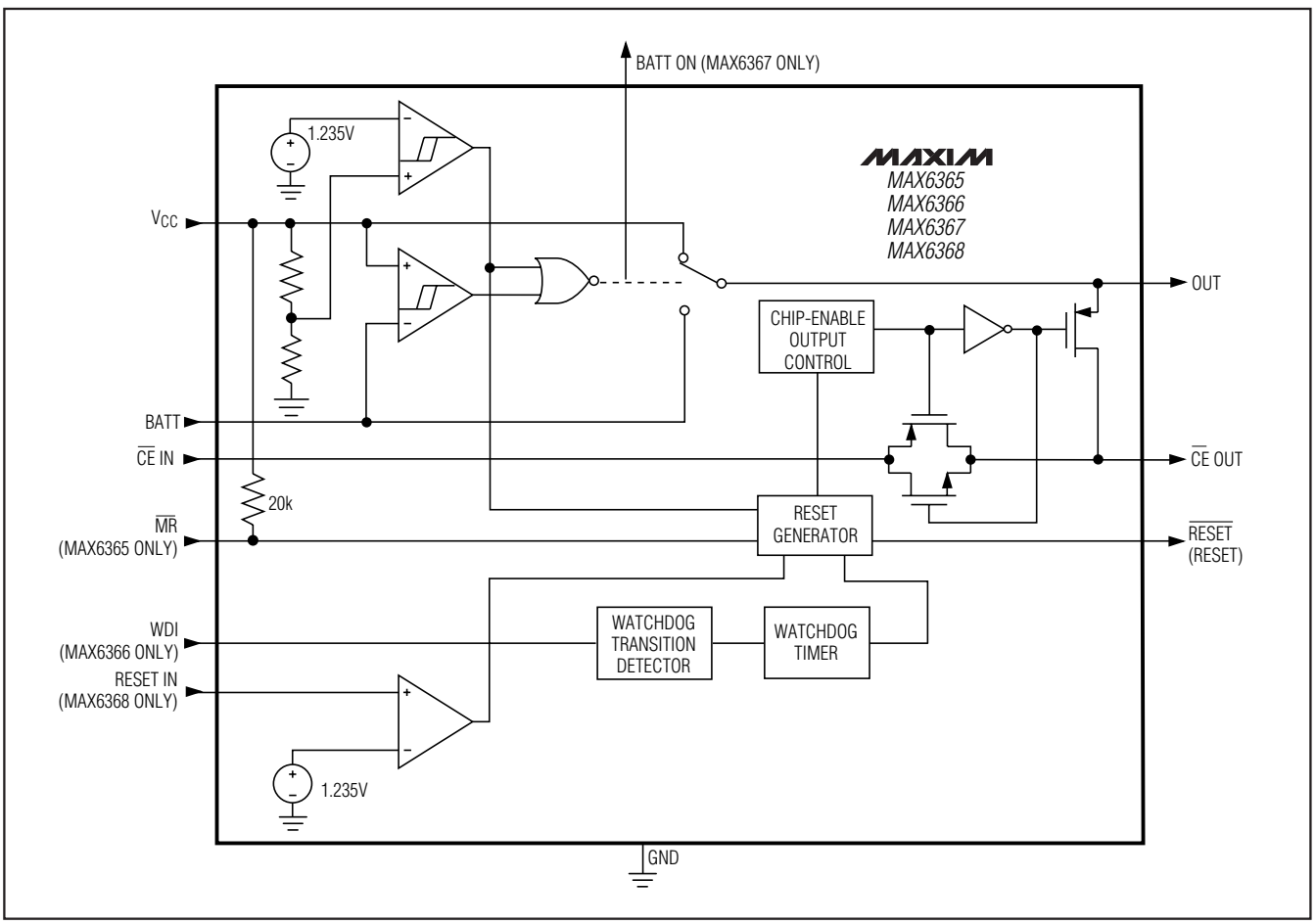


Pin Description

PIN	NAME	FUNCTION
1	RESET	Active-High Reset Output. RESET asserts high continuously when V_{CC} is below the reset threshold (V_{TH}), $\overline{MR}$ is low, or RESET IN is low. It asserts in pulses when the internal watchdog times out. RESET remains asserted for the reset timeout period (t_{RP}) after V_{CC} rises above the reset threshold, after the manual reset input goes from low to high, after RESET IN goes high, or after the watchdog triggers a reset event. RESET is an open-drain active-high reset output.
	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ asserts low continuously when V_{CC} is below the reset threshold (V_{TH}), the manual reset input is low, or RESET IN is low. It asserts low in pulses when the internal watchdog times out. $\overline{RESET}$ remains asserted low for the reset timeout period (t_{RP}) after V_{CC} rises above the reset threshold, after the manual reset input goes from low to high, after RESET IN goes high, or after the watchdog triggers a reset event. The MAX636_L is an active-low push-pull output, while the MAX636_P is an active-low open-drain output.
2	$\overline{CE}$ IN	Chip-Enable Input. The input to chip-enable gating circuitry. Connect to GND or OUT if not used.
3	GND	Ground
4	$\overline{MR}$	**MAX6365** Manual-Reset Input. Maintaining logic low on $\overline{MR}$ asserts a reset. Reset output remains asserted as long as $\overline{MR}$ is low and for the reset timeout period (t_{RP}) after $\overline{MR}$ transitions from low to high. Leave unconnected, or connect to V_{CC} if not used. $\overline{MR}$ has an internal 20kΩ pullup to V_{CC}.
	WDI	**MAX6366** Watchdog Input. If WDI remains high or low for longer than the watchdog timeout period (t_{WD}), the internal watchdog timer runs out and a reset pulse is triggered for the reset timeout period (t_{RP}). The internal watchdog clears whenever reset asserts or whenever WDI sees a rising or falling edge (Figure 2).
	BATT ON	**MAX6367** Battery-On Output. BATT ON goes high when in battery-backup mode.
	RESET IN	**MAX6368** Reset Input. When RESET IN falls below 1.235V, reset asserts. Reset output remains asserted as long as RESET IN is low and for at least t_{RP} after RESET IN goes high.
5	V_{CC}	Supply Voltage, 1.2V to 5.5V. Reset asserts when V_{CC} drops below the reset threshold voltage (V_{TH}). Reset remains asserted until V_{CC} rises above V_{TH} and for at least t_{RP} after V_{CC} rises above V_{TH}.
6	OUT	Output. OUT sources from V_{CC} when not in reset and from the greater of V_{CC} or BATT when V_{CC} is below the reset threshold.
7	BATT	Backup-Battery Input. When V_{CC} falls below the reset threshold, OUT switches to BATT if V_{BATT} is 20mV greater than V_{CC}. When V_{CC} rises 20mV above V_{BATT}, OUT switches to V_{CC}. The 40mV hysteresis prevents repeated switching if V_{CC} falls slowly.
8	$\overline{CE}$ OUT	Chip-Enable Output. $\overline{CE}$ OUT goes low only when $\overline{CE}$ IN is low and reset is not asserted. If $\overline{CE}$ IN is low when reset is asserted, $\overline{CE}$ OUT will stay low for 12µs (typ) or until $\overline{CE}$ IN goes high, whichever occurs first.

SOT23, Low-Power µP Supervisory Circuits with Battery Backup and Chip-Enable Gating

Functional Diagram



Detailed Description

The *Typical Operating Circuit* shows a typical connection for the MAX6365–MAX6368. OUT powers the static random-access memory (SRAM). If V_{CC} is greater than the reset threshold (V_{TH}), or if V_{CC} is lower than V_{TH} but higher than V_{BATT}, V_{CC} is connected to OUT. If V_{CC} is lower than V_{TH} and V_{CC} is less than V_{BATT}, BATT is connected to OUT. OUT supplies up to 150mA from V_{CC}. In battery-backup mode, an internal MOSFET connects the backup battery to OUT. The on-resistance of the MOSFET is a function of backup-battery voltage and is shown in the BATT-to-OUT On-Resistance vs. Temperature graph in the *Typical Operating Characteristics*.

Chip-Enable Signal Gating

The MAX6365–MAX6368 provide internal gating of $\overline{CE}$ signals to prevent erroneous data from being written to CMOS RAM in the event of a power failure. During normal operation, the $\overline{CE}$ gate is enabled and passes all $\overline{CE}$ transitions. When reset asserts, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. All of these devices use a series transmission gate from $\overline{CE}$ IN to $\overline{CE}$ OUT. The 2ns propagation delay from $\overline{CE}$ IN to $\overline{CE}$ OUT allows the devices to be used with most µPs and high-speed DSPs.

During normal operation, $\overline{CE}$ IN is connected to $\overline{CE}$ OUT through a low on-resistance transmission gate. This is valid when reset is not asserted. If $\overline{CE}$ IN is high when reset is asserted, $\overline{CE}$ OUT remains high regardless of any subsequent transitions on $\overline{CE}$ IN during the reset event.

If $\overline{CE}$ IN is low when reset is asserted, $\overline{CE}$ OUT is held low for 12µs to allow completion of the read/write operation (Figure 1). After the 12µs delay expires, the $\overline{CE}$

OUT goes high and stays high regardless of any subsequent transitions on $\overline{CE}$ IN during the reset event. When $\overline{CE}$ OUT is disconnected from $\overline{CE}$ IN, $\overline{CE}$ OUT is actively pulled up to OUT.

The propagation delay through the chip-enable circuitry depends on both the source impedance of the drive to $\overline{CE}$ IN and the capacitive loading at $\overline{CE}$ OUT. The chip-enable propagation delay is production tested from the 50% point of $\overline{CE}$ IN to the 50% point of $\overline{CE}$ OUT, using a 50Ω driver and 50pF load capacitance. Minimize the capacitive load at $\overline{CE}$ OUT to minimize propagation delay, and use a low-output-impedance driver.

Backup-Battery Switchover

In a brownout or power failure, it may be necessary to preserve the contents of the RAM. With a backup battery installed at BATT, the MAX6365–MAX6368 automatically switch the RAM to backup power when V_{CC} falls. The MAX6367 has a BATT ON output that goes high in battery-backup mode. These devices require two conditions before switching to battery-backup mode:

1) V_{CC} must be below the reset threshold.

2) V_{CC} must be below V_{BATT}.

Table 1 lists the status of the inputs and outputs in battery-backup mode. The devices do not power up if the only voltage source is on BATT. OUT only powers up from V_{CC} at startup.

Table 1. Input and Output Status in Battery-Backup Mode

PIN	STATUS
V_{CC}	Disconnected from OUT
OUT	Connected to BATT
BATT	Connected to OUT. Current drawn from the battery is less than 1µA (at V_{BATT} = 2.8V, excluding I_{OUT}) when V_{CC} = 0V.
RESET/$\overline{RESET}$	Asserted
BATT ON	High state
$\overline{MR}$, RESET IN, $\overline{CE}$ IN, WDI	Inputs ignored
$\overline{CE}$ OUT	Connected to OUT

Manual Reset Input (MAX6365 Only)

Many µP-based products require manual reset capability, allowing the user or external logic circuitry to initiate a reset. For the MAX6365, a logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low and for a minimum of 150ms (t_{RP}) after it returns high. $\overline{MR}$ has an internal 20kΩ pullup resistor to V_{CC}. This input can be driven with TTL/CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity.

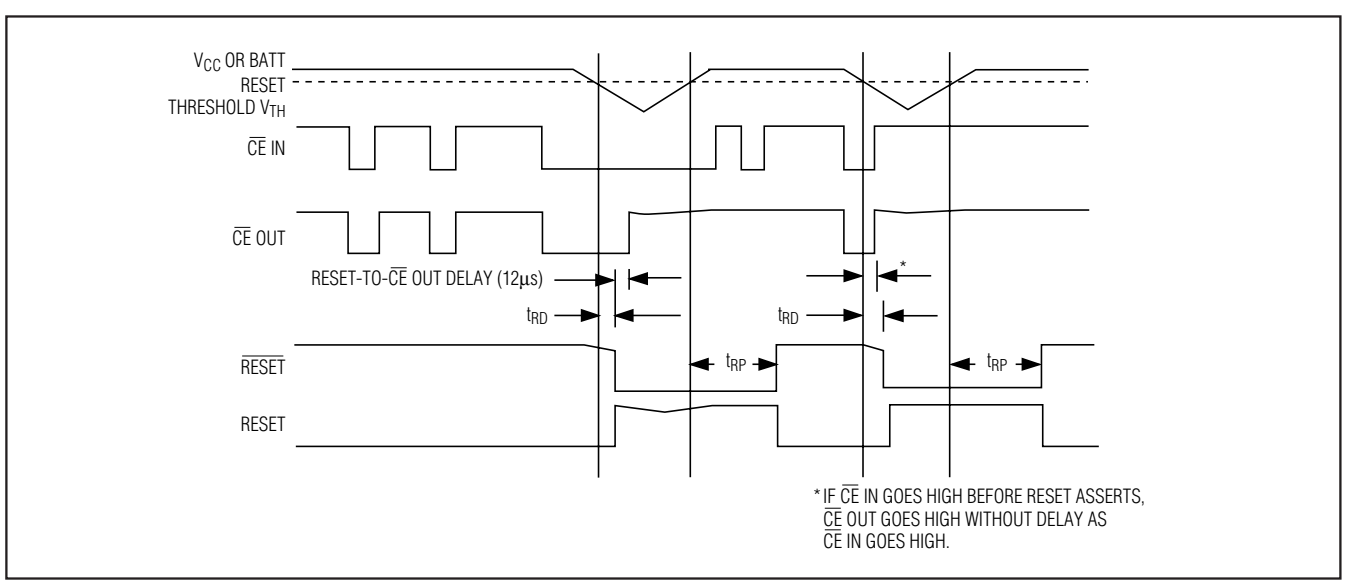


Figure 1. Reset and Chip-Enable Timing

SOT23, Low-Power µP Supervisory Circuits with Battery Backup and Chip-Enable Gating

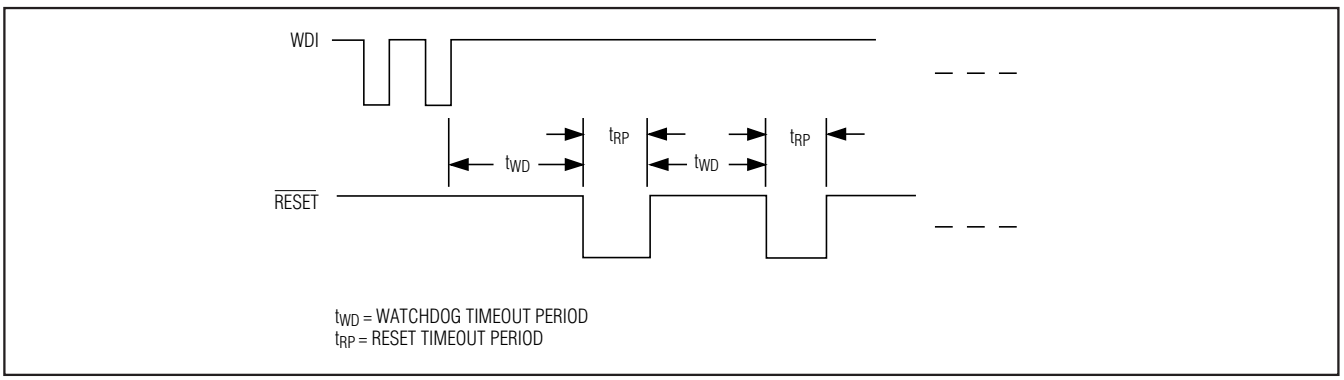


Figure 2. MAX6366 Watchdog Timeout Period and Reset Active Time

Watchdog Input (MAX6366 Only)

The watchdog monitors µP activity through the watchdog input (WDI). If the µP becomes inactive, reset asserts. To use the watchdog function, connect WDI to a bus line or µP I/O line. A change of state (high to low, low to high, or a minimum 100ns pulse) resets the watchdog timer. If WDI remains high or low for longer than the watchdog timeout period (t_{WD}), the internal watchdog timer runs out and a reset pulse is triggered for the reset timeout period (t_{RP}). The internal watchdog timer clears whenever reset asserts or whenever WDI sees a rising or falling edge. If WDI remains in either a high or low state, a reset pulse asserts periodically after every t_{WD} (Figure 2).

BATT ON Indicator (MAX6367 Only)

BATT ON is a push-pull output that drives high when in battery-backup mode. BATT ON typically sinks 3.2mA at 0.1V saturation voltage. In battery-backup mode, this terminal sources approximately 10µA from OUT. Use BATT ON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher current applications (Figure 3).

RESET IN Comparator (MAX6368 Only)

RESET IN is compared to an internal 1.235V reference. If the voltage at RESET IN is less than 1.235V, reset asserts. Use the RESET IN comparator as an undervoltage detector to signal a failing power supply or as a secondary power-supply reset monitor.

To program the reset threshold (V_{RTH}) of the secondary power supply, use the following (see *Typical Operating Circuit*):

$$V_{RTH} = V_{REF} (R1 / R2 + 1)$$

where V_{REF} = 1.235V. To simplify the resistor selection, choose a value for R2 and calculate R1:

$$R1 = R2 [(V_{RTH} / V_{REF}) - 1]$$

Since the input current at RESET IN is 25nA (max), large values (up to 1MΩ) can be used for R2 with no significant loss in accuracy. For example, in the *Typical Operating Circuit*, the MAX6368 monitors two supply voltages. To monitor the secondary 5V logic or analog supply with a 4.60V nominal programmed reset threshold, choose R2 = 100kΩ, and calculate R1 = 273kΩ.

Reset Output

A µP's reset input starts the µP in a known state. The MAX6365–MAX6368 µP supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. RESET is guaranteed to be a logic low or logic high, depending on the device chosen (see the *Ordering Information*). RESET or $\overline{RESET}$ asserts when V_{CC} is below the reset threshold and for at least 150ms (t_{RP}) after V_{CC} rises above the reset threshold. RESET or $\overline{RESET}$ also asserts when $\overline{MR}$ is low (MAX6365) and when RESET IN is less than 1.235V (MAX6368). The MAX6366 watchdog function will cause RESET (or $\overline{RESET}$) to assert in pulses following a watchdog timeout (Figure 2).

Applications Information

Operation Without a Backup Power Source

The MAX6365–MAX6368 provide battery-backup functions. If a backup power source is not used, connect BATT to GND and OUT to V_{CC}.

Watchdog Software Considerations

One way to help the watchdog timer monitor the software execution more closely is to set and reset the watchdog at different points in the program rather than pulsing the watchdog input periodically. Figure 4 shows a flow diagram in which the I/O driving the watchdog is set low in the beginning of the program, set high at the beginning of every subroutine or loop, and set low again when the program returns to the beginning. If the program should hang in any subroutine, the problem would be quickly corrected.

Replacing the Backup Battery

When V_{CC} is above V_{TH}, the backup power source can be removed without danger of triggering a reset pulse. The device does not enter battery-backup mode when V_{CC} stays above the reset threshold voltage.

Negative-Going V_{CC} Transients

These supervisors are relatively immune to short-duration, negative-going V_{CC} transients. Resetting the µP when V_{CC} experiences only small glitches is usually not desirable.

The *Typical Operating Characteristics* section has a Maximum Transient Duration vs. Reset Threshold Overdrive graph for which reset is not asserted. The graph was produced using negative-going V_{CC} pulses, starting at V_{CC} and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient can typically have without triggering a reset pulse. As the amplitude of the transient increases (i.e., goes further below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 30µs will not trigger a reset pulse.

A 0.1µF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

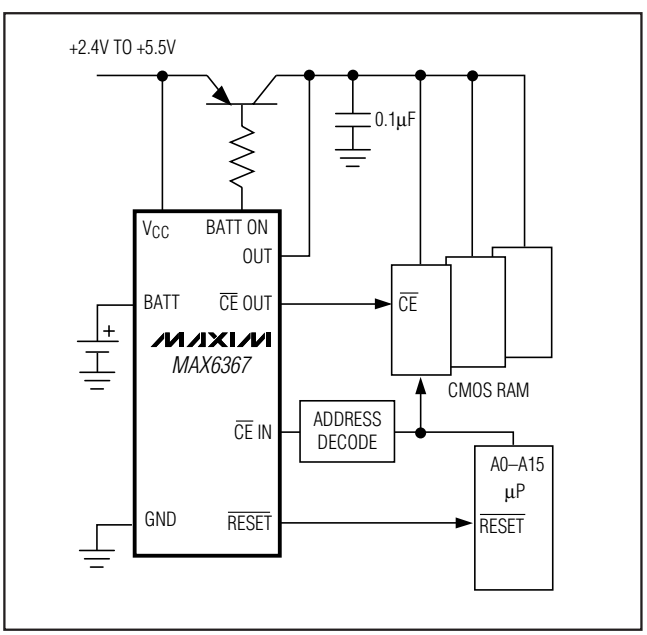


Figure 3. MAX6367 BATT ON Driving an External Pass Transistor

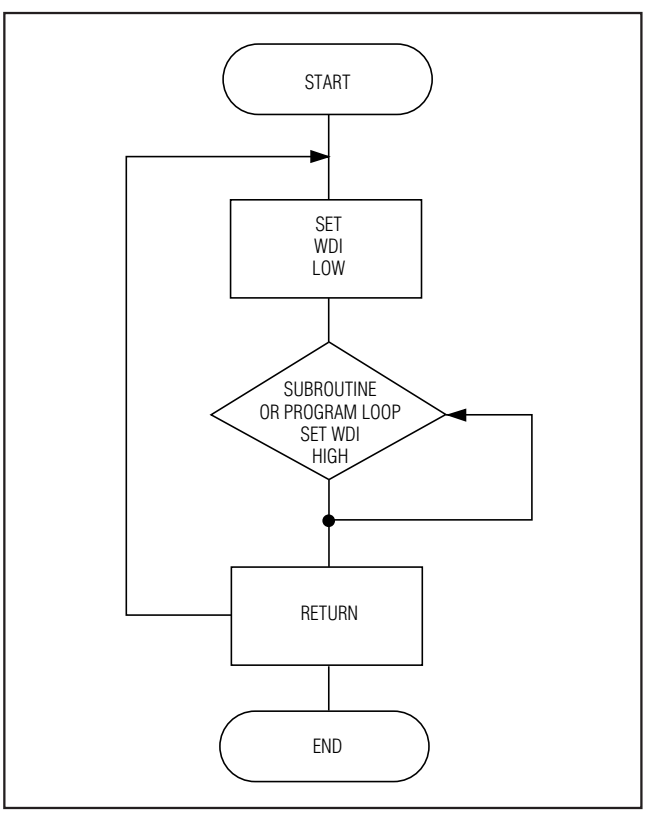


Figure 4. Watchdog Flow Diagram

SOT23, Low-Power µP Supervisory Circuits with Battery Backup and Chip-Enable Gating

Reset Threshold Ranges

SUFFIX	RESET THRESHOLD RANGES (V)		
	MIN	TYP	MAX
46	4.50	4.63	4.75
44	4.25	4.38	4.50
31	3.00	3.08	3.15
29	2.85	2.93	3.00
26	2.55	2.63	2.70
23	2.25	2.32	2.38

Device Marking Codes

PART	TOP MARK	PART	TOP MARK	PART	TOP MARK
MAX6365LKA23	AAAM	MAX6366PKA23	AABK	MAX6367HKA23	AACI
MAX6365LKA26	AAAL	MAX6366PKA26	AABJ	MAX6367HKA26	AACH
MAX6365LKA29*	AAAK	MAX6366PKA29*	AABI	MAX6367HKA29	AACG
MAX6365LKA31	AAAJ	MAX6366PKA31	AABH	MAX6367HKA31	AACF
MAX6365LKA44	AAAI	MAX6366PKA44	AABG	MAX6367HKA44	AACE
MAX6365LKA46*	AAAH	MAX6366PKA46*	AABF	MAX6367HKA46*	AACD
MAX6365PKA23	AAAS	MAX6366HKA23	AABQ	MAX6368LKA23	AACO
MAX6365PKA26	AAAR	MAX6366HKA26	AABP	MAX6368LKA26	AACN
MAX6365PKA29*	AAAQ	MAX6366HKA29	AABO	MAX6368LKA29*	AACM
MAX6365PKA31	AAAP	MAX6366HKA31	AABN	MAX6368LKA31	AACL
MAX6365PKA44	AAAO	MAX6366HKA44	AABM	MAX6368LKA44	AACK
MAX6365PKA46*	AAAN	MAX6366HKA46*	AABL	MAX6368LKA46*	AACJ
MAX6365HKA23	AAAY	MAX6367LKA23	AABW	MAX6368PKA23	AACU
MAX6365HKA26	AAAX	MAX6367LKA26	AABV	MAX6368PKA26	AACT
MAX6365HKA29	AAAW	MAX6367LKA29*	AABU	MAX6368PKA29*	AACS
MAX6365HKA31	AAAV	MAX6367LKA31	AABT	MAX6368PKA31	AACR
MAX6365HKA44	AAAU	MAX6367LKA44	AABS	MAX6368PKA44	AACQ
MAX6365HKA46*	AAAT	MAX6367LKA46*	AABR	MAX6368PKA46*	AACP
MAX6366LKA23	AABE	MAX6367PKA23	AACC	MAX6368HKA23	AADA
MAX6366LKA26	AABD	MAX6367PKA26	AACB	MAX6368HKA26	AACZ
MAX6366LKA29*	AABC	MAX6367PKA29*	AACA	MAX6368HKA29	AACY
MAX6366LKA31	AABB	MAX6367PKA31	AABZ	MAX6368HKA31	AACX
MAX6366LKA44	AABA	MAX6367PKA44	AABY	MAX6368HKA44	AACW
MAX6366LKA46*	AAAZ	MAX6367PKA46*	AABX	MAX6368HKA46*	AACV

**These standard versions are available in small quantities through Maxim Distribution. Sample stock is generally held on standard versions only. Contact factory for availability of nonstandard versions.*

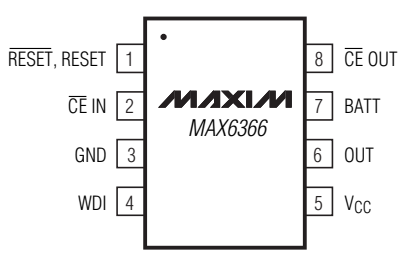
SOT23, Low-Power µP Supervisory Circuits with Battery Backup and Chip-Enable Gating

Selector Guide

PART	MANUAL RESET INPUT	WATCH-DOG INPUT	BATT ON	RESET IN	$\overline{\text{RESET}}$ PUSH-PULL	$\overline{\text{RESET}}$ OPEN-DRAIN	RESET OPEN-DRAIN	CHIP-ENABLE GATING
MAX6365LKA__	✓				✓			✓
MAX6365PKA__	✓					✓		✓
MAX6365HKA__	✓						✓	✓
MAX6366LKA__		✓			✓			✓
MAX6366PKA__		✓				✓		✓
MAX6366HKA__		✓					✓	✓
MAX6367LKA__			✓		✓			✓
MAX6367PKA__			✓			✓		✓
MAX6367HKA__			✓				✓	✓
MAX6368LKA__				✓	✓			✓
MAX6368PKA__				✓		✓		✓
MAX6368HKA__				✓			✓	✓

Pin Configurations (continued)

TOP VIEW



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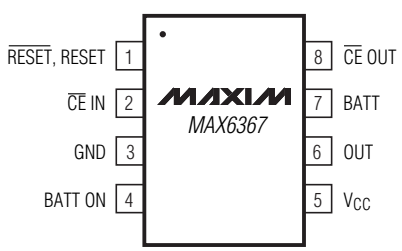

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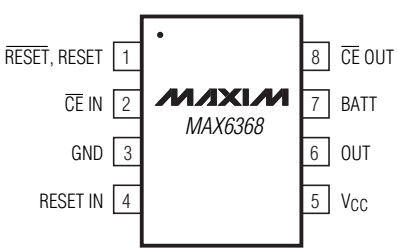

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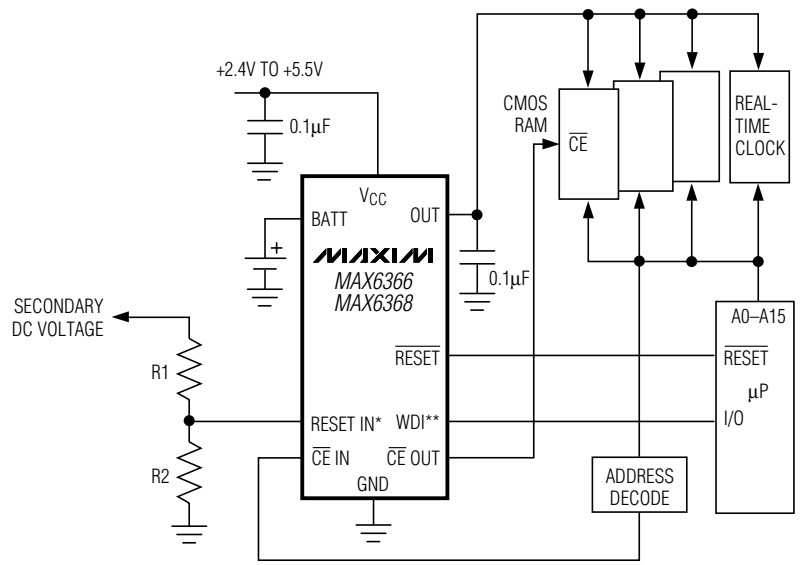
SOT23, Low-Power µP Supervisory Circuits with Battery Backup and Chip-Enable Gating

Typical Operating Circuit



Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SOT23	K8SN-1	21-0078	90-0176

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	5/09	Added automotive part number to *Ordering Information* table	1
5	10/11	Updated the *Electrical Characteristics*.	2