128-Tap, Nonvolatile, Linear-Taper Digital Potentiometer in 2mm x 2mm µDFN Package

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6.0V
UP and DN to GND .....-0.3V to (V_{CC} + 0.3V)
H, L, and W to GND.....-0.3V to (V_{CC} + 0.3V)
Maximum Continuous Current into H, L, and W .....±0.5mA
Maximum Continuous Current into All Other Pins .....±50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin µDFN (derate 4.7mW/°C above +70°C) 376.5mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.25V, H = V_{CC}, L = GND, T_A = -40°C to +85°C. Typical values are at V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE (voltage-divider mode)						
Resolution	N		7			Bits
Integral Nonlinearity	INL	(Note 2)			±1.0	LSB
Differential Nonlinearity	DNL	(Note 2)			±1.0	LSB
End-to-End Resistance Temperature Coefficient	TC_R			50		ppm/°C
Ratiometric Resistance Temperature Coefficient				5		ppm/°C
Full-Scale Error	FSE		-3		0	LSB
Zero-Scale Error	ZSE		0		+2	LSB
DC PERFORMANCE (variable-resistor mode)						
Integral Nonlinearity	INL	(Note 3)			±1.75	LSB
Differential Nonlinearity	DNL	(Note 3)			±1	LSB
DC PERFORMANCE (resistor characteristics)						
Wiper Resistance	R_W	(Note 4)		0.6	0.8	kΩ
Wiper Capacitance	C_W			20		pF
End-to-End Resistance	R_{HL}		16	22	27	kΩ
DIGITAL INPUTS (UP, DN)						
Input-High Voltage (Note 5)	V_{IH}	3.4V ≤ V_{CC} ≤ 5.25V	2.4			V
		2.7V ≤ V_{CC} < 3.4V	0.7 x V_{CC}			
Input-Low Voltage	V_{IL}	(Note 5)			0.8	V
Input Leakage Current	I_{IN}				±1	µA
Input Capacitance	C_{IN}			5		pF
DYNAMIC CHARACTERISTICS						
Wiper -3dB Bandwidth	f_{3dB}	(Note 6)		400		kHz
THD Plus Noise	THD+N	V_H = 0.3V_{RMS}, f = 1kHz, wiper set to midscale		0.02		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.25V, H = V_{CC}, L = GND, T_A = -40°C to +85°C. Typical values are at V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NONVOLATILE MEMORY RELIABILITY						
Data Retention		T_A = +85°C		50		Years
Endurance		T_A = +25°C		80,000		Stores
		T_A = +85°C		50,000		
POWER SUPPLY						
Supply Voltage	V_{CC}		2.70		5.25	V
Average Programming Current	I_{PG}	During nonvolatile write only; digital inputs = V_{CC} or GND		220	400	µA
Peak Programming Current	I_{PK}	During nonvolatile write only; digital inputs = V_{CC} or GND		4		mA
Standby Current	I_{CC}	Digital inputs = V_{CC} or GND, T_A = +25°C		0.5	1.5	µA

TIMING CHARACTERISTICS

(V_{CC} = +2.7V to +5.25V, H = V_{CC}, L = GND, T_A = -40°C to +85°C. Typical values are at V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.) (See Figures 1, 2, 3, and 4).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG SECTION						
Wiper Settling Time	t_S	(Note 7)		500		ns
DIGITAL SECTION						
UP or DN Pulse-Width High	t_{PWH}		80			ns
UP or DN Pulse-Width Low	t_{PWL}		80			ns
UP or DN Glitch Immunity	t_{IMMU}		20			ns
UP Fall to DN Rise Setup or DN Fall to UP Rise Setup	t_{MS1}		80			ns
Before Entering NVM-Write Mode, UP Fall to UP Rise	t_{MS2}		80			ns
UP Rise to DN Rise Setup when Entering NVM-Write	t_{WS}		80			ns
UP Fall to DN Fall Hold or DN Fall to UP Fall Hold during NVM-Write	t_{WH}		0			ns

128-Tap, Nonvolatile, Linear-Taper Digital Potentiometer in 2mm x 2mm µDFN Package

TIMING CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.25V, H = V_{CC}, L = GND, T_A = -40°C to +85°C. Typical values are at V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.) (See Figures 1, 2, 3, and 4).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NVM-Write Mode Pulse-Width High	t_{WP}		80			ns
Write NV Register Busy Time	t_{BUSY}				14	ms
Power-Up Settling Time	t_{ACC}	(Note 8)		2		µs

Note 1: All devices are production tested at T_A = +25°C and are guaranteed by design for T_A = -40°C to +85°C.

Note 2: The DNL and INL are measured with the potentiometer configured as a voltage-divider with H = V_{CC} and L = GND. The wiper terminal is unloaded and measured with a high input-impedance voltmeter.

Note 3: The DNL and INL are measured with the potentiometer configured as a variable resistor. H is unconnected and L = GND. For the +5V condition, the wiper terminal is driven with a source current of 200µA and for the +2.7V condition, the wiper terminal is driven with a source current of 100µA.

Note 4: The wiper resistance is measured using the source currents given in Note 3.

Note 5: The device draws higher supply current when the digital inputs are driven with voltages between (V_{CC} - 0.5V) and (GND + 0.5V). See Supply Current vs. Digital Input Voltage in the *Typical Operating Characteristics*.

Note 6: Wiper at midscale with a 10pF load, L = GND, an AC source is applied to H, and the output is measured as 3dB lower than the DC W/H value in dB.

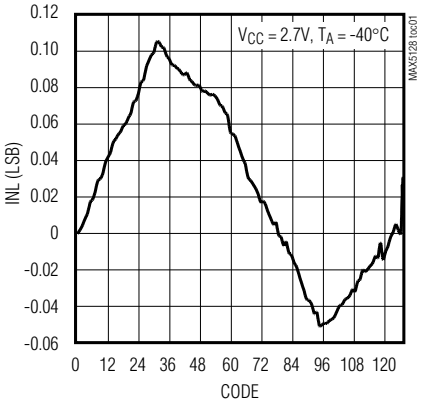
Note 7: Wiper-settling time is the worst-case 0 to 50% rise time measured between consecutive wiper positions. H = V_{CC}, L = GND, and the wiper terminal is unloaded and measured with a 10pF oscilloscope probe. See the Tap-to-Tap Switching Transient in the *Typical Operating Characteristics* section.

Note 8: Power-up settling time is measured from the time V_{CC} = 2.7V to the wiper settling to 1 LSB of the final value.

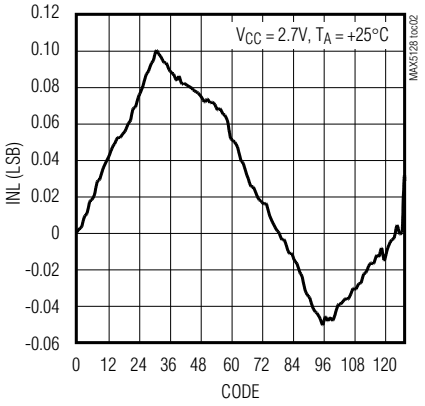
Typical Operating Characteristics

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

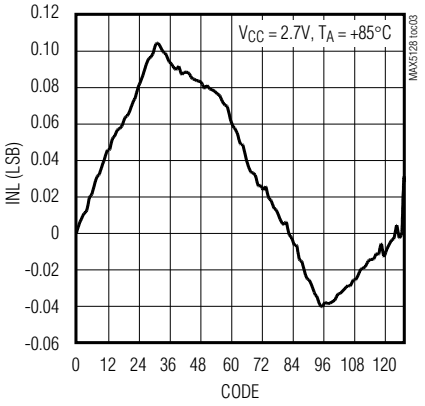
INTEGRAL NONLINEARITY vs. CODE (VOLTAGE-DIVIDER)



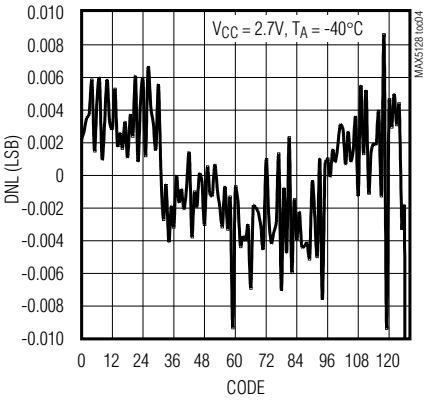
INTEGRAL NONLINEARITY vs. CODE (VOLTAGE-DIVIDER)



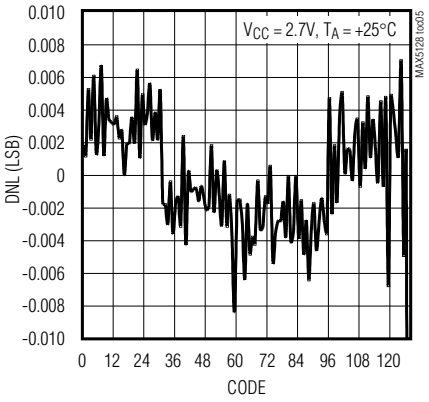
INTEGRAL NONLINEARITY vs. CODE (VOLTAGE-DIVIDER)



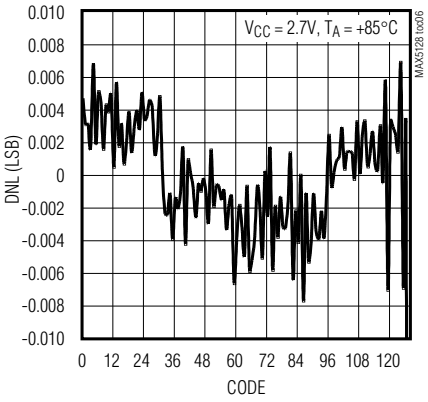
DIFFERENTIAL NONLINEARITY vs. CODE (VOLTAGE-DIVIDER)



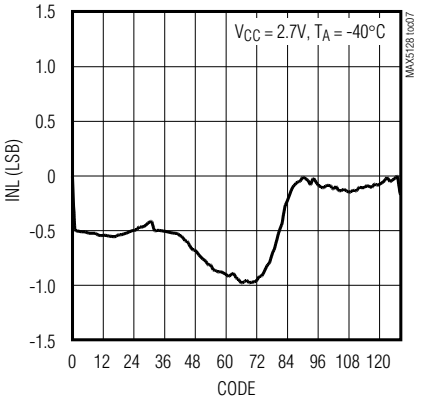
DIFFERENTIAL NONLINEARITY vs. CODE (VOLTAGE-DIVIDER)



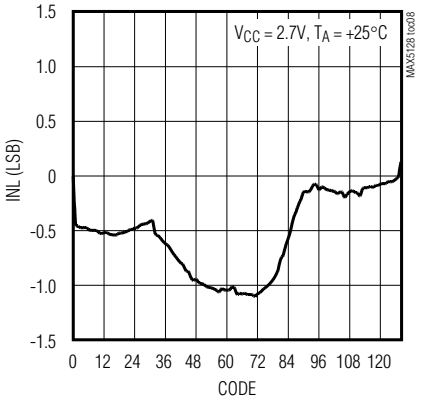
DIFFERENTIAL NONLINEARITY vs. CODE (VOLTAGE-DIVIDER)



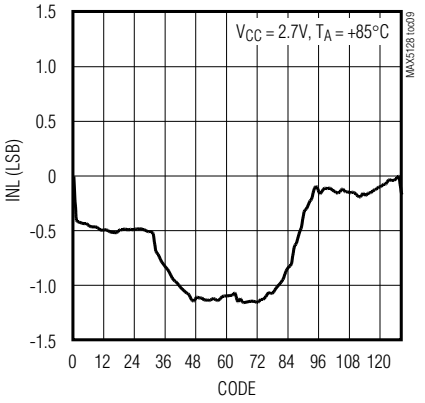
INTEGRAL NONLINEARITY vs. CODE (VARIABLE RESISTOR)



INTEGRAL NONLINEARITY vs. CODE (VARIABLE RESISTOR)



INTEGRAL NONLINEARITY vs. CODE (VARIABLE RESISTOR)

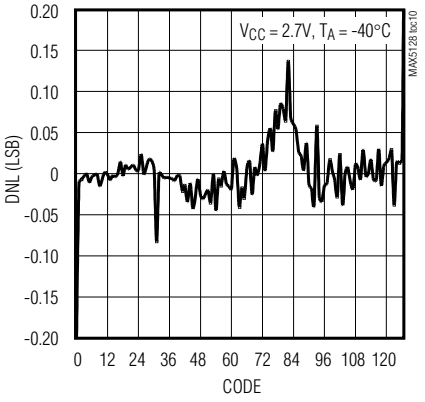


128-Tap, Nonvolatile, Linear-Taper Digital Potentiometer in 2mm x 2mm µDFN Package

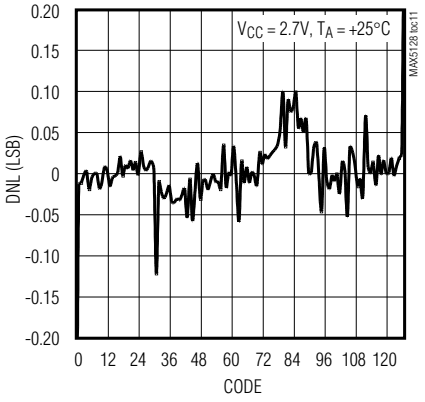
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

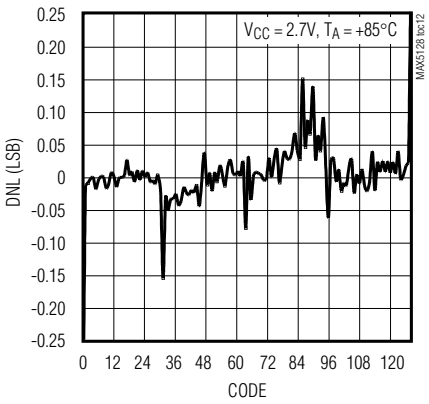
DIFFERENTIAL NONLINEARITY vs. CODE (VARIABLE RESISTOR)



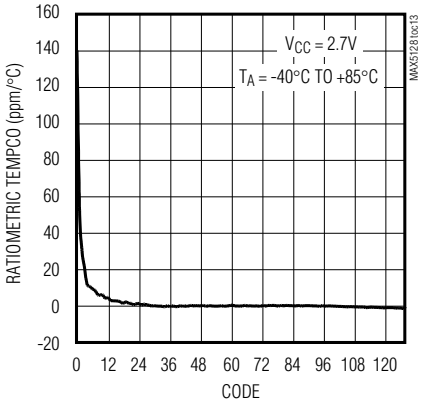
DIFFERENTIAL NONLINEARITY vs. CODE (VARIABLE RESISTOR)



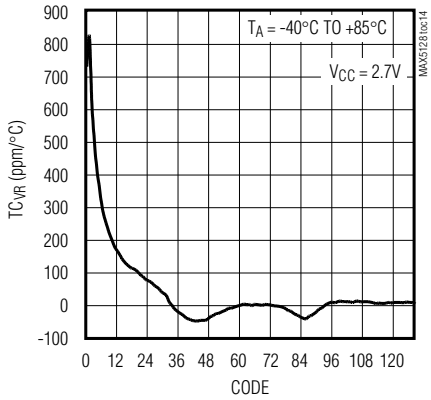
DIFFERENTIAL NONLINEARITY vs. CODE (VARIABLE RESISTOR)



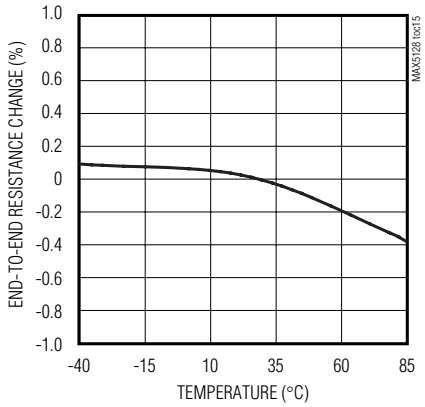
RATIOMETRIC TEMPERATURE COEFFICIENT vs. CODE (VOLTAGE-DIVIDER)



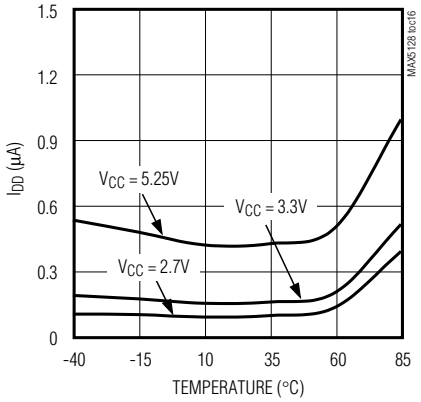
TEMPERATURE COEFFICIENT vs. CODE (VARIABLE RESISTOR)



END-TO-END RESISTANCE (R_{HL}) % CHANGE vs. TEMPERATURE



STANDBY SUPPLY CURRENT vs. TEMPERATURE

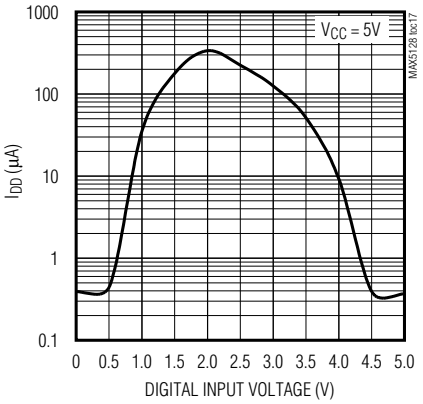


128-Tap, Nonvolatile, Linear-Taper Digital Potentiometer in 2mm x 2mm µDFN Package

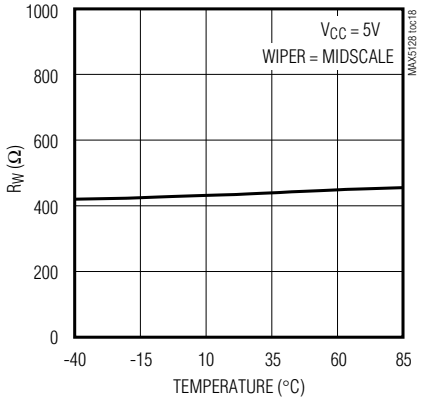
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

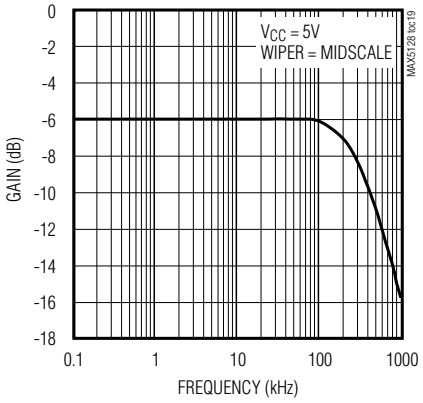
SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



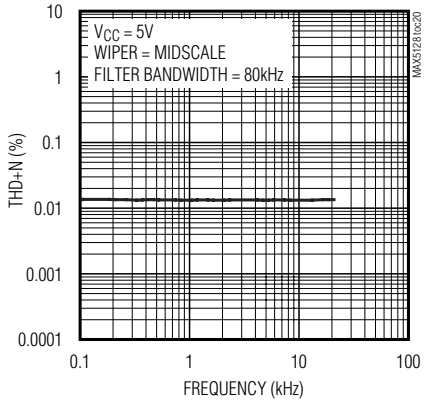
WIPER RESISTANCE vs. TEMPERATURE



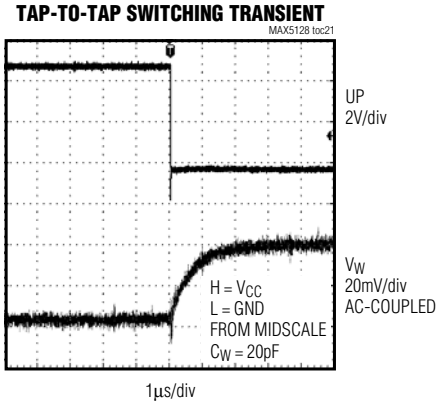
WIPER RESPONSE vs. FREQUENCY



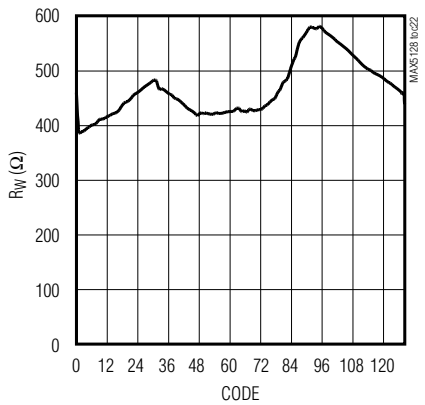
THD+N vs. FREQUENCY



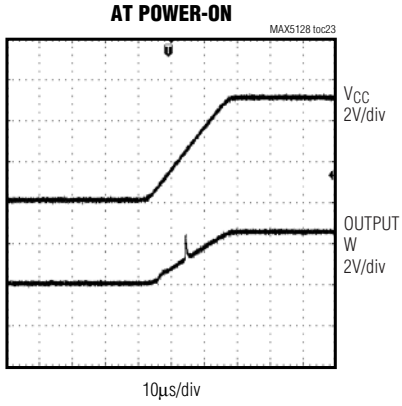
TAP-TO-TAP SWITCHING TRANSIENT



WIPER RESISTANCE vs. CODE



MIDSCALE WIPER TRANSIENT AT POWER-ON



128-Tap, Nonvolatile, Linear-Taper Digital Potentiometer in 2mm x 2mm µDFN Package

Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Power Supply. Bypass V_{CC} with a 0.1µF capacitor to GND as close to the device as possible. For proper operation, limit the supply voltage slew rate to ≥ 10µs.
2	H	High Terminal. The voltage at H can be higher than or lower than the voltage at L. Current can flow into or out of H.
3	W	Wiper Terminal
4	L	Low Terminal. The voltage at L can be higher than or lower than the voltage at H. Current can flow into or out of L.
5	GND	Ground
6	DN	Down Input
7	UP	Up Input
8	N.C.	No Connection. Not internally connected.

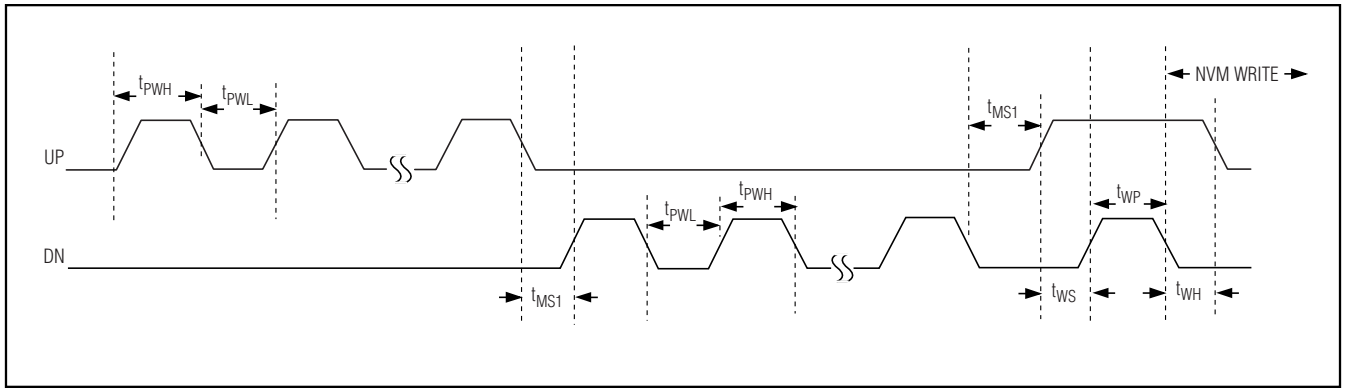


Figure 1. Digital-Interface Timing Diagram

Detailed Description

The MAX5128 nonvolatile, single, linear-taper, digital potentiometer performs the function of a mechanical potentiometer or variable resistor, but replaces the mechanics with a simple 2-wire digital interface. This device features 128 taps and 22kΩ end-to-end resistance with a 5ppm/°C ratiometric temperature coefficient. The MAX5128 operates from a +2.7V to +5.25V power supply and consumes only 0.5µA (typ) of standby supply current. The MAX5128 includes an integrated nonvolatile memory that recalls the stored wiper position of the digital potentiometer. A simple 2-wire up/down interface programs the wiper positions.

Analog Circuitry

The MAX5128 consists of a resistor array with 127 resistive elements; 128 tap points along the resistor string between H and L are accessible to the wiper, W. Select the wiper tap point by programming the potentiometer through the 2-wire (UP, DN) interface.

The MAX5128 features power-on reset circuitry that loads the wiper position from the nonvolatile memory at power-up.

The nonvolatile memory is programmed to midscale at the factory.

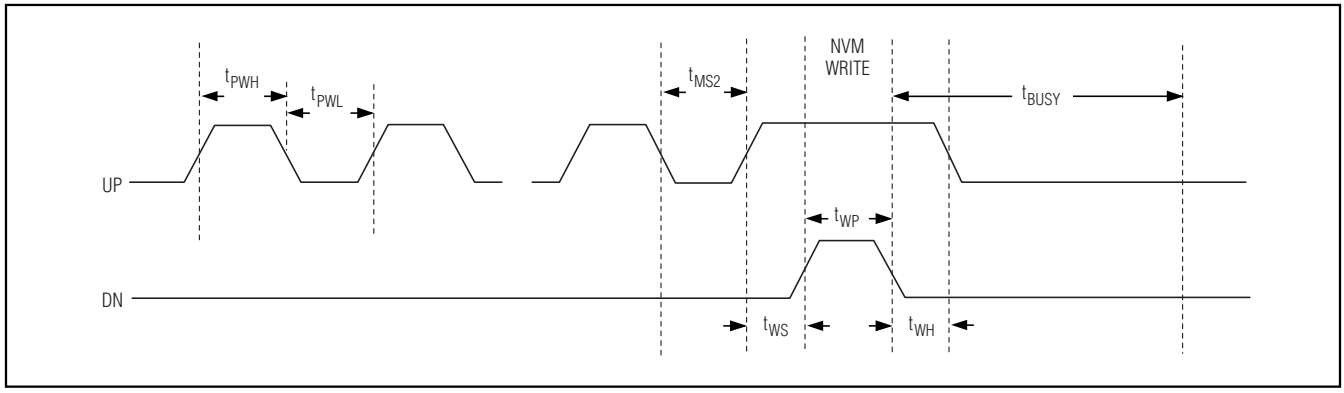


Figure 2. Digital-Interface Timing Diagram with t_{BUSY}

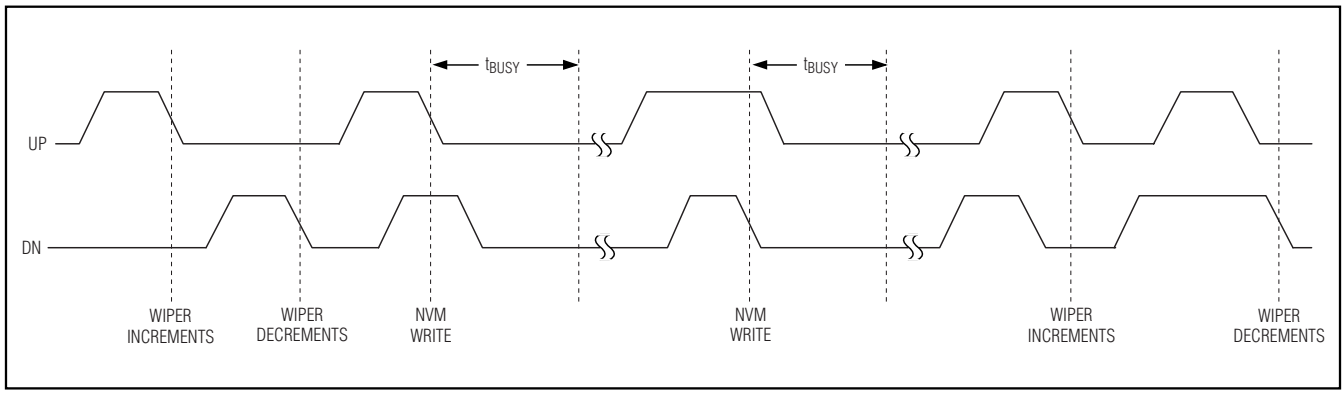


Figure 3. Digital-Interface Command Diagram

Digital Interface

The MAX5128 features a 2-wire interface consisting of two logic inputs (UP and DN). Logic inputs UP and DN control the wiper position and program the position to the nonvolatile memory. Transition UP from high to low with DN low to increment the wiper position. Transition DN from high to low with UP low to decrement the wiper position (see Figures 1, 2, and 3). When the wiper decrements, it decreases the resistance between W and L (and it increases the resistance between H and W).

To program the nonvolatile memory, force UP high, then force DN high, and then transition either input (UP/DN) from high to low (see Figure 3).

The wiper performs a make-before-break transition, ensuring that an open circuit during a transition from one resistor tap to another does not occur. The wiper does not wrap around when it reaches either end of the resistor array (max/min). Additional transition commands in the direction of the end point do not change the tap position.

The logic inputs also feature pulse glitch immunity (20ns) to protect the wiper from transitioning due to glitches (see Figure 4).

Write NV Register

The internal EEPROM consists of a 7-bit nonvolatile memory that retains the value written to it even after power-down. To program the nonvolatile memory, force UP high, then force DN high, and then transition either input (UP/DN) from high to low. A nonvolatile write requires a busy time of 14ms (max). During the busy time, any nonvolatile write requests are ignored as well as requests to increment or decrement the wiper position. Upon power-up, the wiper returns to the position stored in the nonvolatile register. The MAX5128 features a factory-default wiper position of midscale.

128-Tap, Nonvolatile, Linear-Taper Digital Potentiometer in 2mm x 2mm µDFN Package

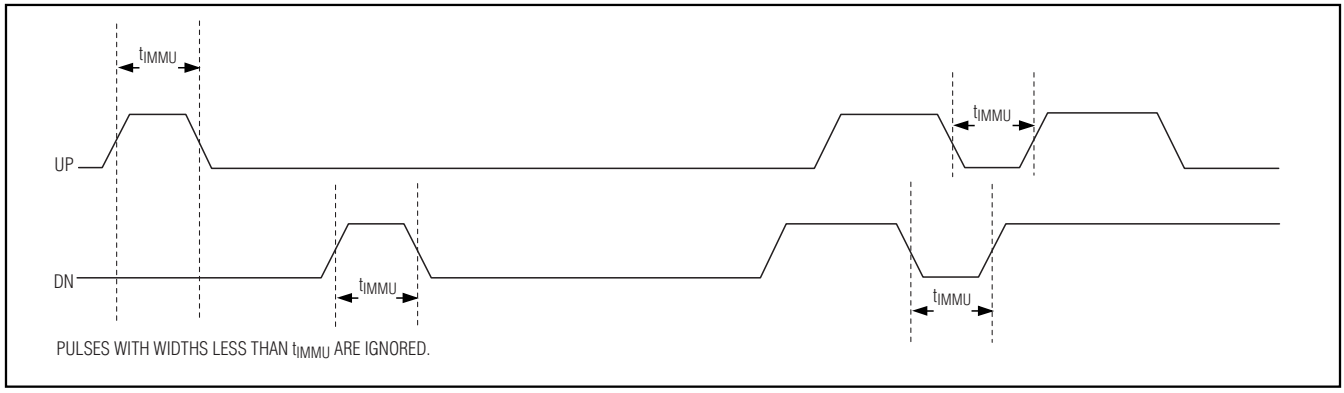


Figure 4. Glitch-Immunity Timing Diagram

Standby Mode

The MAX5128 operates in standby mode while the serial interface is inactive. Programming the MAX5128 increases the average operating current to 400µA (max). When in standby mode, the static supply current reduces to less than 0.5µA (typ).

Power-Up

Upon power-up, the MAX5128 updates the wiper position with the data stored in the nonvolatile memory. This initialization period takes 2µs (typ). For proper operation, limit the supply voltage slew rate to ≥ 10µs.

Applications Information

Use the MAX5128 for applications requiring digitally controlled adjustable resistance or voltage, such as LCD contrast control (where voltage biasing adjusts the display contrast), or DC-DC converters with adjustable outputs. The 22kΩ end-to-end resistance is divided into 128 tap points of 172Ω each. Use the MAX5128 in a voltage-divider or variable-resistor configuration.

V_{COM} Generator

Figure 5 shows an application using the MAX4238 and the MAX5128 to generate the V_{COM} voltage for a LCD panel. Adjusting the resistor value of the MAX5128 changes the V_{COM} voltage. Adjusting the V_{COM} voltage changes the contrast for the LCD panel.

DC-DC Converter Applications

Figures 6 and 7 show two applications using the MAX5128 to adjust the output voltage of a DC-DC converter. Figure 6 shows the MAX5128 in the grounded potentiometer configuration. Figure 7 shows the MAX5128 in a floating potentiometer configuration. The grounded potentiometer configuration forces the output voltage range of the DC-DC converter to fall within the supply voltage range of the MAX5128. Use the floating potentiometer configuration to allow the DC-DC converter's output to exceed the supply voltage range of the MAX5128. The floating potentiometer configuration increases the output voltage range and increases the precision of the output voltage adjustment range.

LED Bias Adjustment

Figure 8 shows a LED bias adjustment application using a MAX5128 to set the current of the LEDs that the MAX1574 drives. Use the MAX5128 for an adjustable LED current drive of 10mA to 60mA.

Chip Information

PROCESS: BiCMOS

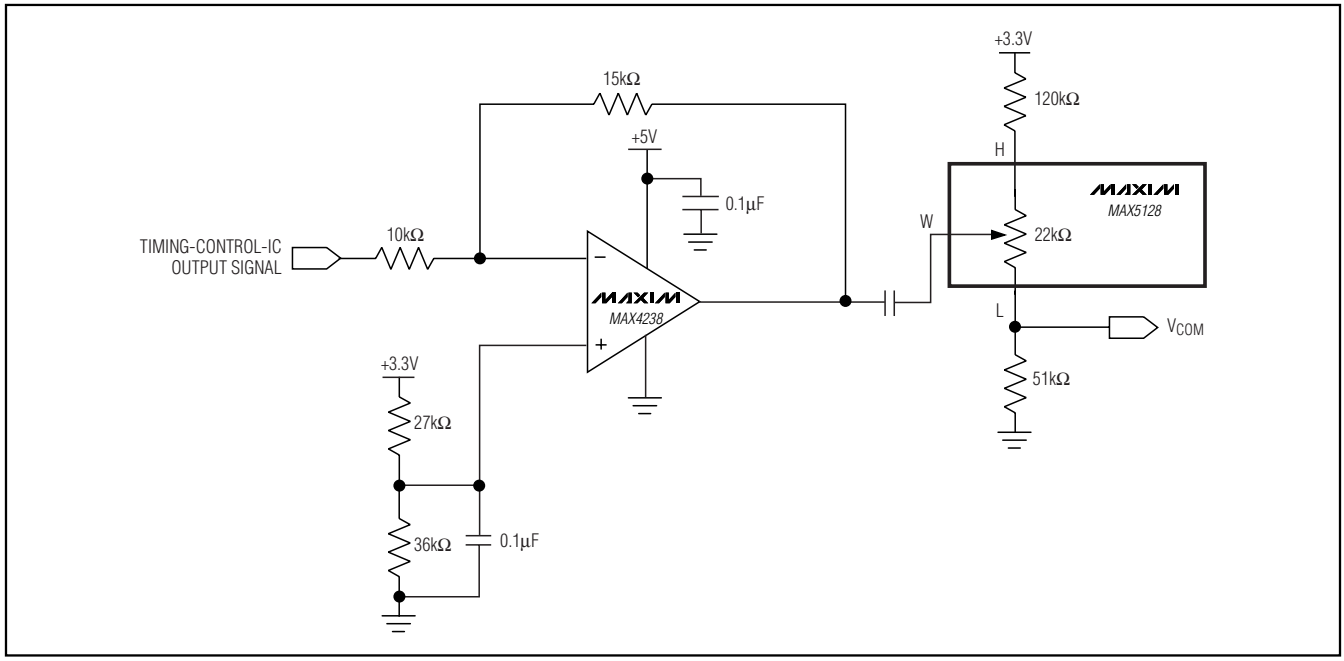


Figure 5. V_{COM} Generator Circuit for LCD Panels

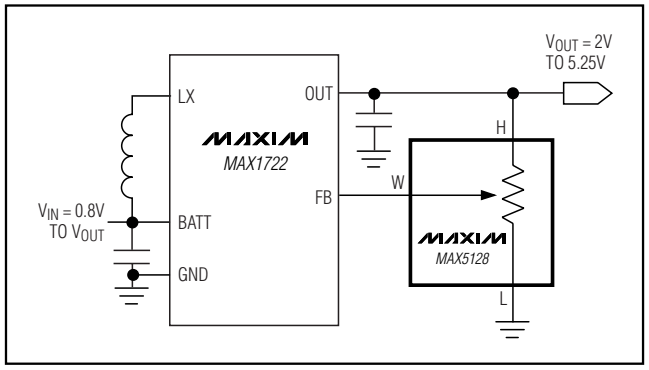


Figure 6. DC-DC Converter Using a Grounded Potentiometer

128-Tap, Nonvolatile, Linear-Taper Digital Potentiometer in 2mm x 2mm µDFN Package

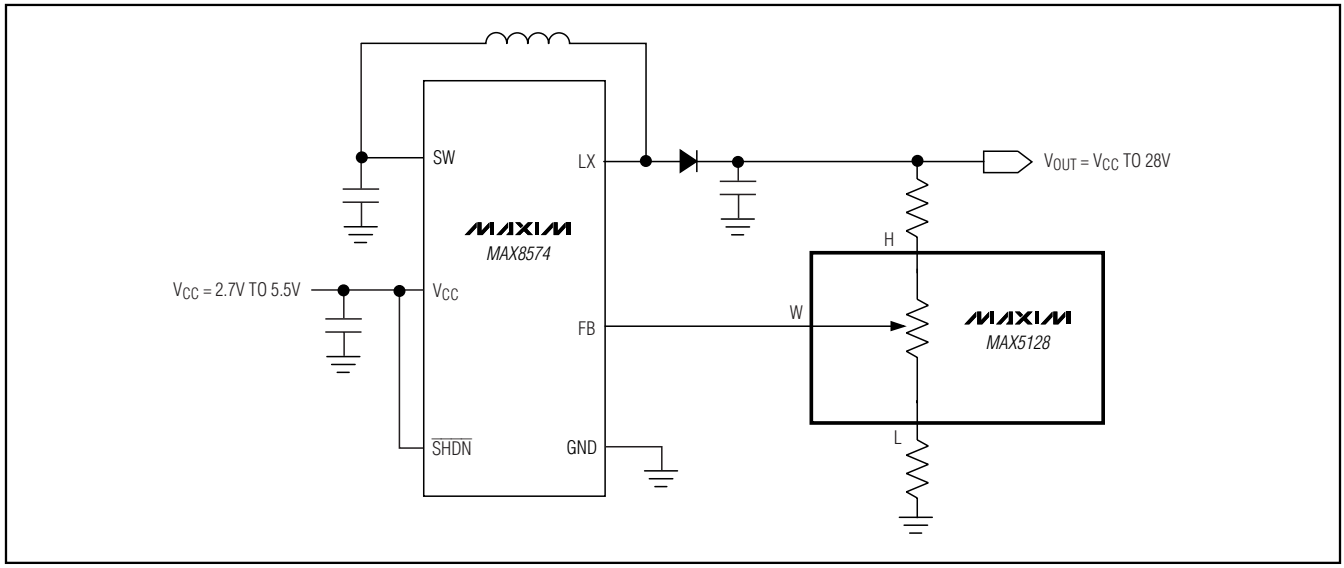


Figure 7. DC-DC Converter Using a Floating Potentiometer

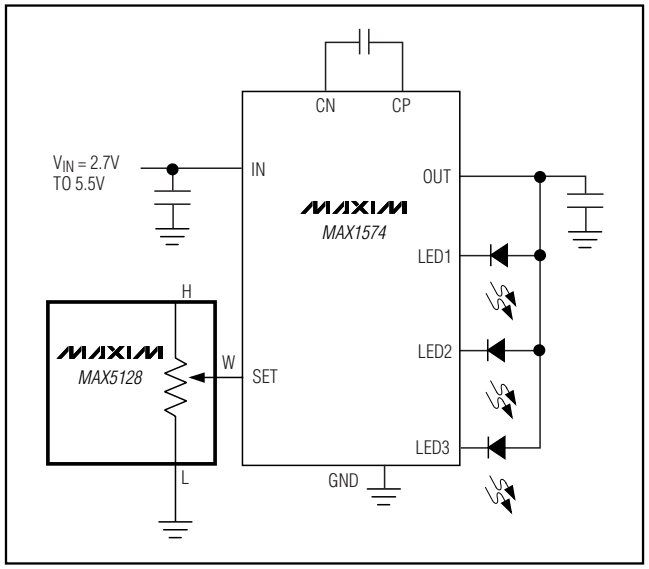
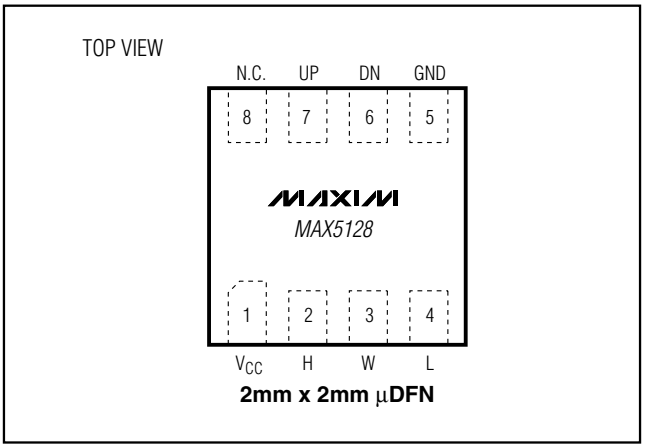


Figure 8. LED Bias Adjustment Using the MAX5128

Pin Configuration

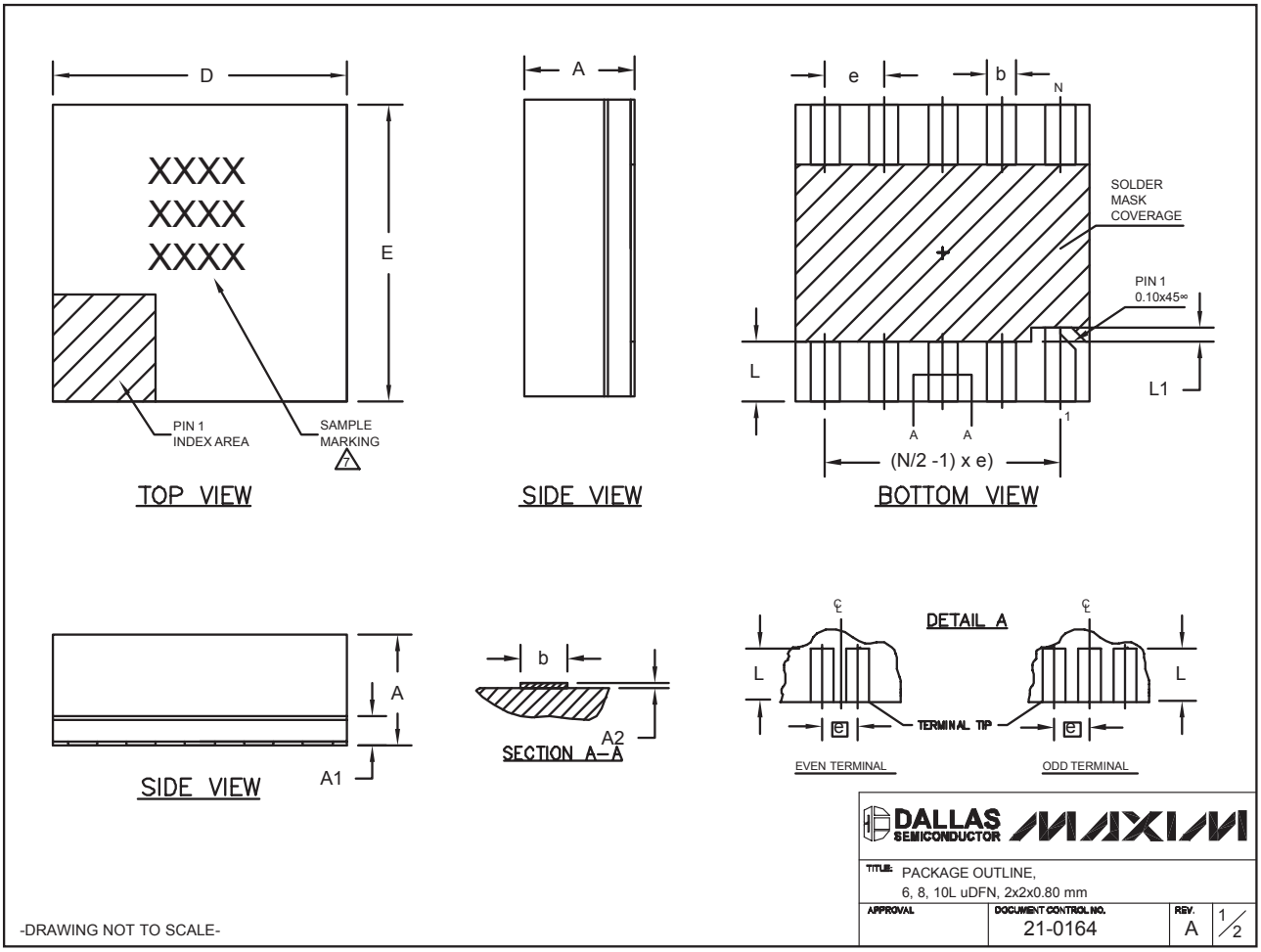


128-Tap, Nonvolatile, Linear-Taper Digital Potentiometer in 2mm x 2mm µDFN Package

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6, 8, 10L UDFN.EPS



128-Tap, Nonvolatile, Linear-Taper Digital Potentiometer in 2mm x 2mm µDFN Package

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.15	0.20	0.25
A2	0.020	0.025	0.035
D	1.95	2.00	2.05
E	1.95	2.00	2.05
L	0.30	0.40	0.50
L1	0.10 REF.		

PACKAGE VARIATIONS				
PKG. CODE	N	e	b	(N/2 -1) x e
L622-1	6	0.65 BSC	0.30±0.05	1.30 REF.
L822-1	8	0.50 BSC	0.25±0.05	1.50 REF.
L1022-1	10	0.40 BSC	0.20±0.03	1.60 REF.

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. "N" IS THE TOTAL NUMBER OF LEADS.
6. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6, 8, 10L uDFN, 2x2x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0164	A	2/2

Revision History

Pages changed at Rev 1: 1, 9, 10, 13

Pages changed at Rev 2: 1, 9–14