Absolute Maximum Ratings

(All voltages referenced to GND.)
IN (Note 1).....-0.3V to +29V
OUT.....-0.3V to +26V
IN - OUT.....-26V to +29V
OTG_EN, ACOK, $\overline{ACOK}$.....-0.3V to +6V
OVLO.....-0.3V to +26V
Continuous Current into IN, OUT
WLP (Note 2).....±4.5A
TDFN.....±3.2A

Continuous Power Dissipation (T_A = +70°C)
WLP (derate 16.4mW/°C above +70°C).....1312mW
TDFN (derate 24.4mW/°C above +70°C).....1951mW
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

Note 1: Survives burst pulses up to 100V with 2Ω series resistance and hot plug events. Above the input clamp voltage, the IN must be a surge in nature with a limited energy.
Note 2: Limited by the PCB thermal design.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 3)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....52°C/W

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....41°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....9°C/W

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = +3V to +28V, V_{OUT} = +3V to +24V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = +5V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Startup Voltage	V_{INBT}			2.17	3	V
Input Sustaining Voltage	V_{INBU}	I_{OUT} = 0A		1.5	2.3	V
Input Clamp Voltage	V_{IN_CLAMP}	I_{IN} = 10mA, T_A = +25°C		33.7		V
Input Supply Current	I_{IN}	V_{OVLO} = 0V, V_{IN} = 5V, ACOK is unconnected, I_{OUT} = 0mA		100	190	µA
Output Startup Voltage	V_{OUTBT}			2.15	3	V
Output Sustaining Voltage	V_{OUTBU}	I_{IN} = 0A		1.5	2.3	V
Output Supply Current	I_{OUT}	V_{OVLO} = 0V, V_{OUT} = 5V, I_{IN} = 0mA, V_{OTG_EN} = 1.8V		83	170	µA
Output Shutdown Current		V_{OVLO} = 3V, V_{OUT} = 5V, V_{IN} = 0V, V_{OTG_EN} = 0V		6	12	µA
IN Leakage Voltage		V_{OUT} = 21V, IN unconnected, V_{OTG_EN} = 0V		0.001	0.1	V
IN Discharge Current		V_{IN} = V_{OUT} = 5V, IN discharge current after an OTG_EN transition from high to low		100	150	mA

Electrical Characteristics (continued)

(V_{IN} = +3V to +28V, V_{OUT} = +3V to +24V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = +5V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OVP (IN TO OUT)							
On-Resistance (IN to OUT)	R_{ON}	V_{IN} = 5V, I_{OUT} = 100mA	WLP, T_A = +25°C		65	87	mΩ
			TDFN, T_A = +25°C		85	110	
Internal Overvoltage Trip Level	V_{IN_OVLO}	MAX14670	V_{IN} rising	6.6	6.8	7.0	V
			V_{IN} falling	6.5			
		MAX14671	V_{IN} rising	15.0	15.5	16.0	
			V_{IN} falling	14.5			
		MAX14672	V_{IN} rising	5.65	5.825	6.0	
			V_{IN} falling	5.55			
OVLO Set Threshold	V_{OVLO_TH}			1.18	1.221	1.26	V
Adjustable OVLO Threshold Range	V_{OVLO_EXT}			5		22	V
External OVLO Select Threshold	V_{OVLO_SEL}			0.2	0.25	0.3	V
DIGITAL SIGNALS (ACOK, $\overline{ACOK}$, OTG_EN)							
ACOK Output High Voltage	V_{ACOK}	I_{SOURCE} ≤ 100µA, V_{IN} > 3V		1.6	1.8	2.0	V
ACOK Leakage Current		Pull down to ground, V_{OUT} = 5V, OTG_EN = high, ACOK deasserted				1	µA
$\overline{ACOK}$ Output Low Voltage	V_{OL}	V_{IO} = 3.3V, I_{SINK} = 1mA				0.4	V
$\overline{ACOK}$ Leakage Current		V_{IO} = 3.3V, $\overline{ACOK}$ deasserted				1	µA
OTG_EN Input Logic-High	V_{IH}			1.6			V
OTG_EN Input Logic-Low	V_{IL}					0.4	V
OTG_EN Input Leakage Current	I_{IN}	0V ≤ V_{IN} ≤ V_{IL} and V_{IH} ≤ V_{IN} ≤ V_{CC}, V_{CC} = 5.5V		-1		+1	µA
TIMING CHARACTERISTICS (Figure 1)							
IN Debounce Time	t_{DEB}	V_{IN} = 5V to charge pump on (V_{OUT} = 10% of V_{IN}), R_{LOAD} = 100Ω, C_{LOAD} = 10µF			20		ms
IN/OUT Soft-Start Time	t_{SS}	V_{IN} = 5V to V_{OUT} = 90% of V_{IN}, R_{LOAD} = 100Ω, C_{LOAD} = 10µF			25		ms
IN OVP Turn-On Time During Soft-Start	t_{ON}	V_{IN} = 5V, R_{LOAD} = 100Ω, C_{LOAD} = 10µF, V_{OUT} = 20% of V_{IN} to 80% of V_{IN}			1.5		ms
IN OVP Turn-Off Response Time	t_{OFF}	From V_{IN} > V_{OVLO} to V_{OUT} = 80% of V_{IN}, R_{LOAD} = 100Ω			1		µs
OTG Turn-On Time	t_{OTG_ON}	Time from OTG_EN high to V_{IN} = 80% of V_{OUT}, V_{OUT} = 5V, C_{IN} = 10µF			1.4		ms
In-Discharge Pulse Duration		V_{IN} = V_{OUT} = 5V, current pulse duration after an OTG_EN transition from high to low			1.1		ms

Electrical Characteristics (continued)

(V_{IN} = +3V to +28V, V_{OUT} = +3V to +24V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{IN} = +5V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			150		°C
Thermal Hysteresis	T_{HYST}			20		°C
ESD PROTECTION						
Human Body Model		IN pin		±15		kV
IEC 61000-4-2 Contact Discharge		IN pin		±8		kV
IEC 61000-4-2 Air-Gap Discharge		IN pin		±8		kV

Note 4: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Figure 1

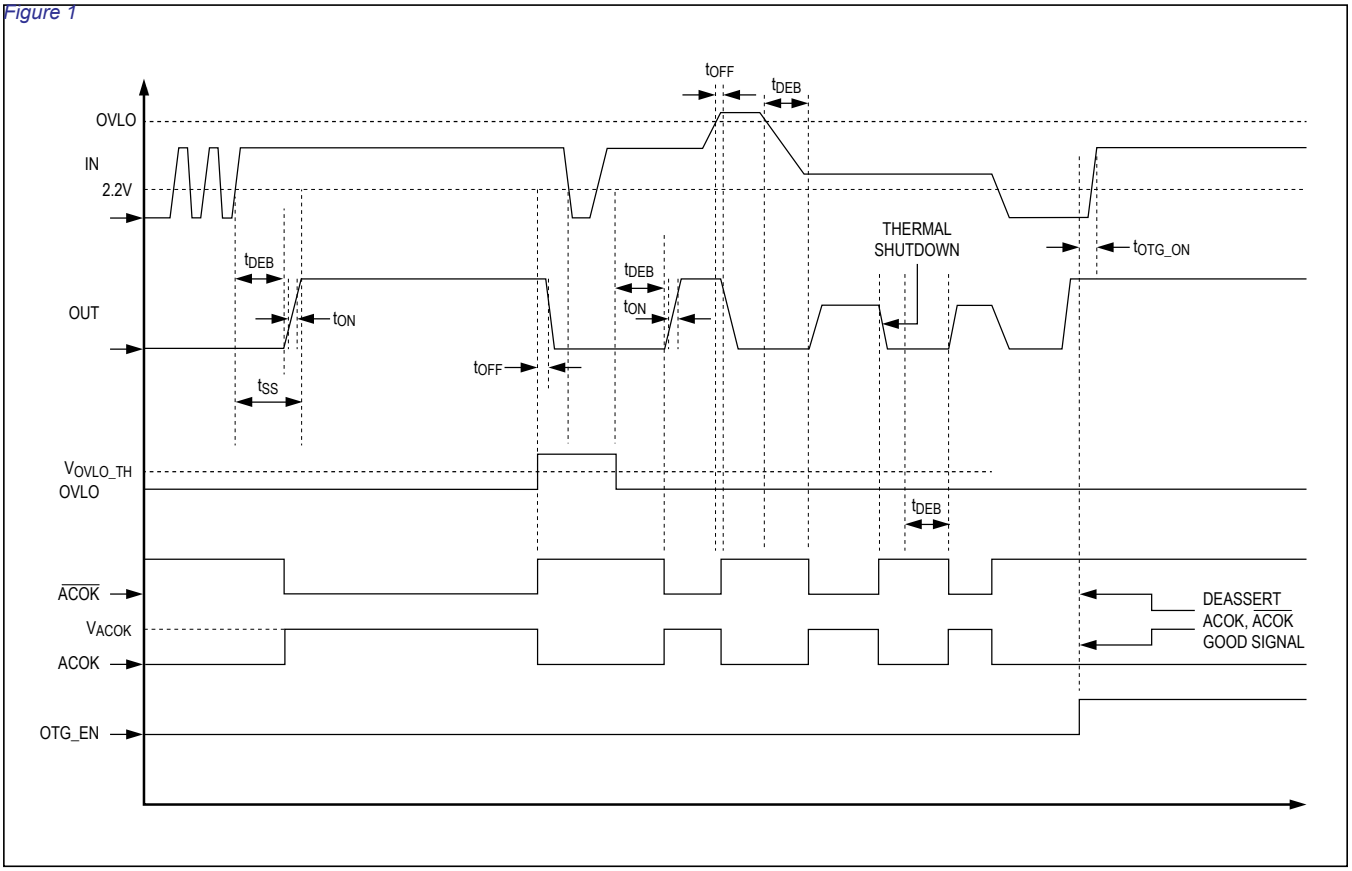
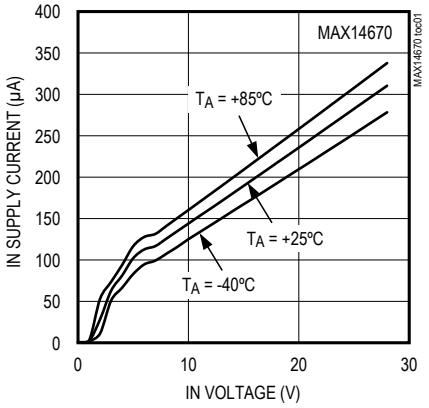


Figure 1. Timing Diagram

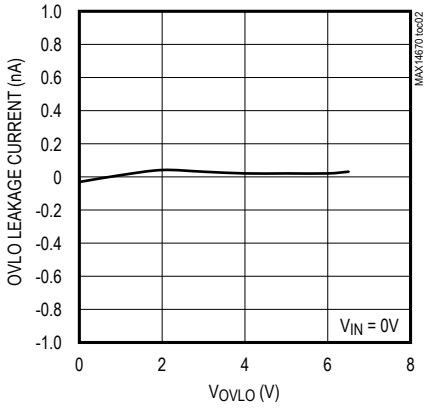
Typical Operating Characteristics

(V_{IN} = +5V, OVLO = GND, C_{IN} = 0.1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

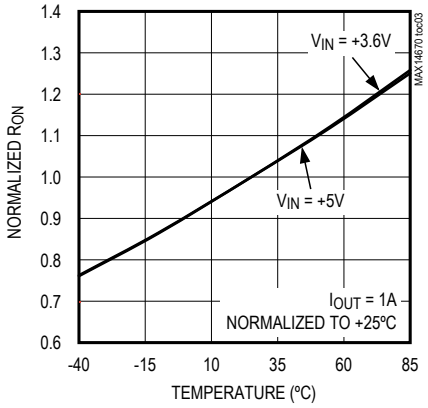
IN SUPPLY CURRENT vs. IN VOLTAGE



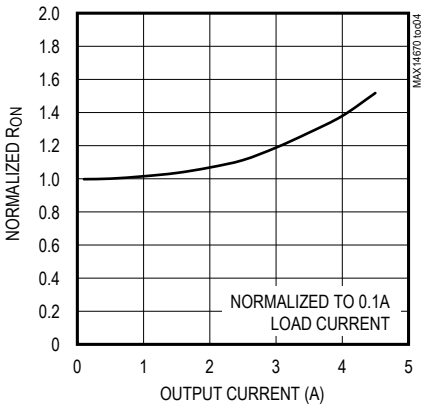
OVLO LEAKAGE CURRENT vs. OVLO VOLTAGE



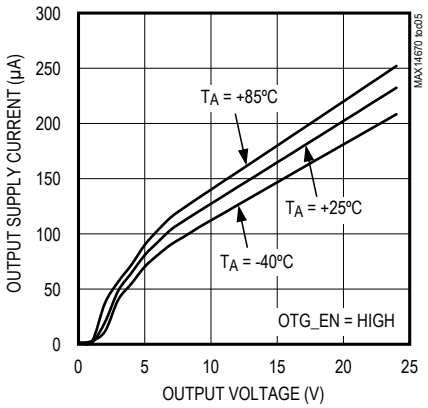
NORMALIZED ON-RESISTANCE vs. TEMPERATURE



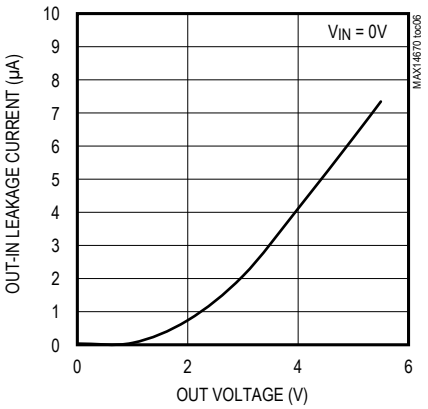
NORMALIZED ON-RESISTANCE vs. OUTPUT CURRENT



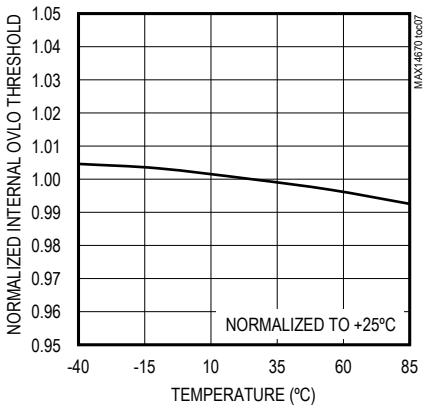
OUTPUT SUPPLY CURRENT vs. OUTPUT VOLTAGE



OUT-IN LEAKAGE CURRENT vs. OUT VOLTAGE



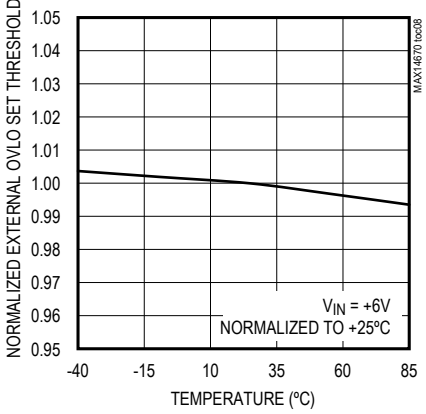
NORMALIZED INTERNAL OVLO THRESHOLD vs. TEMPERATURE



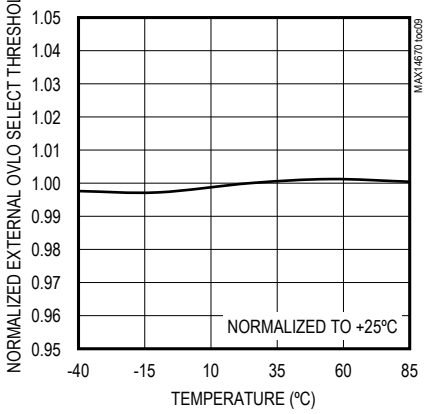
Typical Operating Characteristicsc (continued)

(V_{IN} = +5V, OVLO = GND, C_{IN} = 0.1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

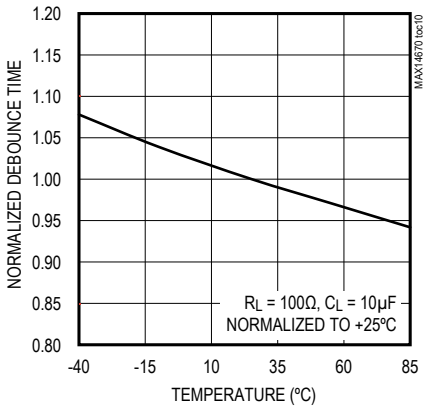
NORMALIZED EXTERNAL OVLO SET THRESHOLD vs. TEMPERATURE



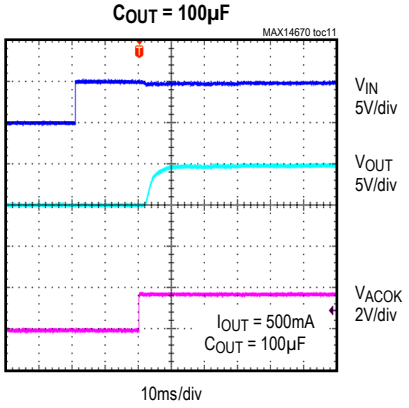
NORMALIZED EXTERNAL OVLO SELECT THRESHOLD vs. TEMPERATURE



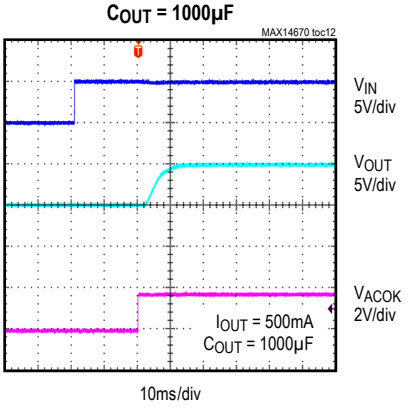
NORMALIZED DEBOUNCE TIME vs. TEMPERATURE



POWER-UP RESPONSE, C_{OUT} = 100µF



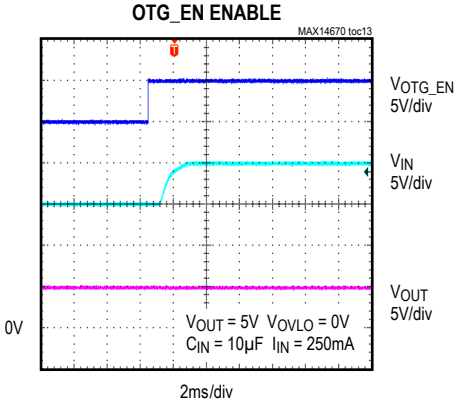
POWER-UP RESPONSE, C_{OUT} = 1000µF



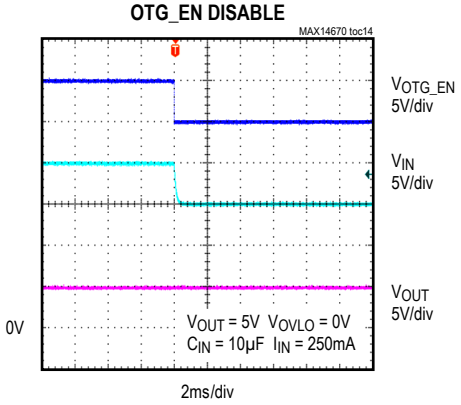
Typical Operating Characteristicsc (continued)

(V_{IN} = +5V, OVLO = GND, C_{IN} = 0.1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

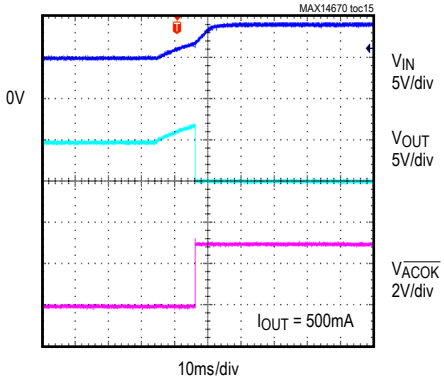
OTG_EN ENABLE



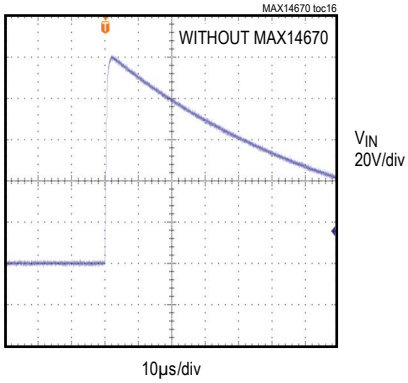
OTG_EN DISABLE



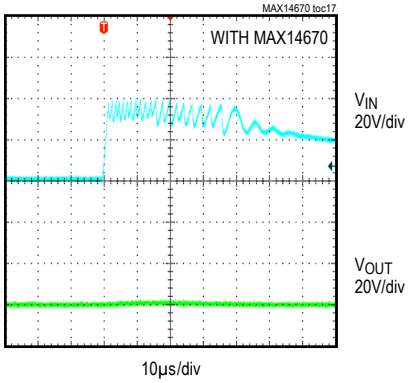
OVERVOLTAGE FAULT RESPONSE



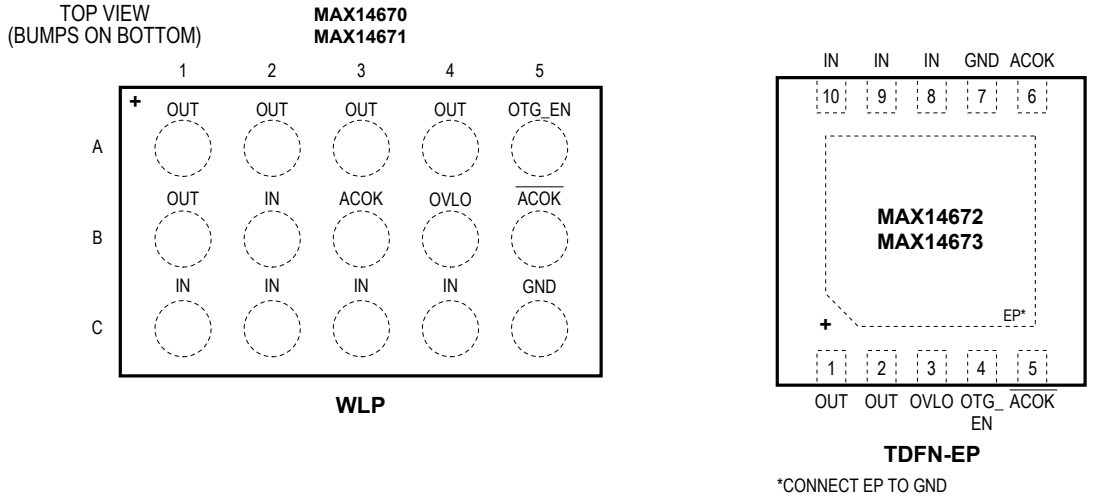
100V SURGE TEST WAVEFORM



100V SURGE TEST WAVEFORM



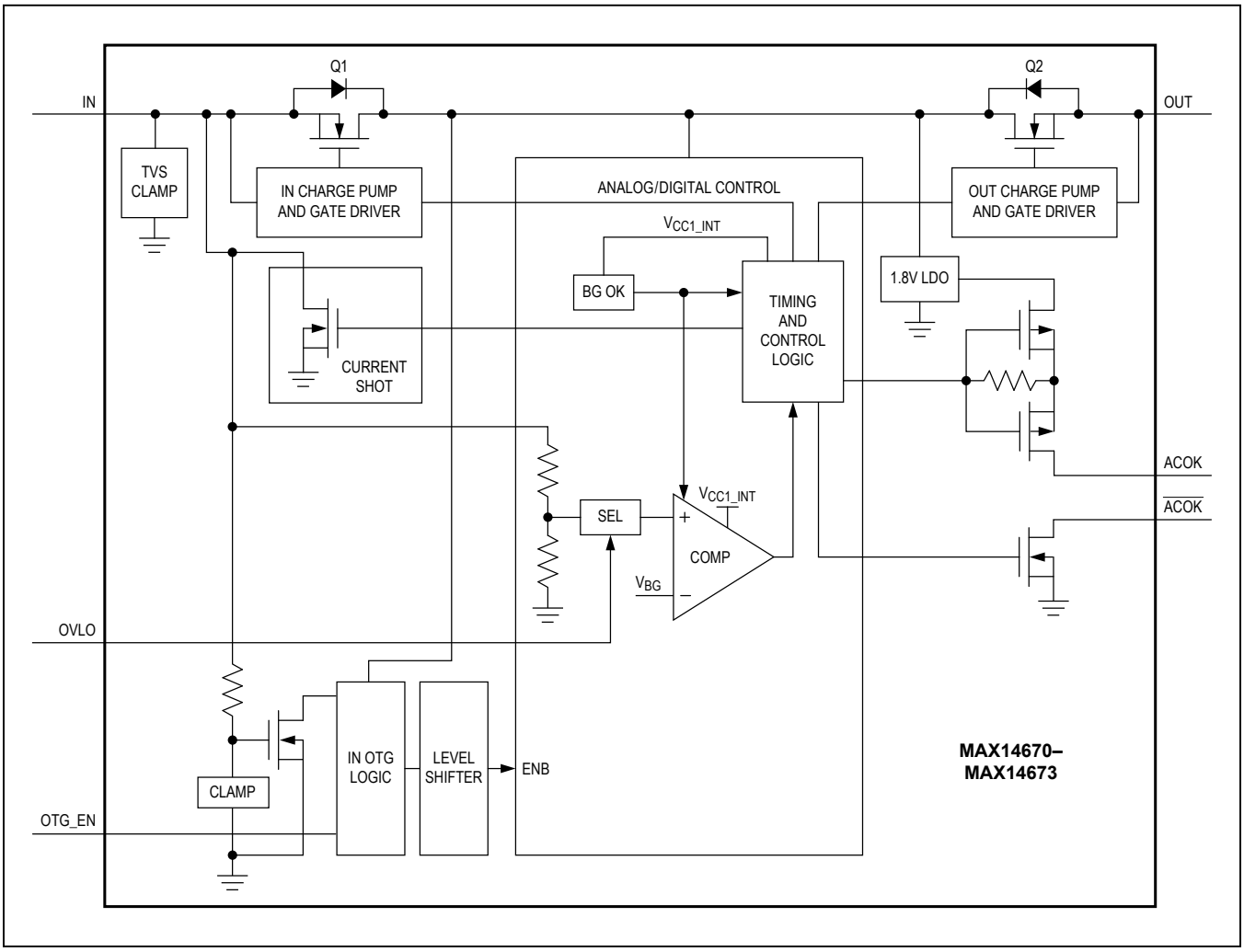
Pin Configurations



Pin Descriptions

BUMP	PIN	NAME	FUNCTION
MAX14670/ MAX14671	MAX14672/ MAX14673		
A1–A4, B1	1, 2	OUT	Overvoltage Protection Output. Bypass OUT with a 1µF ceramic capacitor. Externally connect all OUT together.
A5	4	OTG_EN	Enable Input for OTG Supply Operation
B2, C1–C4	8–10	IN	Overvoltage Protection Input. If desired, bypass IN with a 0.1µF ceramic capacitor as close to the device as possible. Externally connect all IN together.
B3	6	ACOK	1.8V Logic Output. ACOK is driven high after input voltage is stable between minimum V_{IN} and V_{OVLO} when OTG_EN = 0. Connect a pulldown resistor from ACOK to ground.
B4	3	OVLO	Overvoltage Lockout Input. Connect OVLO to GND to use internal OVLO threshold. Connect OVLO to a resistor-divider for a different voltage threshold.
B5	5	$\overline{ACOK}$	Open-Drain Flag Output. $\overline{ACOK}$ is driven low after input voltage is stable between minimum V_{IN} and V_{OVLO} when OTG_EN = 0. Connect a pullup resistor from $\overline{ACOK}$ to the logic I/O voltage of the host system.
C5	7	GND	Ground
—	—	EP	Exposed Pad (TDFN Only). Connect EP to ground.

Functional Diagram



Detailed Description

The MAX14670–MAX14673 overvoltage protection (OVP) devices feature low on-resistance (R_{ON}) internal FETs (Q1+Q2) and protect low-voltage systems against voltage faults up to +28V_{DC}. An internal clamp also protects the devices from surges up to +100V. If the input voltage exceeds the overvoltage threshold, the output is disconnected from the input to prevent damage to the protected components. The 15ms debounce time prevents false turn-on of the internal FETs during startup.

Soft-Start

To minimize inrush current, the devices feature a soft-start capability to slowly turn on Q1 and Q2. Soft-start begins when $\overline{ACOK}$/ACOK is asserted and ends after 15ms (typ).

Overvoltage Lockout (OVLO)

Connect OVLO to ground to use the internal OVLO comparator with the internally set OVLO value. When IN goes above the overvoltage lockout threshold (V_{IN_OVLO}), OUT is disconnected from IN and $\overline{ACOK}$/ACOK is deasserted. When IN drops below V_{IN_OVLO}, the debounce time starts counting. After the debounce time, OUT follows IN again and $\overline{ACOK}$/ACOK is asserted.

External OVLO Adjustment Functionality

When an external resistor-divider is connected to OVLO and V_{OVLO} exceeds the OVLO select voltage (V_{OVLO_SEL}), the internal OVLO comparator reads IN by the external resistor-divider.

R1 = 1MΩ is a good starting value for minimum current consumption. Since V_{IN_OVLO}, V_{OVLO_TH}, and R1 are known, R2 can be calculated from the following formula:

$$V_{IN\_OVLO} = V_{OVLO\_TH} \times \left[1 + \frac{R1}{R2}\right]$$

This external resistor-divider is completely independent from the internal resistor-divider.

Reverse Bias Blocking

The ICs feature reverse bias blocking. When IN voltage is below input startup voltage and OTG_EN is low, the switch between IN and OUT is open and the two back-to-back diodes of the two series switches block reverse bias. Therefore, when the voltage is applied at the output, current does not travel back to the input. When OVLO is high, the parts block against reverse bias as well.

OTG Enable

The devices feature reverse turn-on capability. OTG_EN can be used to turn on the switch for OUT to feed back to IN when the voltage applied at OUT is above the minimum startup voltage. When OTG_EN is high, ACOK and $\overline{ACOK}$ are deasserted. During the OTG operation, if IN goes above OVLO, the OVP switch turns off. It is recommended that the power is supplied to OUT prior to OTG operation and also the power is removed from OUT prior to disable OTG operation.

Thermal Shutdown Protection

The devices feature thermal shutdown protection to protect the devices from overheating. The internal FETs turn off when the junction temperature exceeds +150°C (typ), and the device returns to normal operation after the temperature drops by approximately 20°C (typ).

Applications Information

IN Bypass Capacitor

If desired, bypass IN to GND with a 0.1µF ceramic capacitor as close to the device as possible. If the power source has significant inductance due to long lead length, the device prevents overshoots due to the LC tank circuit and provides protection by clamping the overshooting.

Output Capacitor

The slow turn-on time provides a soft-start function that allows the devices to charge an output capacitor up to 1000µF without turning off due to an overcurrent condition. Bypass OUT to GND with a minimum of 1µF ceramic capacitor.

Extended ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (Human Body Model) encountered during handling and assembly. IN is further protected against ESD up to ±15kV (HBM), ±15kV (Air-Gap Discharge method described in IEC 61000-4-2) and ±8kV (Contact Discharge Method described in IEC 61000-4-2) without damage.

The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX14670–MAX14673 continue to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model ESD Protection

Figure 2 shows the HBM and Figure 3 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 4 shows the IEC 61000-4-2 model, and Figure 5 shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

Figure 2

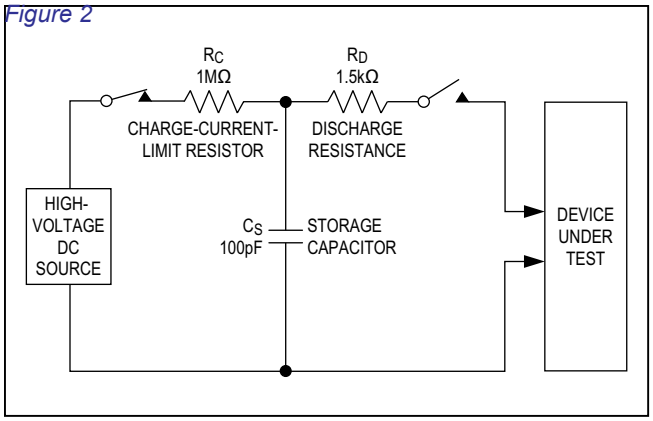


Figure 2. Human Body ESD Test Model

Figure 4

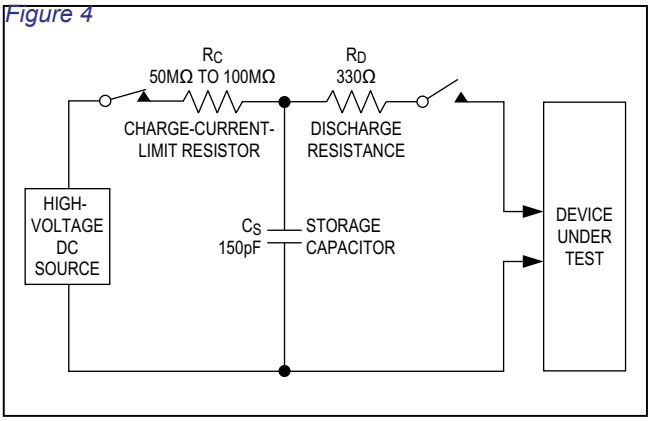


Figure 4. IEC 61000-4-2 ESD Test Model

Figure 3

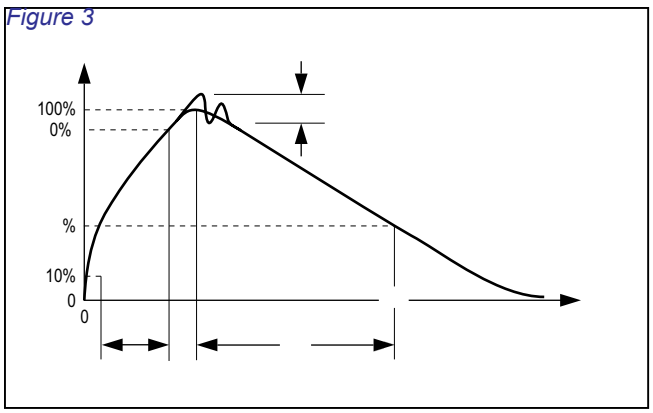


Figure 3. Human Body Current Waveform

Figure 5

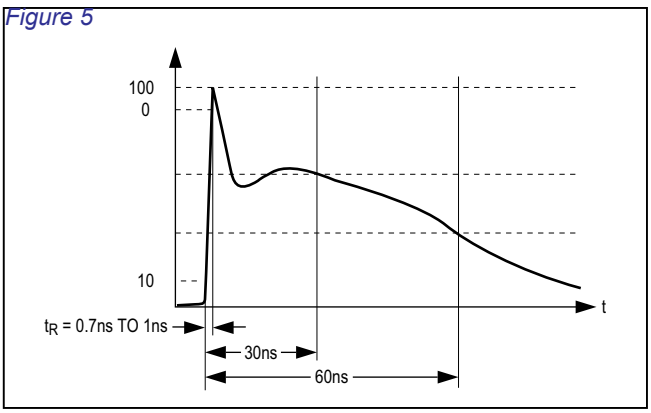
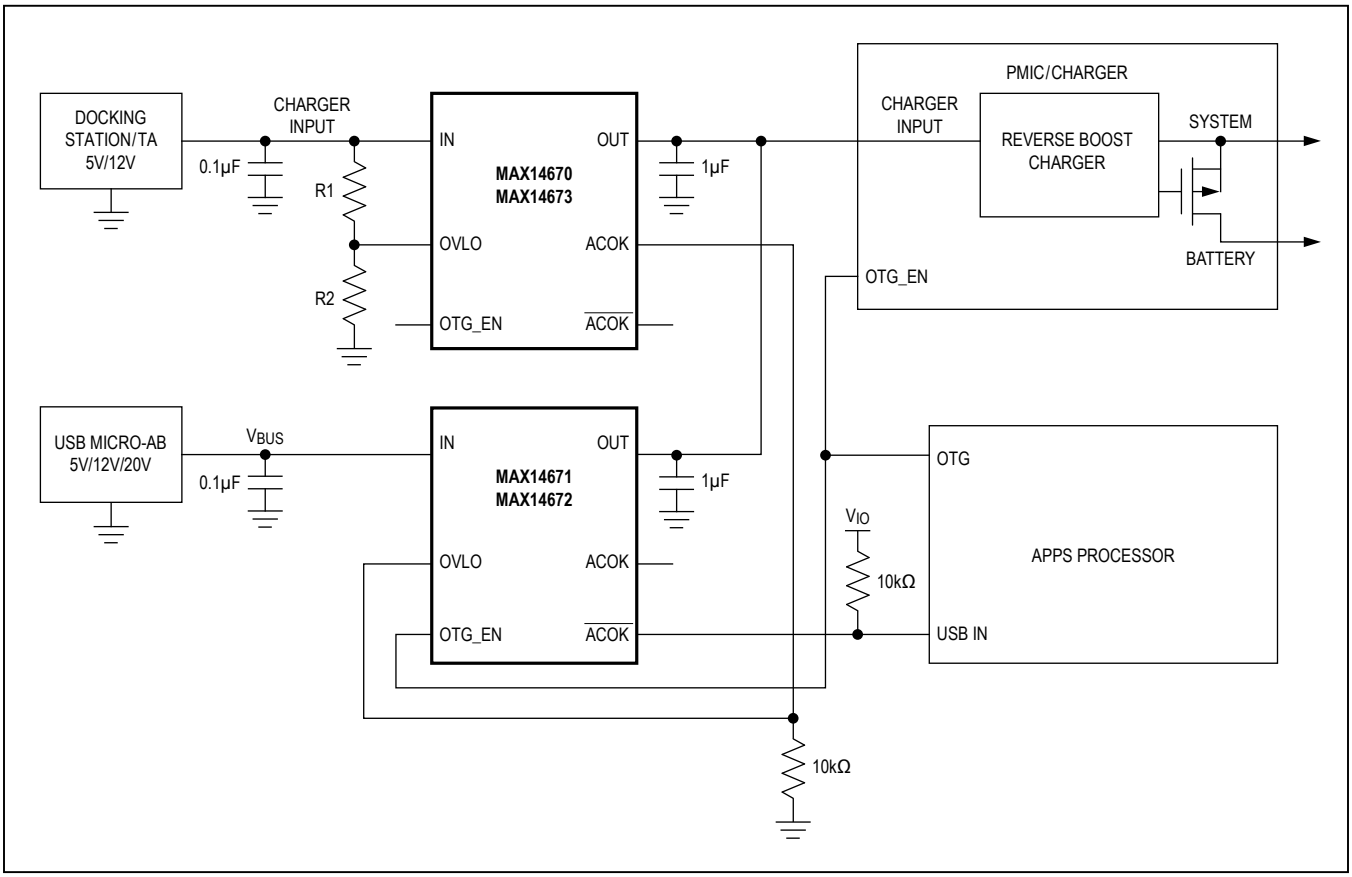


Figure 5. IEC 61000-4-2 ESD Generator Current Waveform

Typical Operating Circuit



Ordering Information/Selector Guide

PART	OVLO (V)	TOP MARK	PIN-PACK-AGE
MAX14670EWL+T	6.8	+14670EWL	15 WLP
MAX14671EWL+T	15.5	+14671EWL	15 WLP
MAX14672ETB+T	5.825	AZF	10 TDFN-EP*
MAX14673ETB+T**	22	AZG	10 TDFN-EP*

Note: *All devices are specified over -40°C to +85°C operating temperature range.*

+Denotes a lead(Pb)-free package/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

***Future product—contact factory for availability.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 TDFN	T1033+1	21-0137	90-0003
15 WLP	W151C2+1	21-0686	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/13	Initial release	—
1	7/13	Update *Functional Diagram*	9
2	8/13	Included soldering lead time; corrected nFET and pFET arrows in *Functional Diagram*	2, 9
3	10/13	Updated *Functional Diagram*	9
4	1/14	Updated data sheet to reflect 100V surge protection capability	1, 2, 7, 10
5	9/16	Updated *Pin Descriptions* table	8

