Product Line	Ordering Part Number	Product Status	Reference PCN
M4-64/32	M4-64/32-7JC	Converted to M4A5	Contact pcn@latticesemi.com for more info.
	M4-64/32-10JC		
	M4-64/32-12JC		
	M4-64/32-15JC		
	M4-64/32-10JI		
	M4-64/32-12JI		
	M4-64/32-14JI		
	M4-64/32-18JI		
	M4-64/32-7VC		
	M4-64/32-10VC		
	M4-64/32-12VC		
	M4-64/32-15VC		
	M4-64/32-10VI		
	M4-64/32-12VI		
	M4-64/32-14VI		
	M4-64/32-18VI		
	M4-64/32-7VC48		
	M4-64/32-10VC48		
	M4-64/32-12VC48		
	M4-64/32-15VC48		
	M4-64/32-10VI48		
	M4-64/32-12VI48		
	M4-64/32-14VI48		
	M4-64/32-18VI48		
M4-96/48	M4-96/48-7VC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-96/48-10VC		
	M4-96/48-12VC		
	M4-96/48-15VC		
	M4-96/48-10VI		
	M4-96/48-12VI		
	M4-96/48-14VI		
	M4-96/48-18VI		
M4-128/64	M4-128/64-7YC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-128/64-10YC		
	M4-128/64-12YC		
	M4-128/64-15YC		
	M4-128/64-10YI		
	M4-128/64-12YI		
	M4-128/64-14YI		
	M4-128/64-18YI		

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Product Line	Ordering Part Number	Product Status	Reference PCN
M4-128/64 (Cont'd)	M4-128/64-7VC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-128/64-10VC		
	M4-128/64-12VC		
	M4-128/64-15VC		
	M4-128/64-10VI		
	M4-128/64-12VI		
	M4-128/64-14VI		
	M4-128/64-18VI		
M4-128N/64	M4-128N/64-7JC	Active / Orderable	
	M4-128N/64-10JC		
	M4-128N/64-12JC		
	M4-128N/64-15JC		
	M4-128N/64-10JI		
	M4-128N/64-12JI		
	M4-128N/64-14JI		
	M4-128N/64-18JI		
M4-192/96	M4-192/96-7VC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-192/96-10VC		
	M4-192/96-12VC		
	M4-192/96-15VC		
	M4-192/96-10VI		
	M4-192/96-12VI		
	M4-192/96-14VI		
	M4-192/96-18VI		
M4-256/128	M4-256/128-7YC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-256/128-10YC		
	M4-256/128-12YC		
	M4-256/128-15YC		
	M4-256/128-10YI		
	M4-256/128-12YI		
	M4-256/128-14YI		
	M4-256/128-18YI		
M4LV-32/32	M4LV-32/32-7JC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-32/32-10JC		
	M4LV-32/32-12JC		
	M4LV-32/32-15JC		
	M4LV-32/32-10JI		
	M4LV-32/32-12JI		
	M4LV-32/32-14JI		
	M4LV-32/32-18JI		

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Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-32/32 (Cont'd)	M4LV-32/32-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-32/32-10VC		
	M4LV-32/32-12VC		
	M4LV-32/32-15VC		
	M4LV-32/32-10VI		
	M4LV-32/32-12VI		
	M4LV-32/32-14VI		
	M4LV-32/32-18VI		
	M4LV-32/32-7VC48		
	M4LV-32/32-10VC48		
	M4LV-32/32-12VC48		
	M4LV-32/32-15VC48		
	M4LV-32/32-10VI48		
	M4LV-32/32-12VI48		
	M4LV-32/32-14VI48		
	M4LV-32/32-18VI48		
M4LV-64/32	M4LV-64/32-7JC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-64/32-10JC		
	M4LV-64/32-12JC		
	M4LV-64/32-15JC		
	M4LV-64/32-10JI		
	M4LV-64/32-12JI		
	M4LV-64/32-14JI		
	M4LV-64/32-18JI		
	M4LV-64/32-7VC		
	M4LV-64/32-10VC		
	M4LV-64/32-12VC		
	M4LV-64/32-15VC		
	M4LV-64/32-10VI		
	M4LV-64/32-12VI		
	M4LV-64/32-14VI		
	M4LV-64/32-18VI		
	M4LV-64/32-7VC48		
	M4LV-64/32-10VC48		
	M4LV-64/32-12VC48		
	M4LV-64/32-15VC48		
	M4LV-64/32-10VI48		
	M4LV-64/32-12VI48		
	M4LV-64/32-14VI48		
	M4LV-64/32-18VI48		

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Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-96/48	M4LV-96/48-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-96/48-10VC		
	M4LV-96/48-12VC		
	M4LV-96/48-15VC		
	M4LV-96/48-10VI		
	M4LV-96/48-12VI		
	M4LV-96/48-14VI		
	M4LV-96/48-18VI		
M4LV-128/64	M4LV-128/64-7YC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-128/64-10YC		
	M4LV-128/64-12YC		
	M4LV-128/64-15YC		
	M4LV-128/64-10YI		
	M4LV-128/64-12YI		
	M4LV-128/64-14YI		
	M4LV-128/64-18YI		
	M4LV-128/64-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-128/64-10VC		
	M4LV-128/64-12VC		
	M4LV-128/64-15VC		
	M4LV-128/64-10VI		
	M4LV-128/64-12VI		
	M4LV-128/64-14VI		
	M4LV-128/64-18VI		
M4LV-128N/64	M4LV-128N/64-7JC	**Discontinued**	PCN#09-10
	M4LV-128N/64-10JC		
	M4LV-128N/64-12JC		
	M4LV-128N/64-15JC		
	M4LV-128N/64-10JI		
	M4LV-128N/64-12JI		
	M4LV-128N/64-14JI		
	M4LV-128N/64-18JI		
M4LV-192/96	M4LV-192/96-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-192/96-10VC		
	M4LV-192/96-12VC		
	M4LV-192/96-15VC		
	M4LV-192/96-10VI		
	M4LV-192/96-12VI		
	M4LV-192/96-14VI		
	M4LV-192/96-18VI		

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Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-256/128	M4LV-256/128-7YC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-256/128-10YC		
	M4LV-256/128-12YC		
	M4LV-256/128-15YC		
	M4LV-256/128-10YI		
	M4LV-256/128-12YI		
	M4LV-256/128-14YI		
	M4LV-256/128-18YI		
	M4LV-256/128-7AC		
	M4LV-256/128-10AC		
	M4LV-256/128-12AC		
	M4LV-256/128-15AC		
	M4LV-256/128-10AI		
	M4LV-256/128-12AI		
	M4LV-256/128-14AI		
	M4LV-256/128-18AI		

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MACH 4 CPLD Family

High Performance E^{2}CMOS® In-System Programmable Logic

FEATURES

- **High-performance, E^{2}CMOS 3.3-V & 5-V CPLD families**
- **Flexible architecture for rapid logic designs**
  - — Excellent First-Time-Fit™ and refit feature
  - — SpeedLocking™ performance for guaranteed fixed timing
  - — Central, input and output switch matrices for 100% routability and 100% pin-out rete
- **High speed**
  - — 7.5ns t_{PD} Commercial and 10ns t_{PD} Industrial
  - — 111.1MHz f_{CNT}
- **32 to 256 macrocells; 32 to 384 registers**
- **44 to 256 pins in PLCC, PQFP, TQFP and BGA packages**
- **Flexible architecture for a wide range of design styles**
  - — D/T registers and latches
  - — Synchronous or asynchronous mode
  - — Dedicated input registers
  - — Programmable polarity
  - — Reset/ preset swapping
- **Advanced capabilities for easy system integration**
  - — 3.3-V & 5-V JEDEC-compliant operations
  - — JTAG (IEEE 1149.1) compliant for boundary scan testing
  - — 3.3-V & 5-V JTAG in-system programming
  - — PCI compliant (-7/-10/-12 speed grades)
  - — Safe for mixed supply voltage system designs
  - — Bus-Friendly™ inputs and I/Os
  - — Programmable security bit
  - — Individual output slew rate control
- **Advanced E^{2}CMOS process provides high-performance, cost-effective solutions**
- **Supported by ispDesignEXPERT™ software for rapid logic development**
  - — Supports HDL design methodologies with results optimized for MACH 4
  - — Flexibility to adapt to user requirements
  - — Software partnerships that ensure customer success
- **Lattice and third-party hardware programming support**
  - — LatticePRO™ software for in-system programmability support on PCs and automated equipment
  - — Programming support on all major programmers including Data I/O, BP Microsystems, and System General

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Amendment/**0** Issue Date: **November 2003**

Table 1. MACH 4 Device Features[1, 2]

Feature	M4-32/32 M4LV-32/32	M4-64/32 M4LV-64/32	M4-96/48 M4LV-96/48	M4-128/64 M4LV-128/64	M4-128N/64 M4LV-128N/64	M4-192/96 M4LV-192/96	M4-2 M4LV-
Macrocells	32	64	96	128	128	192	
Maximum User I/O Pins	32	32	48	64	64	96	
t_{PD} (ns)	7.5	7.5	7.5	7.5	7.5	7.5	
f_{CNT} (MHz)	111	111	111	111	111	111	
t_{COS} (ns)	5.5	5.5	5.5	5.5	5.5	5.5	
t_{SS} (ns)	5.5	5.5	5.5	5.5	5.5	5.5	
Static Power (mA)	25	25	50	70	70	85	
JTAG Compliant	Yes	Yes	Yes	Yes	No	Yes	
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	

Notes:

1. *For information on the M4-96/96 device, please refer to the M4-96/96 data sheet at www.latticesemi.com.*
2. *"M4-xxx" is for 5-V devices. "M4LV-xxx" is for 3.3-V devices.*

GENERAL DESCRIPTION

The MACH® 4 family from Lattice offers an exceptionally flexible architecture and delive superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon pro and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The MACH 4 devices of densities ranging from 32 to 256 macrocells with 100% utilization and 100% pin-out reten The MACH 4 family offer 5-V (M4-xxx) and 3.3-V (M4LV-xxx) operation.

MACH 4 products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1 interface. JTAG boundary scan testing also allows product testability on automated test equipment for device connectivity.

All MACH 4 family members deliver First-Time-Fit and easy system integration with pin-o retention after any design change and refit. For both 3.3-V and 5-V operation, MACH 4 pro can deliver guaranteed fixed timing as fast as 7.5 ns t_{PD} and 111 MHz f_{CNT} through the SpeedLocking feature when using up to 20 product terms per output (Table 2).

Table 2. MACH 4 Speed Grades

Device	Speed Grade[1]					
	-7	-10	-12	-14	-15	-1
M4-32/32 M4LV-32/32	C	C, I	C, I	I	C	
M4-64/32 M4LV-64/32	C	C, I	C, I	I	C	
M4-96/48 M4LV-96/48	C	C, I	C, I	I	C	
M4-128/64 M4LV-128/64	C	C, I	C, I	I	C	
M4-128N/64 M4LV-128N/64	C	C, I	C, I	I	C	
M4-192/96 M4LV-192/96	C	C, I	C, I	I	C	
M4-256/128 M4LV-256/128	C	C, I	C, I	I	C	

Note:

1. C = Commercial, I = Industrial

The MACH 4 family offers numerous density-I/O combinations in Thin Quad Flat Pack (T Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), and Ball Grid Array (packages ranging from 44 to 256 pins (Table 3). It also offers I/O safety features for mix voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not ove 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable p down mode for extra power savings and individual output slew rate control for the highest transition or for the lowest noise transition.

Table 3. MACH 4 Package and I/O Options (Number of I/Os and dedicated inputs in Table)

Package	M4-32/32 M4LV-32/32	M4-64/32 M4LV-64/32	M4-96/48 M4LV-96/48	M4-128/64 M4LV-128/64	M4-128N/64 M4LV-128N/64	M4-192/96 M4LV-192/96	M4LV-
44-pin PLCC	32+2	32+2					
44-pin TQFP	32+2	32+2					
48-pin TQFP	32+2	32+2					
84-pin PLCC					64+6		
100-pin TQFP			48+8	64+6			
100-pin PQFP				64+6			
144-pin TQFP						96+16	
208-pin PQFP							12
256-ball BGA							12

FUNCTIONAL DESCRIPTION

The fundamental architecture of MACH 4 devices (Figure 1) consists of multiple, optimized blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the P blocks and central switch matrix allow the logic designer to create large designs in a sin device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect sch In MACH 4 architecture, the macrocells are flexibly coupled to the product terms throug logic allocator, and the I/O pins are flexibly coupled to the macrocells due to the output matrix. In addition, more input routing options are provided by the input switch matrix. resources provide the flexibility needed to fit designs efficiently.

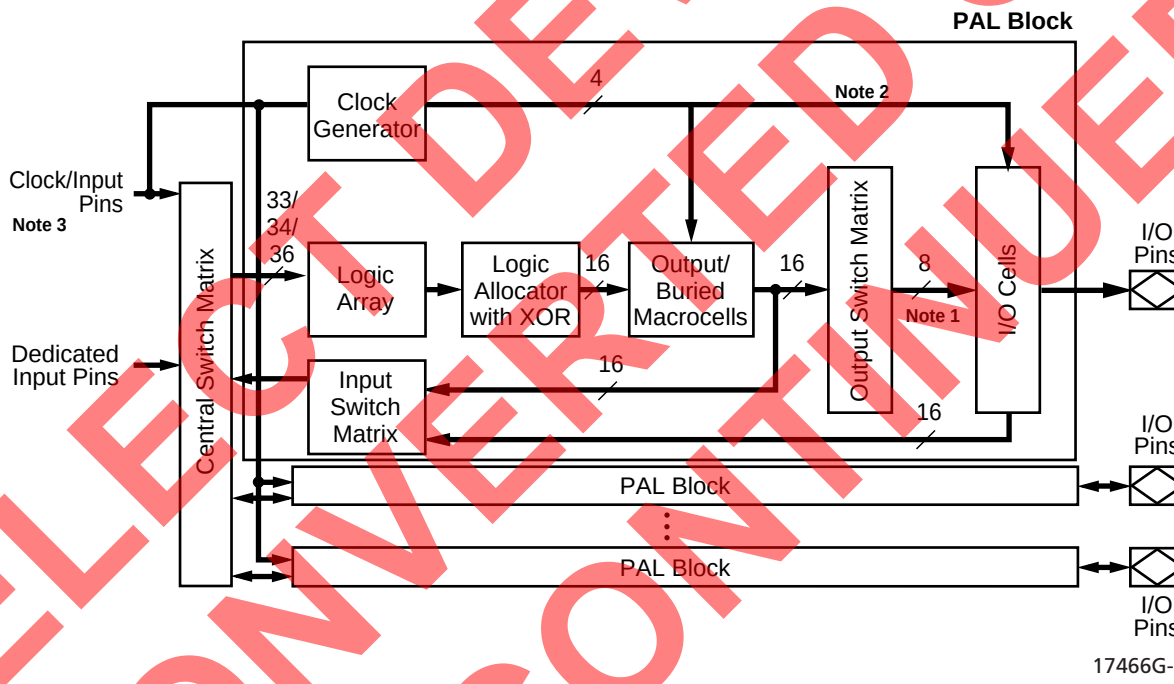


Figure 1. MACH 4 Block Diagram and PAL Block Structure

Notes:

1. *16 for MACH 4 devices with 1:1 macrocell-I/O cell ratio (see next page).*
2. *Block clocks do not go to I/O cells in M4(LV)-32/32.*
3. *M4(LV)-192/96 and M4(LV)-256/128 have dedicated clock pins which cannot be used as inputs and do not connect to th switch matrix.*

Table 4. Architectural Summary of MACH 4 devices

	MACH 4 Devices	
	M4-64/32, M4LV-64/32 M4-96/48, M4LV-96/48 M4-128/64, M4LV-128/64 M4-128N/64, M4LV-128N/64 M4-192/96, M4LV-192/96 M4-256/128, M4LV-256/128	M4-32/32 M4LV-32/32
Macrocell-I/O Cell Ratio	2:1	1:1
Input Switch Matrix	Yes	Yes
Input Registers	Yes	No
Central Switch Matrix	Yes	Yes
Output Switch Matrix	Yes	Yes

The Macrocell-I/O cell ratio is defined as the number of macrocells versus the number o cells internally in a PAL block (Table 4).

The central switch matrix takes all dedicated inputs and signals from the input switch ma and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL still must go through the central switch matrix. This mechanism ensures that PAL blocks in 4 devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a MACH 4 device more advanced than simply several P devices on a single chip. It allows the designer to think of the device not as a collection blocks, but as a single programmable device; the software partitions the design into PAL through the central switch matrix so that the designer does not have to be concerned wi internal architecture of the device.

Each PAL block consists of:

- Product-term array
- Logic allocator
- Macrocells
- Output switch matrix
- I/O cells
- Input switch matrix
- Clock generator

Product-Term Array

The product-term array consists of a number of product terms that form the basis of the being implemented. The inputs to the AND gates come from the central switch matrix (Ta and are provided in both true and complement forms for efficient logic implementation.

Table 5. PAL Block Inputs

Device	Number of Inputs to PAL Block
M4-32/32 and M4LV-32/32	33
M4-64/32 and M4LV-64/32	33
M4-96/48 and M4LV-96/48	33
M4-128/64 and M4LV-128/64	33
M4-128N/64 and M4LV-128N/64	33
M4-192/96 and M4LV-192/96	34
M4-256/128 and M4LV-256/128	34

Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in "product term clu The availability and distribution of product term clusters are automatically considered by software as it fits functions within a PAL block. The size of a product term cluster has be optimized to provide high utilization of product terms, making complex functions using product terms possible. Yet when few product terms are used, there will be a minimal nu of unused—or wasted—product terms left over. The product term clusters available to e macrocell within a PAL block are shown in Tables 6 and 7.

Each product term cluster is associated with a macrocell. The size of a cluster depends c configuration of the associated macrocell. When the macrocell is used in synchronous m (Figure 2a), the basic cluster has 4 product terms. When the associated macrocell is used asynchronous mode (Figure 2b), the cluster has 2 product terms. Note that if the produc cluster is routed to a different macrocell, the allocator configuration is not determined by mode of the macrocell actually being driven. The configuration is always set by the mode macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give ar extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If inc with the basic cluster, this provides for up to 20 product terms on a synchronous functio uses four extended 5-product-term clusters. A similar asynchronous function can have up product terms.

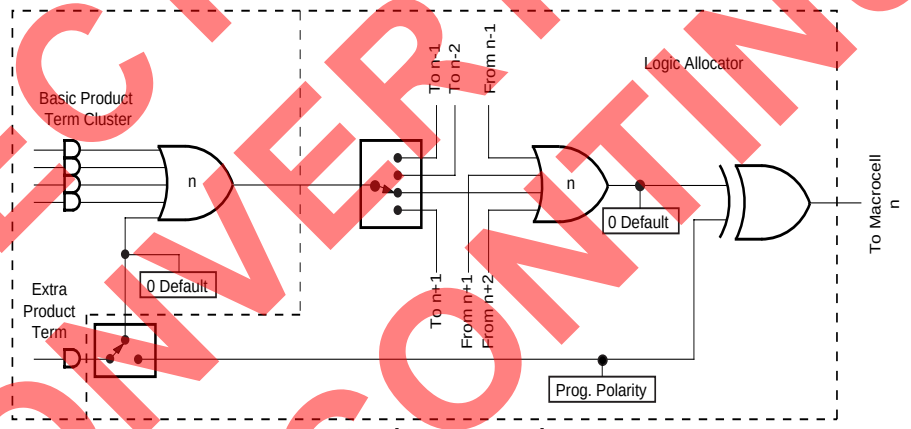
When the extra product term is used to extend the cluster, the value of the second XOR can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the allocator are shown in Figures 3 and 4.

Table 6. Logic Allocator for All MACH 4 Devices (except M4(LV)-32/32)

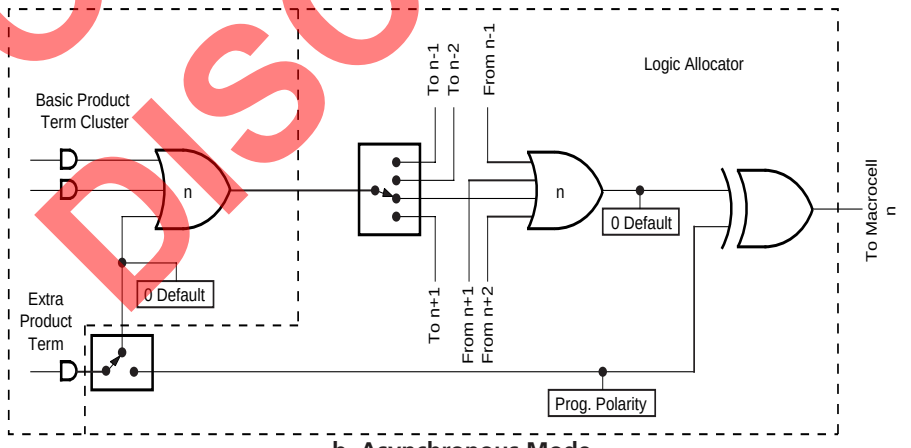
Output Macrocell	Available Clusters	Output Macrocell	Available Cluster
M_0	C_0, C_1, C_2	M_8	C_7, C_8, C_9, C_{10}
M_1	C_0, C_1, C_2, C_3	M_9	C_8, C_9, C_{10}, C_{11}
M_2	C_1, C_2, C_3, C_4	M_{10}	$C_9, C_{10}, C_{11}, C_{12}$
M_3	C_2, C_3, C_4, C_5	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_4	C_3, C_4, C_5, C_6	M_{12}	$C_{11}, C_{12}, C_{13}, C_{14}$
M_5	C_4, C_5, C_6, C_7	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_6	C_5, C_6, C_7, C_8	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7, C_8, C_9	M_{15}	C_{14}, C_{15}

Table 7. Logic Allocator for M4(LV)-32/32

Output Macrocell	Available Clusters	Output Macrocell	Available Cluster
M_0	C_0, C_1, C_2	M_8	C_8, C_9, C_{10}
M_1	C_0, C_1, C_2, C_3	M_9	C_8, C_9, C_{10}, C_{11}
M_2	C_1, C_2, C_3, C_4	M_{10}	$C_9, C_{10}, C_{11}, C_{12}$
M_3	C_2, C_3, C_4, C_5	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_4	C_3, C_4, C_5, C_6	M_{12}	$C_{11}, C_{12}, C_{13}, C_{14}$
M_5	C_4, C_5, C_6, C_7	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_6	C_5, C_6, C_7	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7	M_{15}	C_{14}, C_{15}

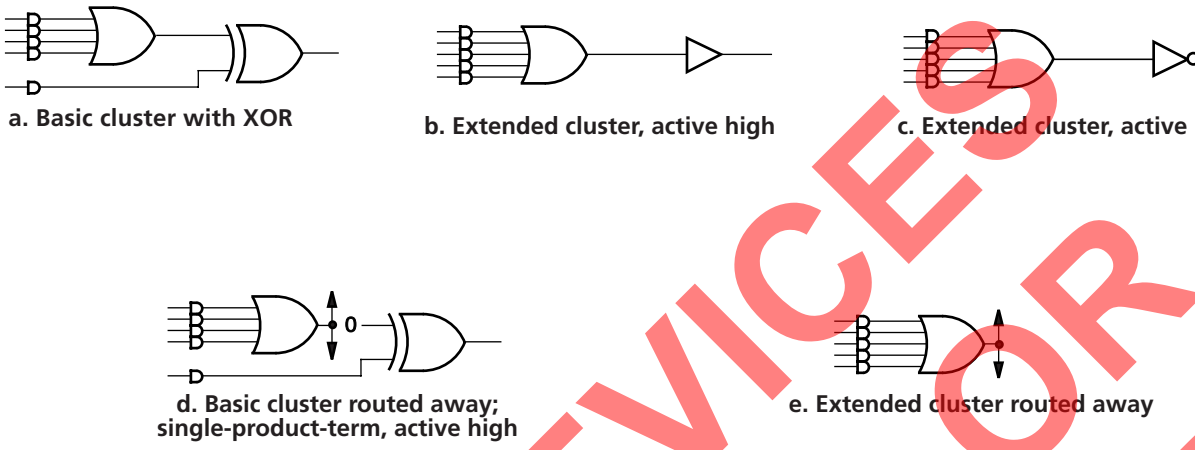


a. Synchronous Mode



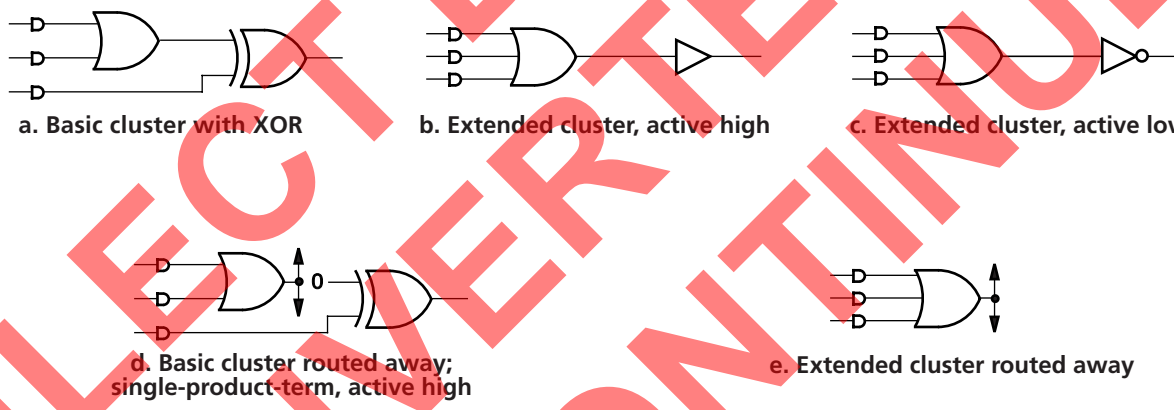
b. Asynchronous Mode

Figure 2. Logic Allocator: Configuration of Cluster "n" Set by Mode of Macrocell "n"



174

Figure 3. Logic Allocator Configurations: Synchronous Mode



174

Figure 4. Logic Allocator Configurations: Asynchronous Mode

Note that the configuration of the logic allocator has absolutely no impact on the speed signal. All configurations have the same delay. This means that designers do not have to c between optimizing resources or speed; both can be optimized.

If not used in the cluster, the extra product term can act in conjunction with the basic clu provide XOR logic for such functions as data comparison, or it can work with the D-,T-typ flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is rout another macrocell, the extra product term is still available for logic. In this case, the first input will be a logic 0. This circuit has the flexibility to route product terms elsewhere w giving up the use of the macrocell.

Product term clusters do not “wrap” around a PAL block. This means that the macrocells ends of the block have fewer product terms available.

Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.

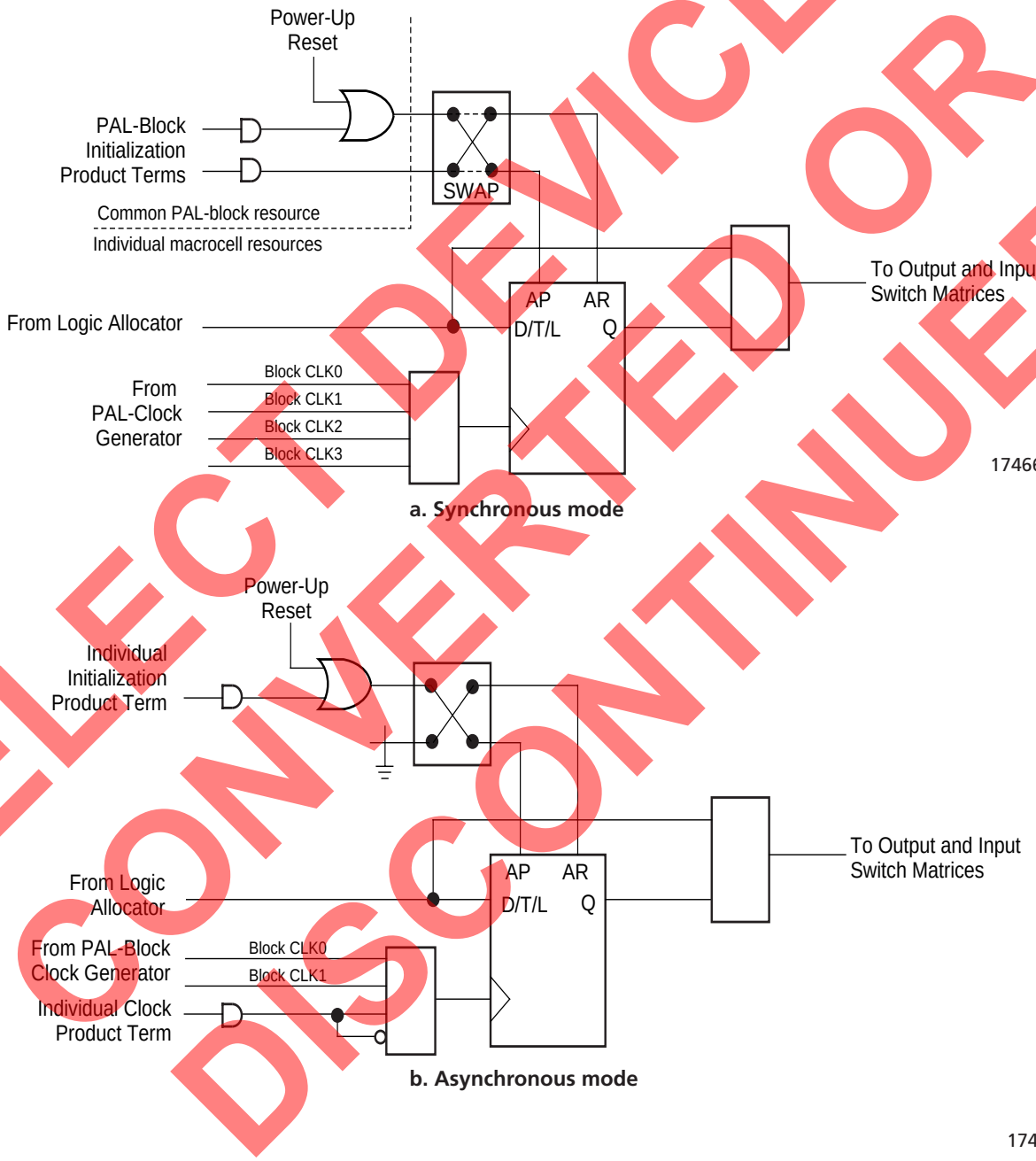
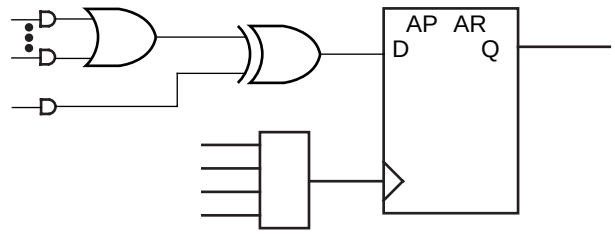


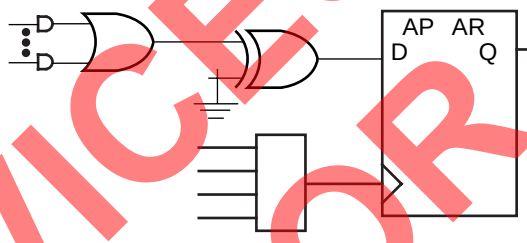
Figure 5. Macrocell

In either mode, a combinatorial path can be used. For combinatorial logic, the synchron mode will generally be used, since it provides more product terms in the allocator.

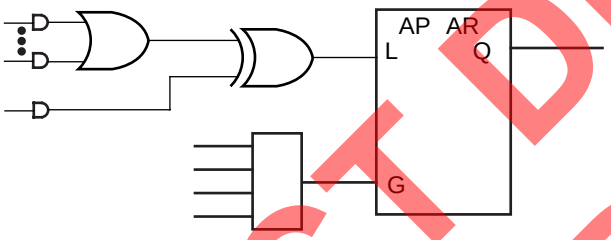
The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as cause oscillation if both J and K inputs are HIGH.



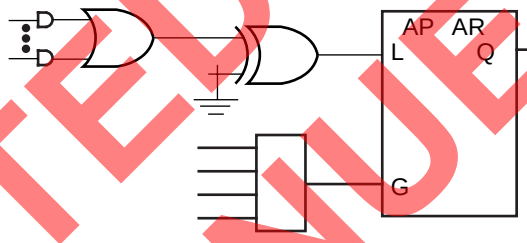
a. D-type with XOR



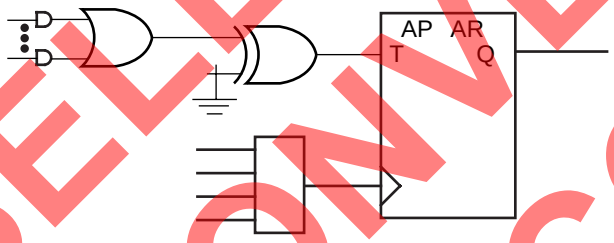
b. D-type with programmable D pola



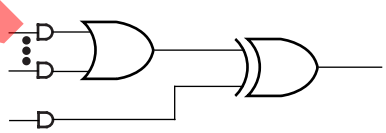
c. Latch with XOR



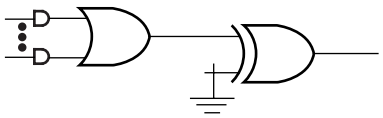
d. Latch with programmable D polar



e. T-type with programmable T polarity



f. Combinatorial with XOR



g. Combinatorial with programmable polarity

Figure 6. Primary Macrocell Configurations

Table 8. Register/Latch Operation

Configuration	Input(s)	CLK/LE [1]	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
D-type Latch	D=X	1 (0)	Q
	D=0	0 (1)	0
	D=1	0 (1)	1

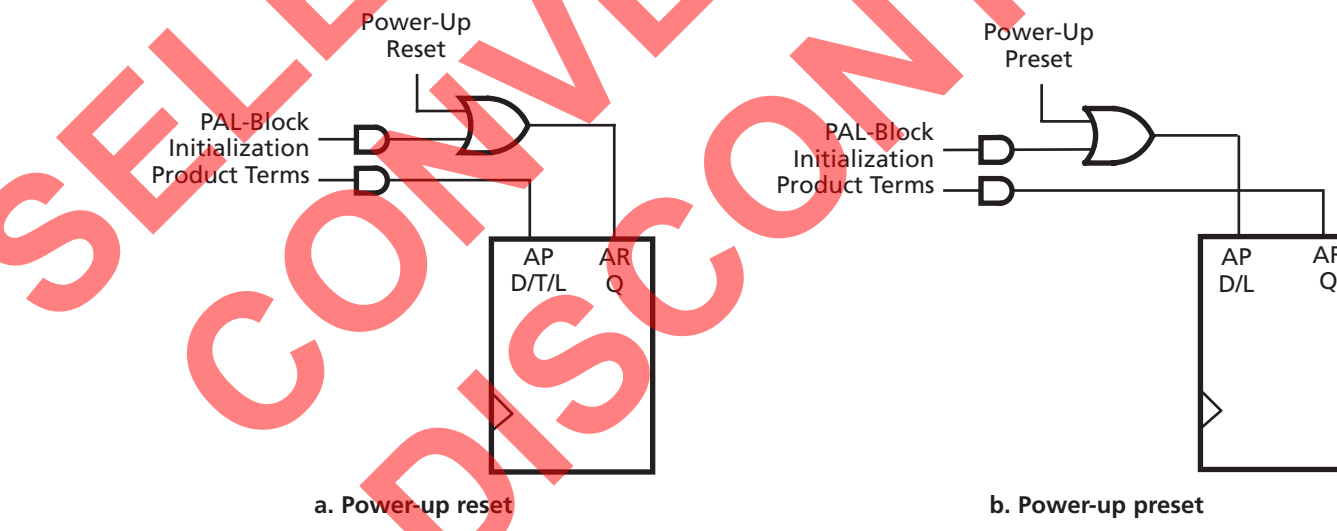
Note:

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic all allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available p terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, extra product term must be used on the XOR gate input for flip-flop emulation. In any r type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchr reset and preset are provided, each driven by a product term common to the entire PAL



a. Power-up reset **b. Power-up preset**

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Figure 7. Synchronous Mode Initialization Configurations

A reset/preset swapping feature in each macrocell allows for reset and preset to be excha
providing flexibility. In asynchronous mode (Figure 8), a single individual product term
provided for initialization. It can be selected to control reset or preset.

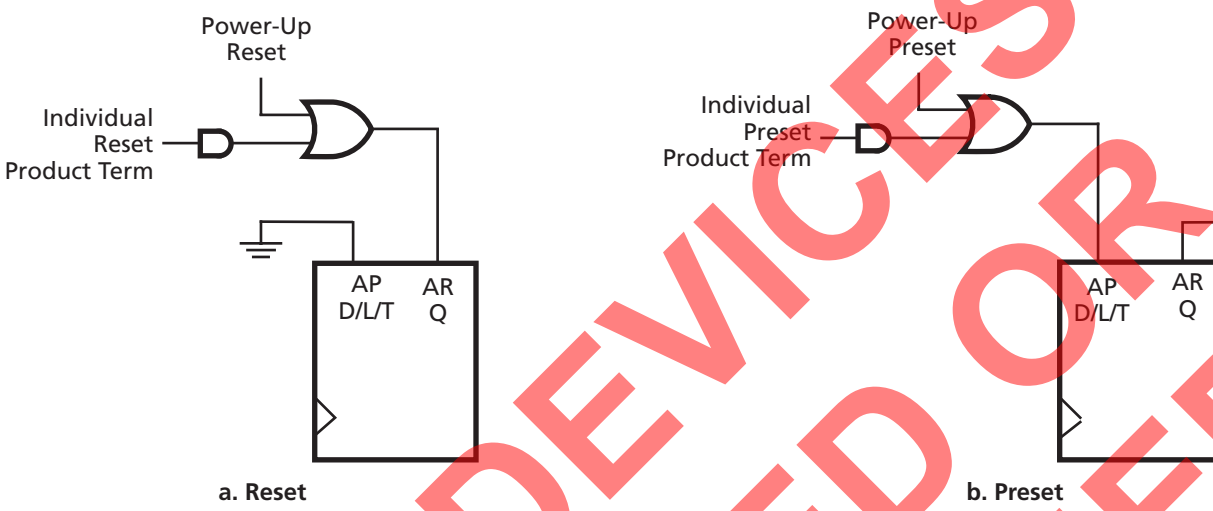


Figure 8. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature effects power-up reset as well. The
initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends it
to the output switch matrix and the input switch matrix. The output switch matrix can rou
data to an output if so desired. The input switch matrix can send the signal back to the c
switch matrix as feedback.

Table 9. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE[1]	Q+
0	0	X	See Table 8
0	1	X	1
1	0	X	0
1	1	X	0

Note:

1. Transparent latch is unaffected by AR, AP

Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells w
PAL block. This provides high flexibility in determining pinout and allows design change
occur without effecting pinout.

In MACH 4 devices with 2:1 Macrocell-I/O cell ratio, each PAL block has twice as many
macrocells as I/O cells. The MACH 4 output switch matrix allows for half of the macroce
drive I/O cells within a PAL block, in combinations according to Figure 9. Each I/O cell
choose from eight macrocells; each macrocell has a choice of four I/O cells. The MACH 4 d
with 1:1 Macrocell-I/O cell ratio allow each macrocell to drive one of eight I/O cells (Fig

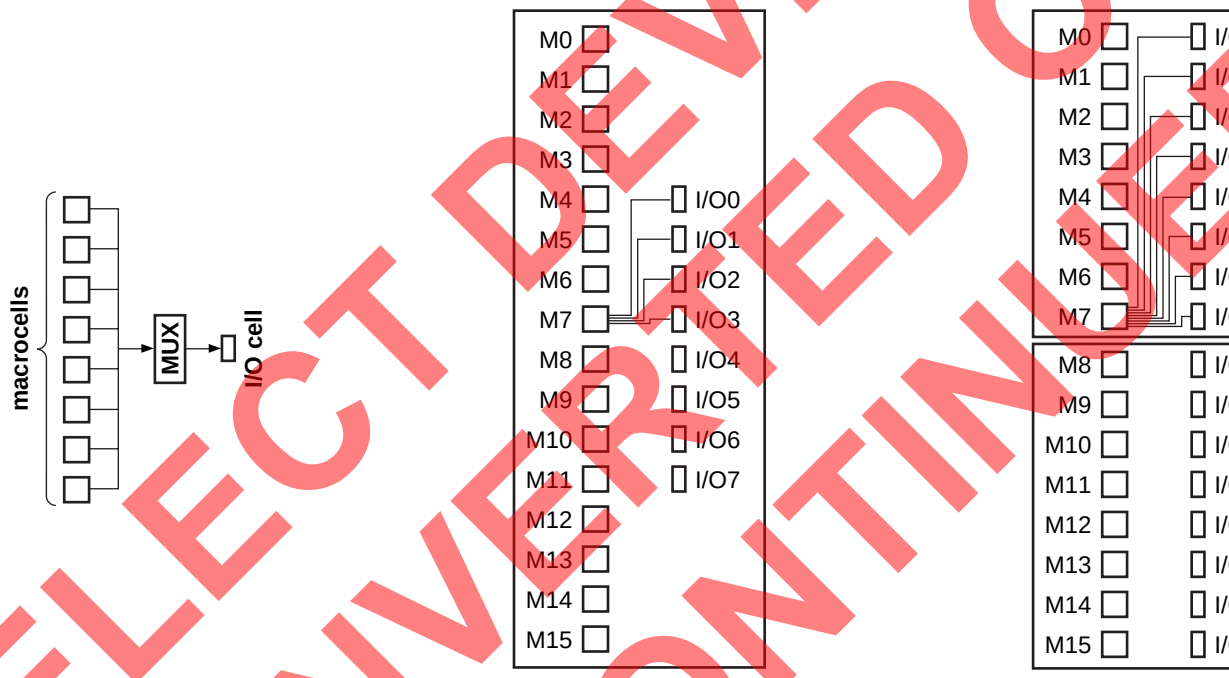


Figure 9. MACH 4 Output Switch Matrix

Table 10. Output Switch Matrix Combinations for MACH 4 Devices with 2:1 Macrocell-I/O Cell Ratio

Macrocell	Routable to I/O Cells
M0, M1	I/O0, I/O5, I/O6, I/O7
M2, M3	I/O0, I/O1, I/O6, I/O7
M4, M5	I/O0, I/O1, I/O2, I/O7
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7

I/O Cell	Available Macrocells
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M0, M1, M10, M11, M12, M13, M14, M15
I/O6	M0, M1, M2, M3, M12, M13, M14, M15
I/O7	M0, M1, M2, M3, M4, M5, M14, M15

Table 11. Output Switch Matrix Combinations for M4(LV)-32/32

Macrocell	Routable to I/O Cells
M0, M1, M2, M3, M4, M5, M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9, M10, M11, M12, M13, M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7	M0, M1, M2, M3, M4, M5, M6, M7
I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15	M8, M9, M10, M11, M12, M13, M14, M15

I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a fee path, and flip-flop (except MACH 4 devices with 1:1 macrocell-I/O cell ratio.) An individ output enable product term is provided for each I/O cell. The feedback signal drives the switch matrix.

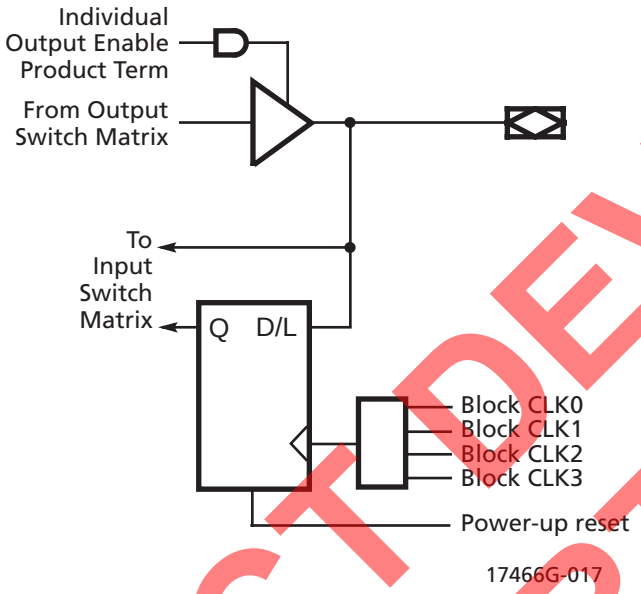


Figure 10. I/O Cell for MACH 4 Devices with 2:1 Macrocell-I/O Cell Ratio

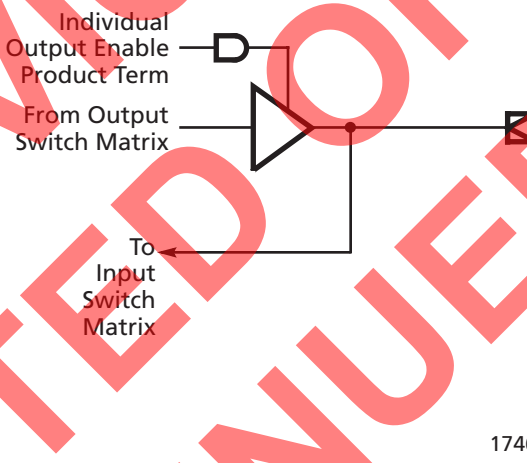


Figure 11. I/O Cell for MACH 4 Devices with Macrocell-I/O Cell Ratio

The I/O cell (Figure 10) contains a flip-flop, which provides the capability for storing the in a D-type register or latch. The clock can be any of the PAL block clocks. Both the dire registered versions of the input are sent to the input switch matrix. This allows for such fun as "time-domain-multiplexed" data comparison, where the first data value is stored, and th second data value is put on the I/O pin and compared with the previous stored value.

Note that the flip-flop used in the MACH 4 I/O cell is independent of the flip-flops in th macrocells. It powers up to a logic low.

Zero-Hold-Time Input Register

The MACH 4 devices have a zero-hold-time (ZHT) fuse which controls the time delay asso with loading data into all I/O cell registers and latches. When programmed, the ZHT fus increases the data path setup delays to input storage elements, matching equivalent dela the clock path. When the fuse is erased, the setup time to the input storage element is mini This feature facilitates doing worst-case designs for which data is loaded from sources w have low (or zero) minimum output propagation delays from clock edges.

Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central sw matrix. Without the input switch matrix, each input and feedback signal has only one wa enter the central switch matrix. The input switch matrix provides additional ways for the signals to enter the central switch matrix.

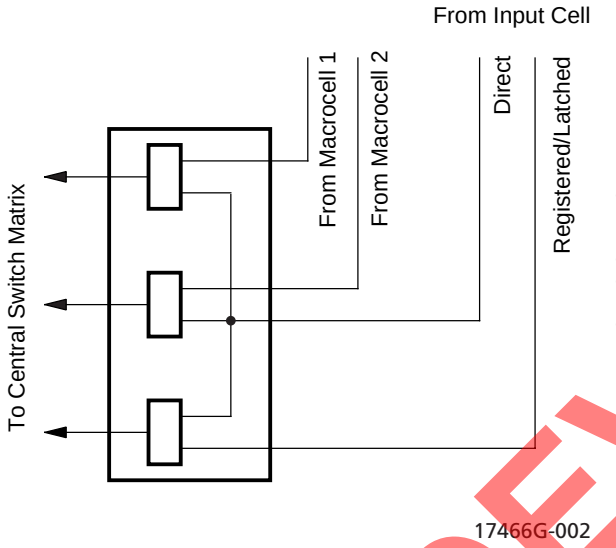


Figure 12. MACH 4 with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

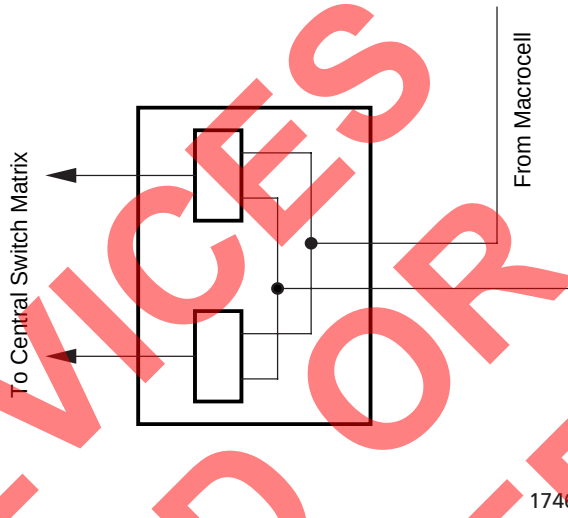


Figure 13. MACH 4 with 1:1 Macrocell-I/O Cell - Input Switch Matrix

PAL Block Clock Generation

Each MACH 4 device has four clock pins that can also be used as inputs. These pins driv clock generator in each PAL block (Figure 14). The clock generator provides four clock s that can be used anywhere in the PAL block. These four PAL block clock signals can con a large number of combinations of the true and complement edges of the global clock si Table 12 lists the possible combinations.

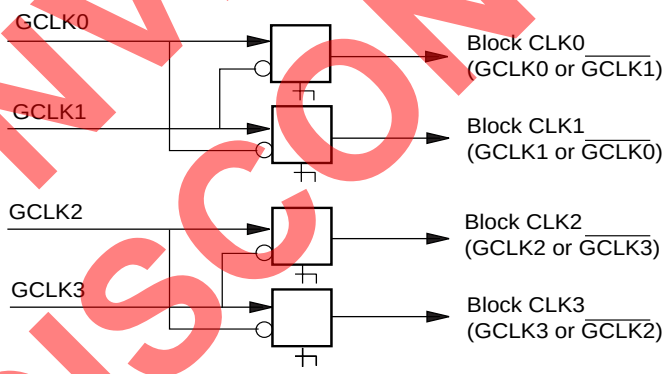


Figure 14. PAL Block Clock Generator [1]

Note:

1. *M4(LV)-32/32 and M4(LV)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 t GCLK1.*

Table 12. PAL Block Clock Combinations[1]

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{\text{GCLK1}}$	GCLK1	X	X
GCLK0	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	GCLK2 (GCLK0)	GCLK3 (GCLK1)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	GCLK3 (GCLK1)
X	X	GCLK2 (GCLK0)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)
X	X	$\overline{\text{GCLK3}}$ (GCLK1)	$\overline{\text{GCLK2}}$ (GCLK0)

Note:

1. Values in parentheses are for the M4(LV)-32/32 and M4(LV)-64/32.

This feature provides high flexibility for partitioning state machines and dual-phase cloc
also allows latches to be driven with either polarity of latch enable, and in a master-slav
configuration.

MACH 4 TIMING MODEL

The primary focus of the MACH 4 timing model is to accurately represent the timing in a M 4 device, and at the same time, be easy to understand. This model accurately describes a combinatorial and registered paths through the device, making a distinction between int feedback and external feedback. A signal uses internal feedback when it is fed back into switch matrix or block without having to go through the output buffer. The input registe specifications are also reported as internal feedback. When a signal is fed back into the s matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF}, is defined as the time it takes to go from feedback through the output to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the para designator is followed by an "i". By adding t_{BUF} to this internal parameter, the external para is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MAC timing model is shown in Figure 15. Refer to the Technical Note entitled *MACH 4 Timing High Speed Design* for a more detailed discussion about the timing parameters.

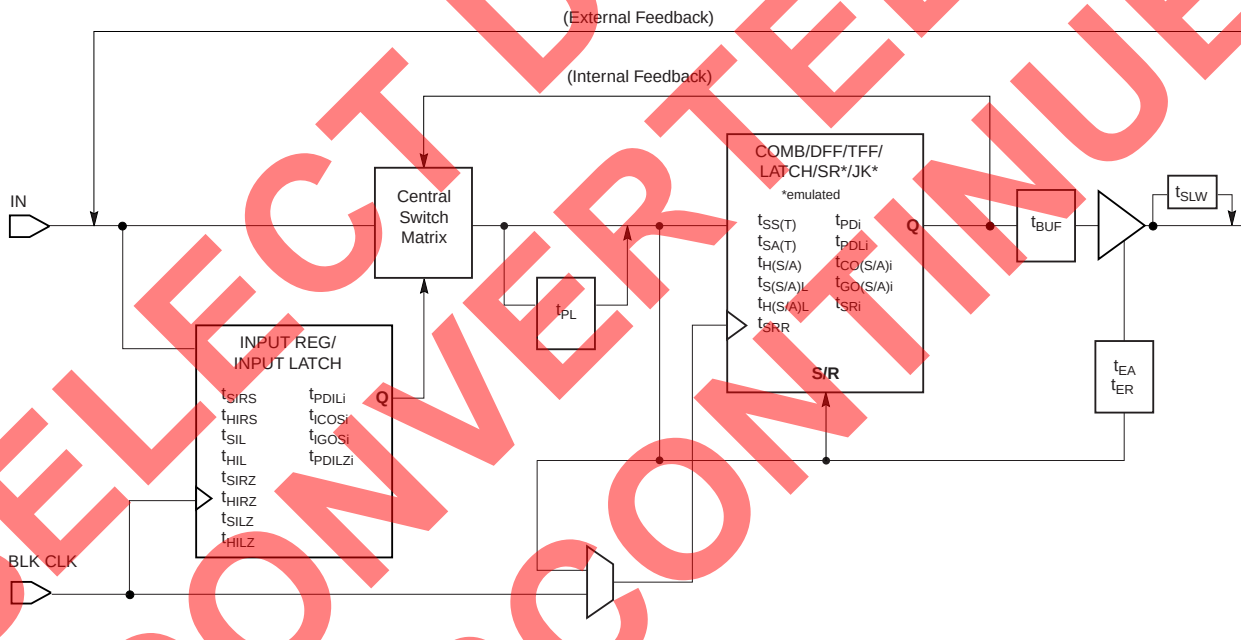


Figure 15. MACH 4 Timing Model

SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The MACH 4 architecture allows allocation of up to 20 product terms to an individual mac with the assistance of an XOR gate without incurring additional timing delays.

The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that i independent of the logic required by the design. Other competitive CPLDs incur serious t delays as product terms expand beyond their typical 4 or 5 product term limits. Speed *a* SpeedLocking combine to give designs easy access to the performance required in today designs.

IEEE 1149.1-COMPLIANT BOUNDARY SCAN TESTABILITY

All MACH 4 devices, except the M4(LV)-128N/64, have boundary scan cells and are com to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which device is mounted through a serial scan path that can access all critical logic nodes. Inte registers are linked internally, allowing test data to be shifted in and loaded directly onto nodes, or test node data to be captured and shifted out for verification. In addition, these d can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1-COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapi prototyping, lower inventory levels, higher quality, and the ability to make in-field modifica All MACH 4 devices provide In-System Programming (ISP) capability through their Boun ScanTest Access Ports. This capability has been implemented in a manner that ensures th port remains compliant to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communi interface through which ISP is achieved, customers get the benefit of a standard, well-de interface.

MACH 4 devices can be programmed across the commercial temperature and voltage rang PC-based LatticePRO software facilitates in-system programming of MACH 4 devices. Lattic takes the JEDEC file output produced by the design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the chain. LatticePRO software can use these vectors to drive a JTAG chain via the parallel po PC. Alternatively, LatticePRO software can output files in formats understood by commo automated test equipment. This equpment can then be used to program MACH 4 devices d the testing of a circuit board.

PCI COMPLIANT

MACH 4 devices in the -7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devic fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI con to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

Both the 3.3-V and 5-V V_{CC} MACH 4 devices are safe for mixed supply voltage system de The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, whil accept inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Bo 5-V and 3.3-V versions have the same high-speed performance and provide easy-to-use voltage design capability.

BUS-FRIENDLY INPUTS AND I/OS

All MACH 4 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorpo two inverters in series which loop back to the input. This double inversion weakly holds input at its last driven logic state. While it is good design practice to tie unused pins to a k state, the Bus-Friendly input structure pulls pins away from the input threshold voltage v noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are res logic level “1.” For the circuit diagram, please refer to the document entitled *MACH Endu Characteristics* on the Lattice/Vantis Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

Each individual PAL block in MACH 4 devices features a programmable low-power mode, results in power savings of up to 50%. The signal speed paths in the low-power PAL bloc be slower than those in the non-low-power PAL block. This feature allows speed critical to run at maximum frequency while the rest of the signal paths operate in the low-power

PROGRAMMABLE SLEW RATE

Each MACH 4 device I/O has an individually programmable output slew rate control bit. output can be individually configured for the higher speed transition (3 V/ns) or for the noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. designs with short traces or well terminated lines, the fast slew rate can be used to achie highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macroc configured to SET on a signal from the control generator, then that macrocell will be SET device power-up. If a macrocell is configured to RESET on a signal from the control gen or is not configured for set/reset, then that macrocell will RESET on power-up. To guara initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive unt reset delay time has elapsed.

SECURITY BIT

A programmable security bit is provided on the MACH 4 devices as a deterrent to unauth copying of the array configuration patterns. Once programmed, this bit defeats readback programmed pattern by a device programmer, securing proprietary designs from compet Programming and verification are also defeated by the security bit. The bit can only be re erasing the entire device.

Figure 16. PAL Block for MACH 4 with 2:1 Macrocell - I/O Cell Ratio

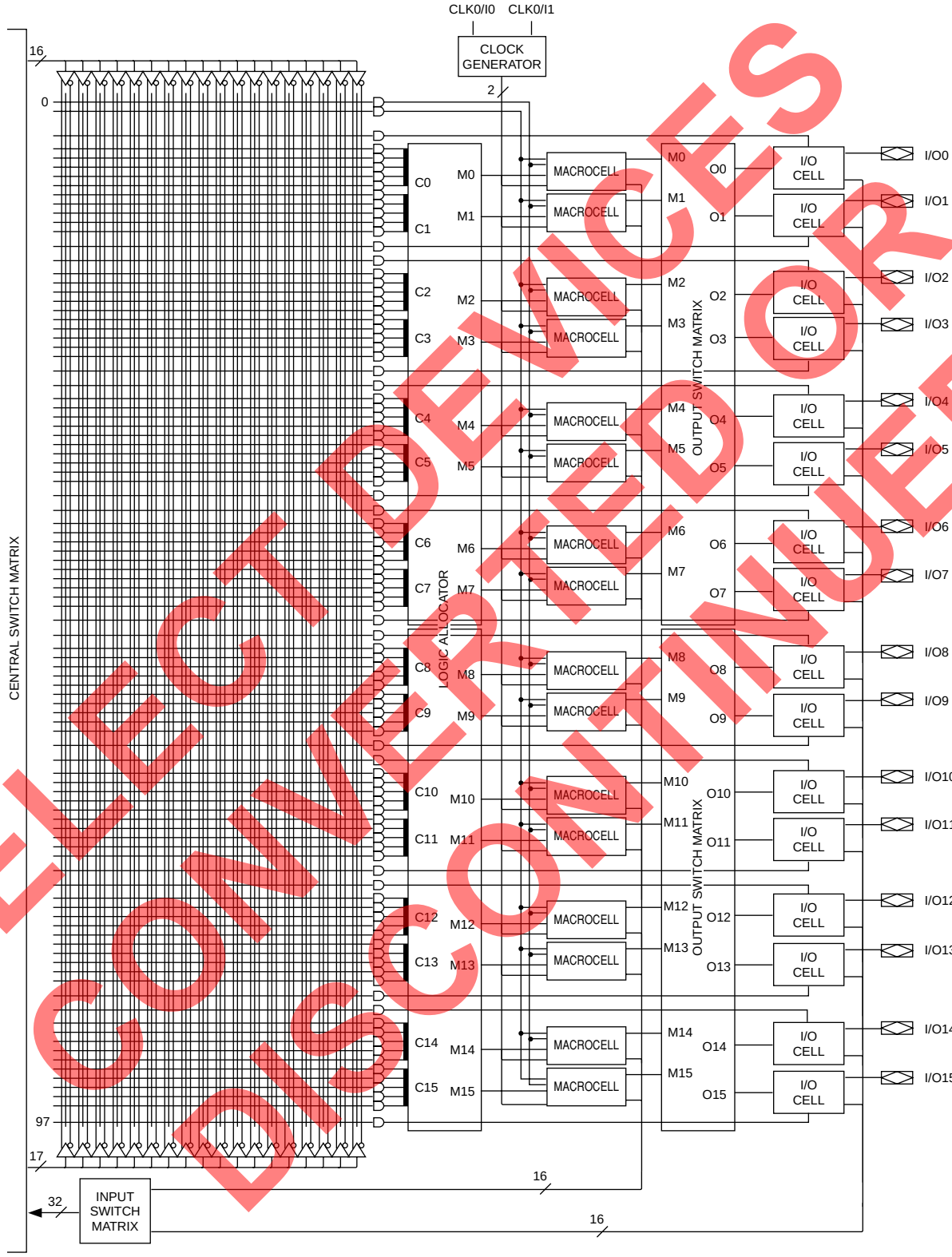
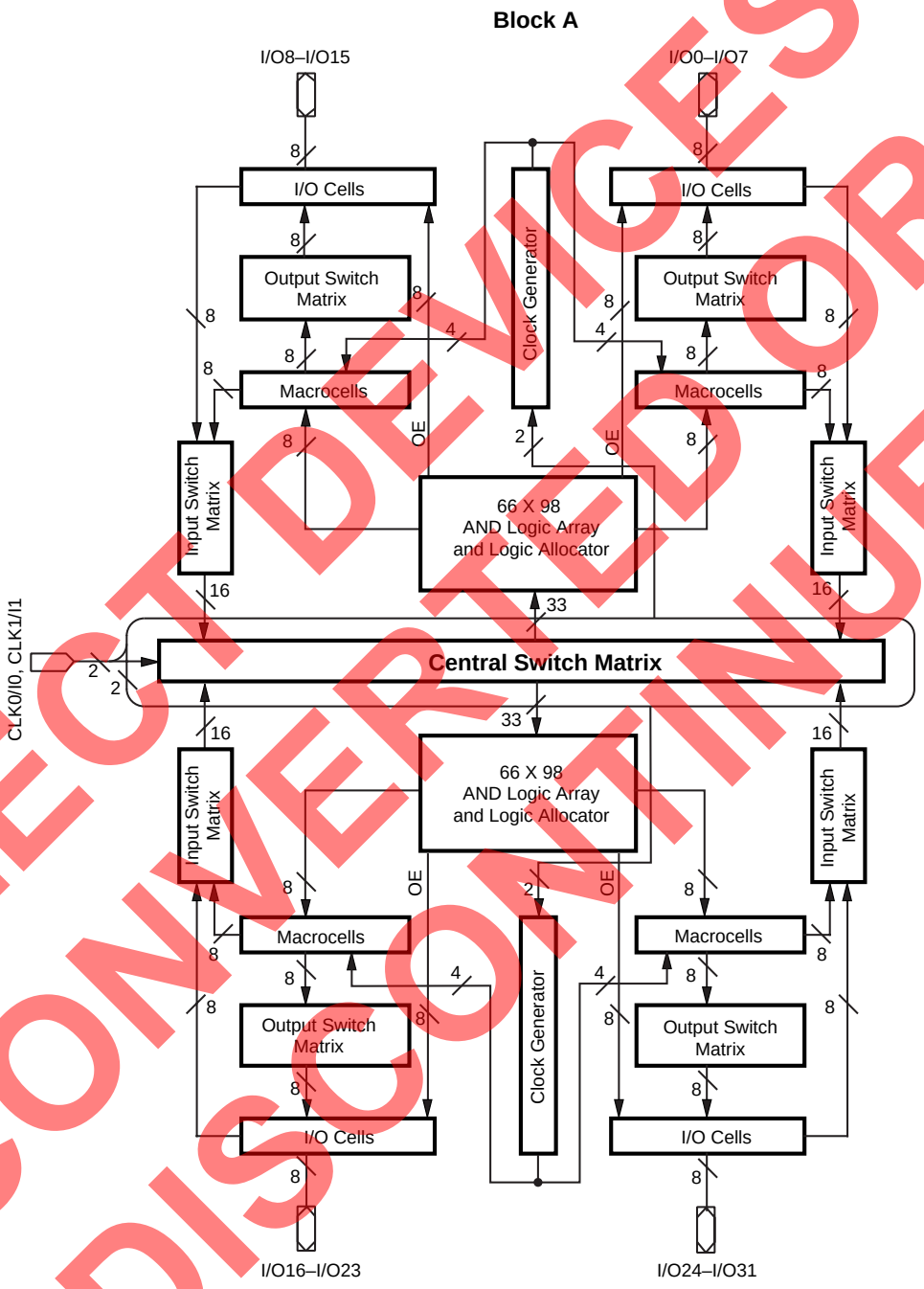


Figure 17. PAL Block for M4(LV)-32/32

BLOCK DIAGRAM – M4(LV)-32/32



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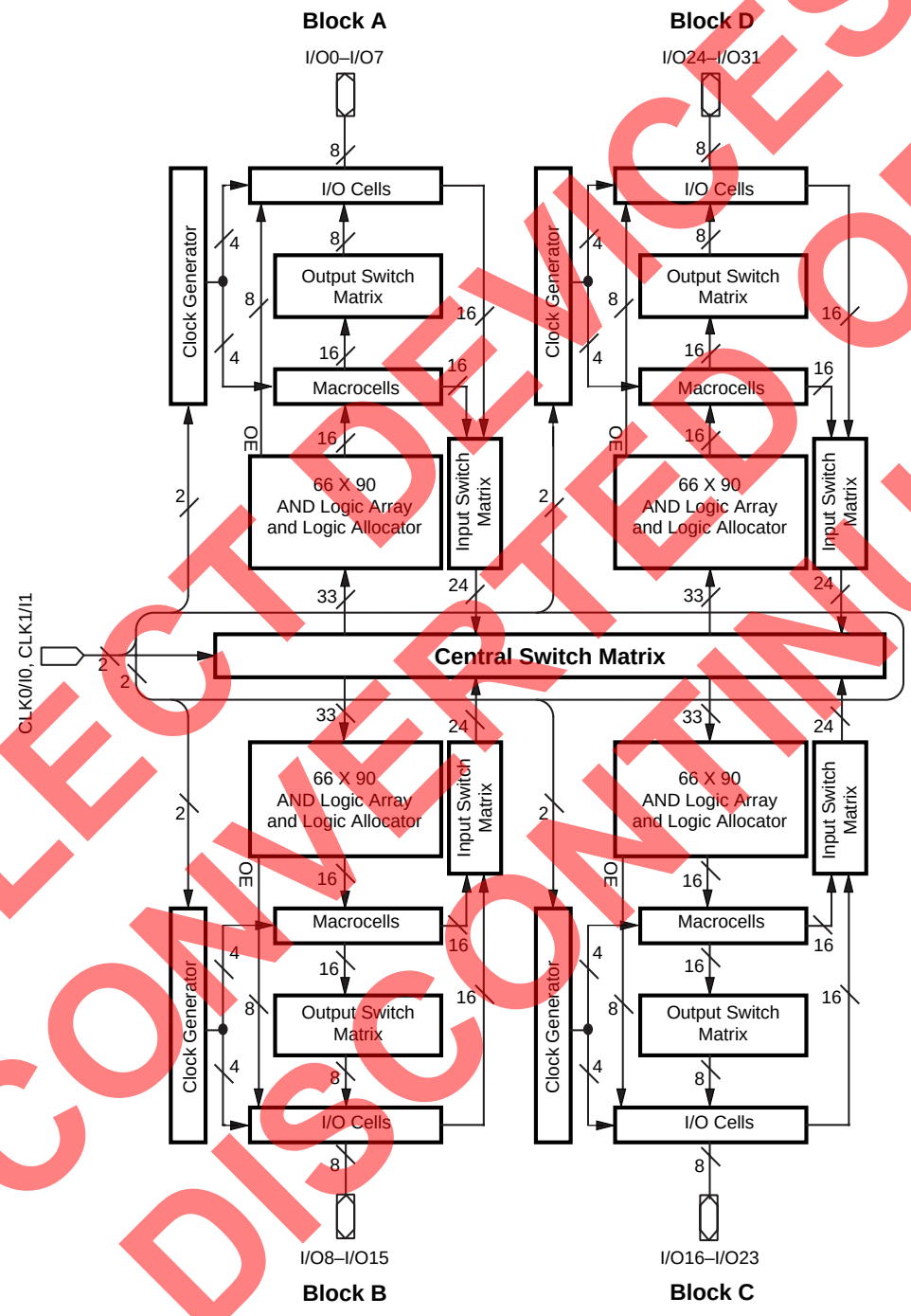
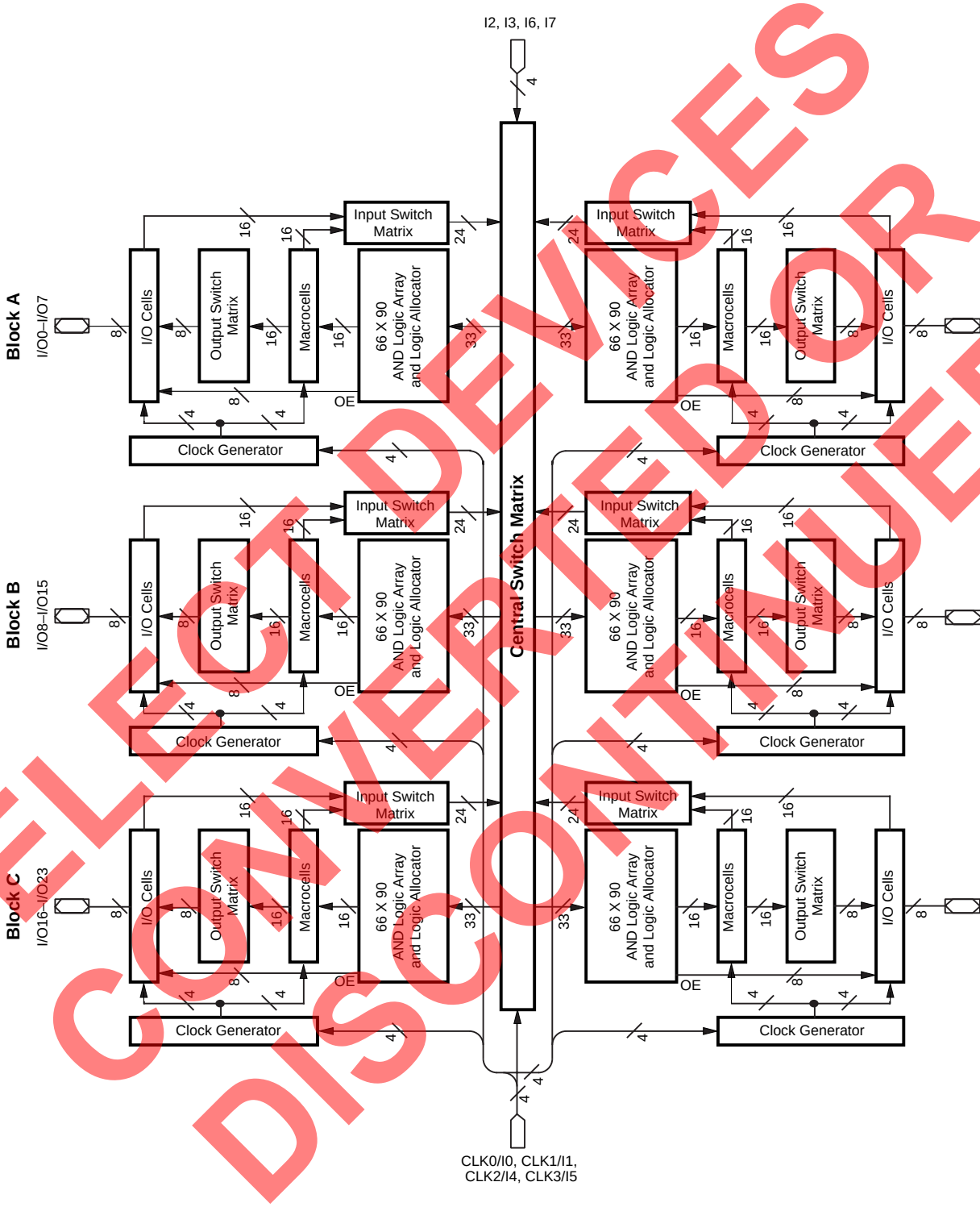
BLOCK DIAGRAM – M4(LV)-64/32

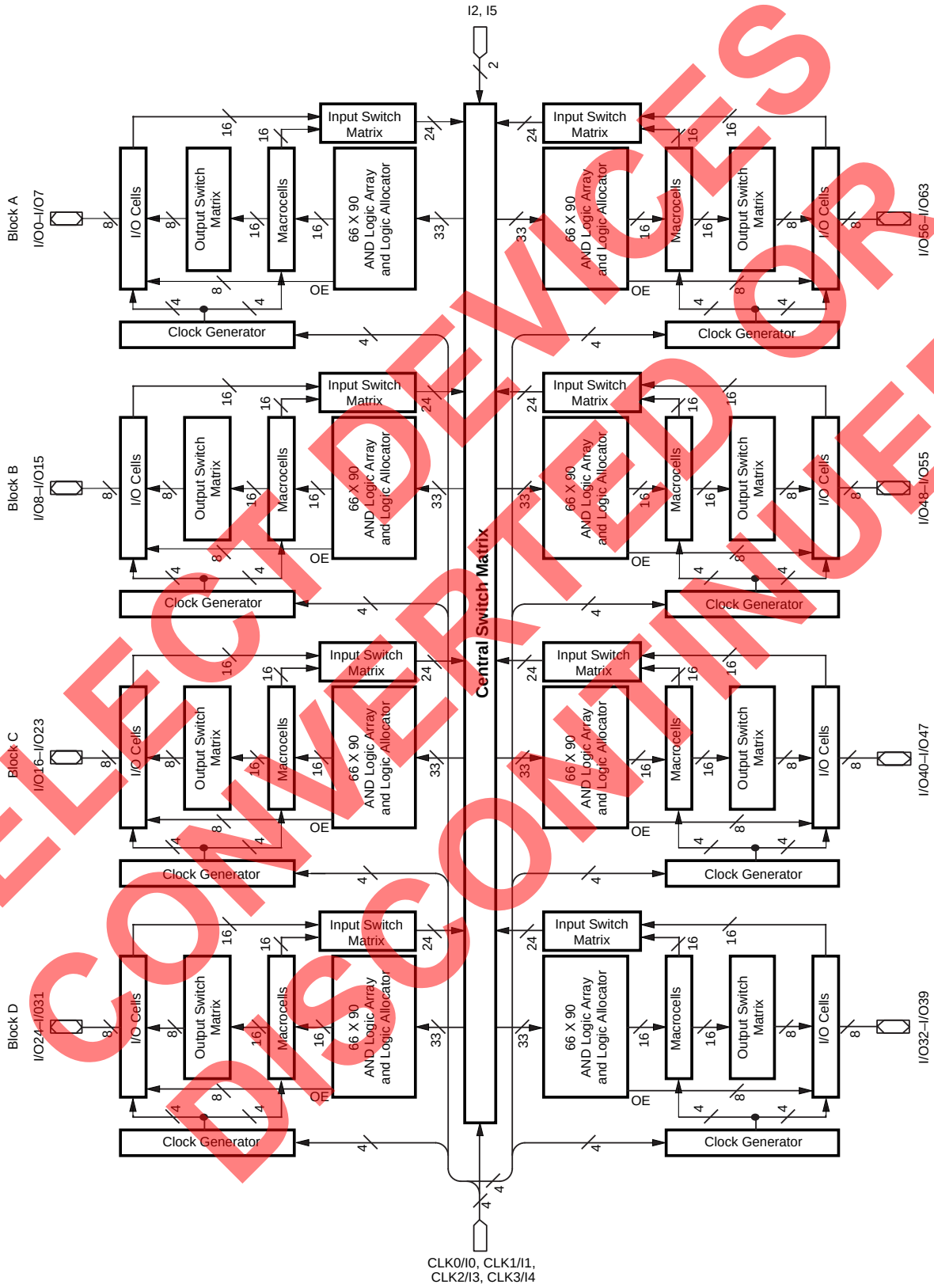


17466H

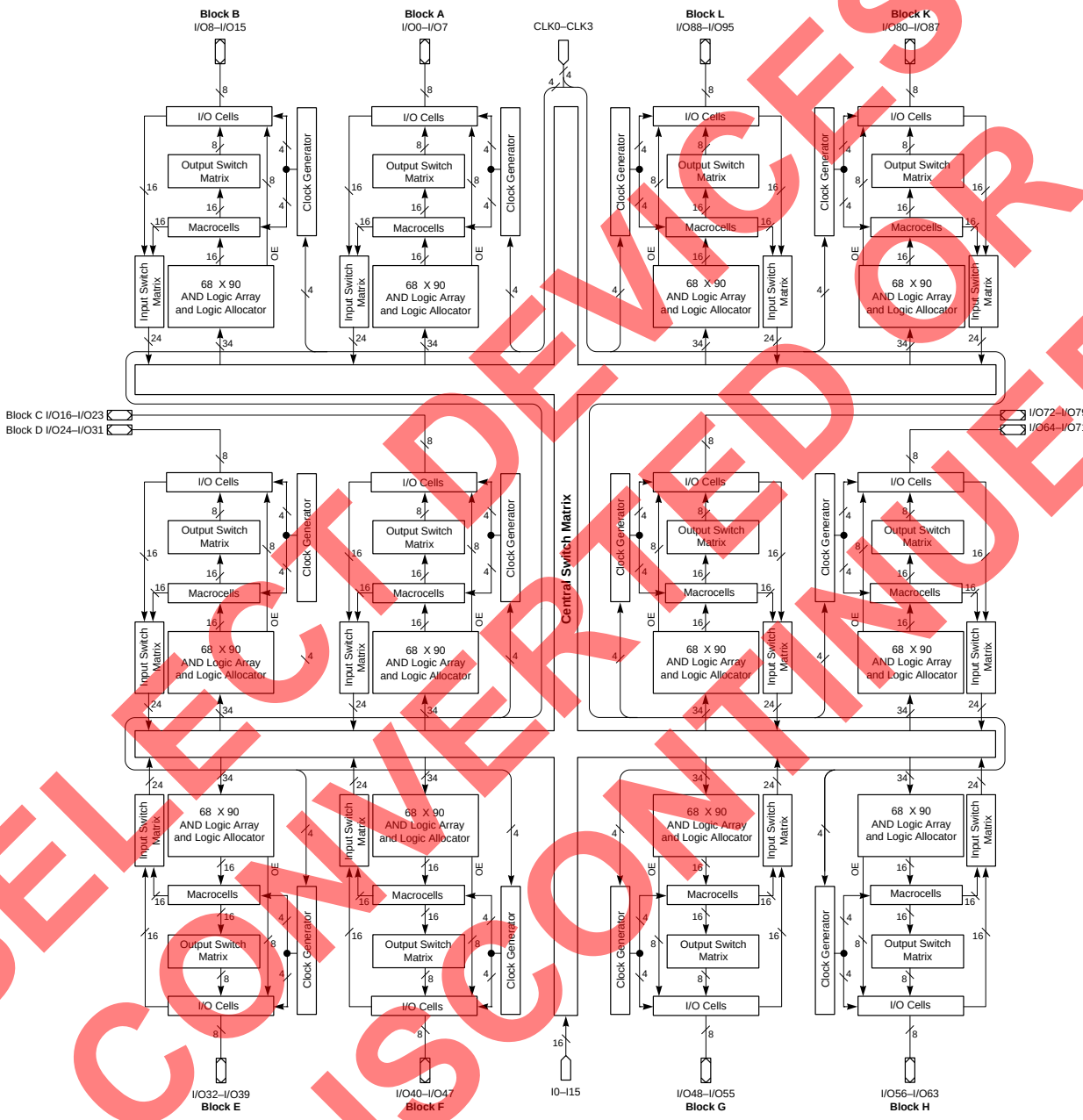
BLOCK DIAGRAM – M4(LV)-96/48



BLOCK DIAGRAM – M4(LV)-128N/64 AND M4(LV)-128/64

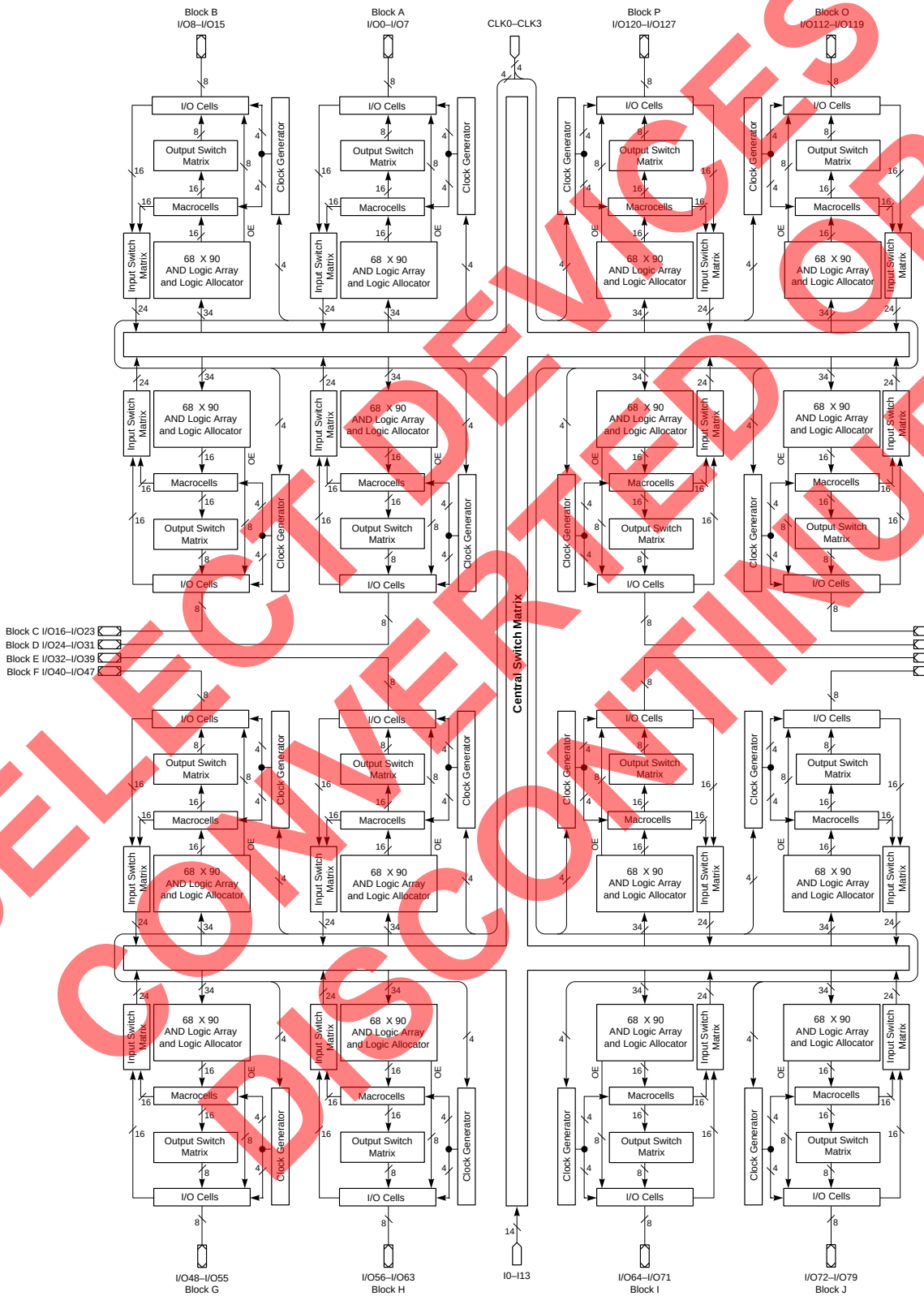


BLOCK DIAGRAM – M4(LV)-192/96



17466G

BLOCK DIAGRAM – M4(LV)-256/128



ABSOLUTE MAXIMUM RATINGS

M4

Storage Temperature . . . . . .-65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . .-0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . 0°C t

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . -40°C t

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.50 V t

Operating ranges define those limits between which tionality of the device is guaranteed.

5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4		
		I_{OH} = 0 mA, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL}			3.3
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0		
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			10
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max , V_{IN} = V_{IH} or V_{IL} (Note 3)			–10
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

ABSOLUTE MAXIMUM RATINGS

M4LV

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +4.5 V

DC Input Voltage . . . . . -0.5 V to 6.0 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C t

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C t

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to

Operating ranges define those limits between which tionality of the device is guaranteed.

3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 µA	V_{CC} – 0.2		
			I_{OH} = –3.2 mA	2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2
			I_{OL} = 24 mA			0.5
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		5.5
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		–0.3		0.8
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				5
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–5
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				5
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				–5
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–15		–160

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*

MACH 4 TIMING PARAMETERS OVER OPERATING RANGES[1]

		-7		-10		-12		-14		-15		-18	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Ma
Combinatorial Delay:													
t_{PDi}	Internal combinatorial propagation delay		5.5		8.0		10.0		12.0		13.0		16.
t_{PD}	Combinatorial propagation delay		7.5		10.0		12.0		14.0		15.0		18.
Registered Delays:													
t_{SS}	Synchronous clock setup time, D-type register	5.5		6.0		7.0		10.0		10.0		12.0	
t_{SST}	Synchronous clock setup time, T-type register	6.5		7.0		8.0		11.0		11.0		13.0	
t_{SA}	Asynchronous clock setup time, D-type register	3.5		4.0		5.0		8.0		8.0		10.0	
t_{SAT}	Asynchronous clock setup time, T-type register	4.5		5.0		6.0		9.0		9.0		11.0	
t_{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0	
t_{HA}	Asynchronous clock hold time	3.5		4.0		5.0		8.0		8.0		10.0	
t_{COSi}	Synchronous clock to internal output		3.5		4.5		6.0		8.0		8.0		10.
t_{COS}	Synchronous clock to output		5.5		6.5		8.0		10.0		10.0		12.
t_{COAi}	Asynchronous clock to internal output		7.5		10.0		12.0		16.0		16.0		18.
t_{COA}	Asynchronous clock to output		9.5		12.0		14.0		18.0		18.0		20.
Latched Delays:													
t_{SSL}	Synchronous Latch setup time	6.0		7.0		8.0		10.0		10.0		12.0	
t_{SAL}	Asynchronous Latch setup time	4.0		4.0		5.0		8.0		8.0		10.0	
t_{HSL}	Synchronous Latch hold time	0.0		0.0		0.0		0.0		0.0		0.0	
t_{HAL}	Asynchronous Latch hold time	4.0		4.0		5.0		8.0		8.0		10.0	
t_{PDLi}	Transparent latch to internal output		8.0		10.0		12.0		15.0		15.0		18.
t_{PDL}	Propagation delay through transparent latch to output		10.0		12.0		14.0		17.0		17.0		20.
t_{GOSi}	Synchronous Gate to internal output		4.0		5.5		8.0		9.0		9.0		10.
t_{GOS}	Synchronous Gate to output		6.0		7.5		10.0		11.0		11.0		12.
t_{GOAi}	Asynchronous Gate to internal output		9.0		11.0		14.0		17.0		17.0		20.
t_{GOA}	Asynchronous Gate to output		11.0		13.0		16.0		19.0		19.0		22.
Input Register Delays:													
t_{SIRS}	Input register setup time	2.0		2.0		2.0		2.0		2.0		2.0	
t_{HIRS}	Input register hold time	3.0		3.0		3.0		4.0		4.0		4.0	
t_{ICOSi}	Input register clock to internal feedback		3.5		4.5		6.0		6.0		6.0		6.0
Input Latch Delays:													
t_{SIL}	Input latch setup time	2.0		2.0		2.0		2.0		2.0		2.0	
t_{HIL}	Input latch hold time	3.0		3.0		3.0		4.0		4.0		4.0	
t_{IGOSi}	Input latch gate to internal feedback		4.0		4.0		4.0		5.0		5.0		6.0
t_{PDILi}	Transparent input latch to internal feedback		2.0		2.0		2.0		2.0		2.0		2.0
Input Register Delays with ZHT Option:													
t_{SIRZ}	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0	
t_{HIRZ}	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0	

MACH 4 TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUE

		-7		-10		-12		-14		-15		-18	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Ma
Input Latch Delays with ZHT Option:													
t_{SILZ}	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0	
t_{HILZ}	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0	
t_{PDILZi}	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0
Output Delays:													
t_{BUF}	Output buffer delay		2.0		2.0		2.0		2.0		2.0		2.0
t_{SLW}	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5
t_{EA}	Output enable time		9.5		10.0		12.0		15.0		15.0		17.
t_{ER}	Output disable time		9.5		10.0		12.0		15.0		15.0		17.
Power Delay:													
t_{PL}	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5
Reset and Preset Delays:													
t_{SRi}	Asynchronous reset or preset to internal register output		10.0		12.0		14.0		18.0		18.0		20.
t_{SR}	Asynchronous reset or preset to register output		12.0		14.0		16.0		20.0		20.0		22.
t_{SRR}	Asynchronous reset and preset register recovery time	8.0		8.0		10.0		15.0		15.0		17.0	
t_{SRW}	Asynchronous reset or preset width	10.0		10.0		12.0		15.0		15.0		17.0	
Clock/LE Width:													
t_{WLS}	Global clock width low	3.0		5.0		6.0		6.0		6.0		7.0	
t_{WHS}	Global clock width high	3.0		5.0		6.0		6.0		6.0		7.0	
t_{WLA}	Product term clock width low	4.0		5.0		8.0		9.0		9.0		10.0	
t_{WHA}	Product term clock width high	4.0		5.0		8.0		9.0		9.0		10.0	
t_{GWS}	Global gate width low (for low transparent) or high (for high transparent)	5.0		5.0		6.0		6.0		6.0		7.0	
t_{GWA}	Product term gate width low (for low transparent) or high (for high transparent)	4.0		5.0		6.0		9.0		9.0		11.0	
t_{WIRL}	Input register clock width low	4.5		5.0		6.0		6.0		6.0		7.0	
t_{WIRH}	Input register clock width high	4.5		5.0		6.0		6.0		6.0		7.0	
t_{WIL}	Input latch gate width	5.0		5.0		6.0		6.0		6.0		7.0	

MACH 4 TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUE

		-7		-10		-12		-14		-15		-18	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Ma
Frequency:													
f_{MAXS}	External feedback, D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	90.9		80.0		66.7		50.0		50.0		41.7	
	External feedback, T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COS})$	83.3		74.1		62.5		47.6		47.6		40.0	
	Internal feedback (f_{CNT}), D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	111.1		95.2		76.9		55.6		55.6		45.5	
	Internal feedback (f_{CNT}), T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COSi})$	100.0		87.0		71.4		52.6		52.6		43.5	
	No feedback[2], Min of $1/(t_{WLS} + t_{WHS})$, $1/(t_{SS} + t_{HS})$ or $1/(t_{SST} + t_{HS})$	153.8		100.0		83.3		83.3		83.3		71.4	
f_{MAXA}	External feedback, D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	76.9		62.5		52.6		38.5		38.5		33.3	
	External feedback, T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COA})$	71.4		58.8		50.0		37.0		37.0		32.3	
	Internal feedback (f_{CNTA}), D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	90.9		71.4		58.8		41.7		41.7		35.7	
	Internal feedback (f_{CNTA}), T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COAi})$	83.3		66.7		55.6		40.0		40.0		34.5	
	No feedback[2], Min of $1/(t_{WLA} + t_{WHA})$, $1/(t_{SA} + t_{HA})$ or $1/(t_{SAT} + t_{HA})$	125.0		100.0		62.5		55.6		55.6		50.0	
f_{MAXI}	Maximum input register frequency, Min of $1/(t_{WIRH} + t_{WIRL})$ or $1/(t_{SIRS} + t_{HIRS})$	111.0		100.0		83.3		83.3		83.3		71.4	

Notes:

1. *See "MACH Switching Test Circuit" document on the Literature Download page of the Lattice web site.*
2. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ
C_{IN}	Input capacitance	V_{IN}=2.0 V	3.3 V or 5 V, 25°C, 1 MHz	6
$C_{I/O}$	Output capacitance	V_{OUT}=2.0V	3.3 V or 5 V, 25°C, 1 MHz	8

Note:

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modifi this parameter may be affected.*

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system fr
cy. The selected "typical" pattern is a 16-bit up-down counter. This pattern fills the devic
exercises every macrocell. Maximum frequency shown uses internal feedback and a D-typ
ister. Power/Speed are optimized to obtain the highest counter frequency and the lowest p
The highest frequency (LSBs) is placed in common PAL blocks, which are set to high powe
lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest po

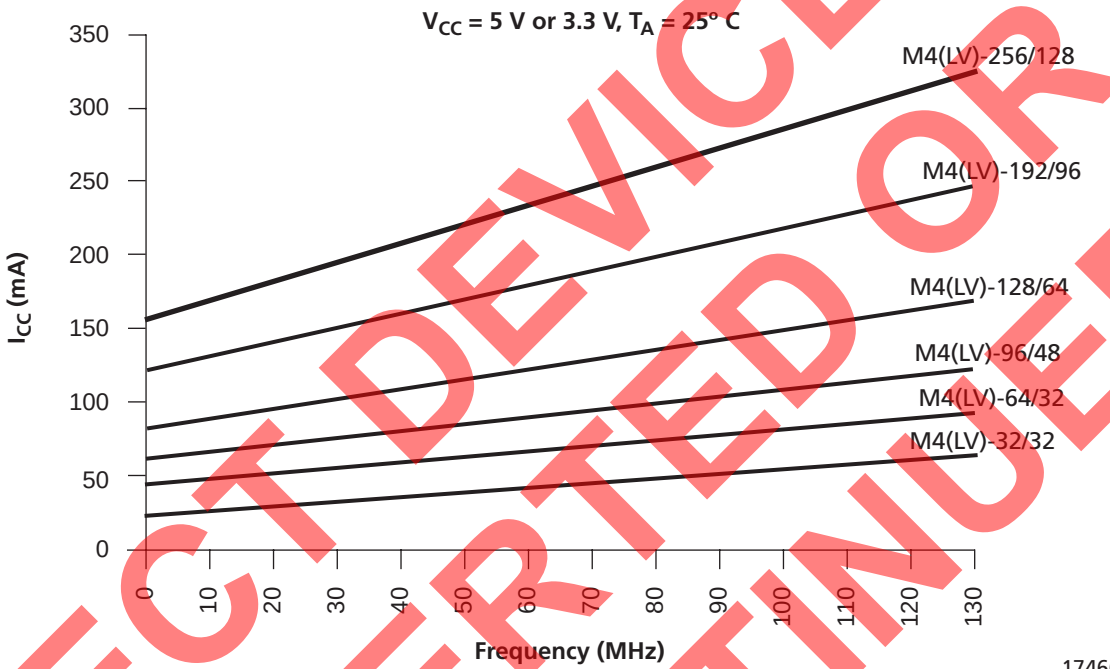


Figure 18. MACH 4 I_{CC} Curves at High Speed Mode

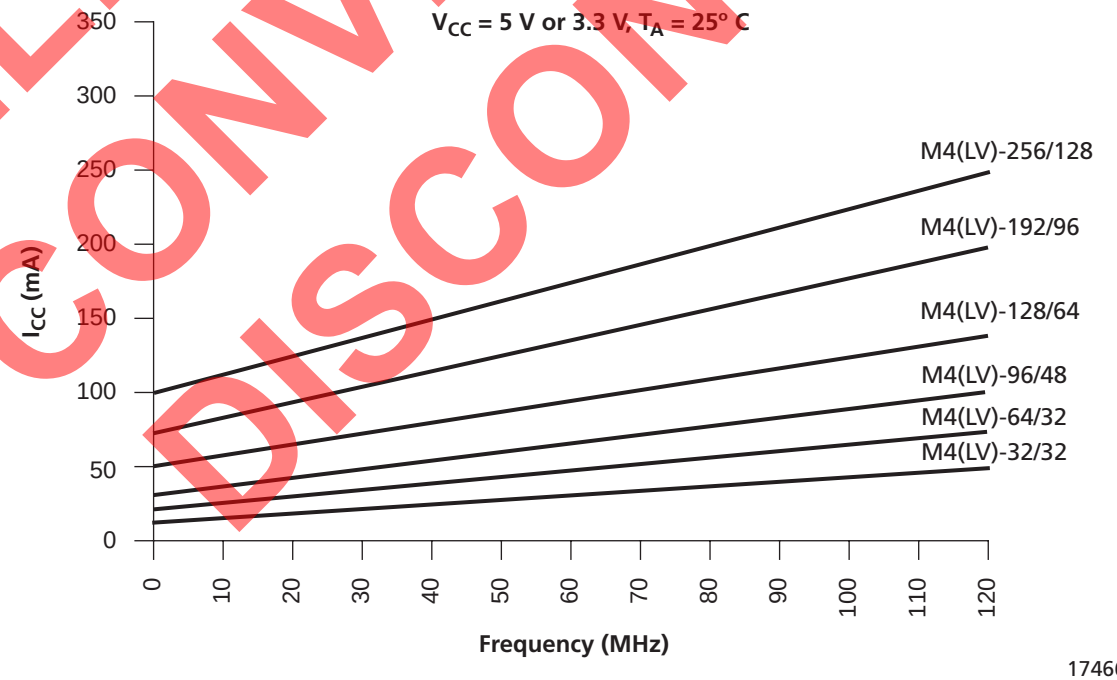
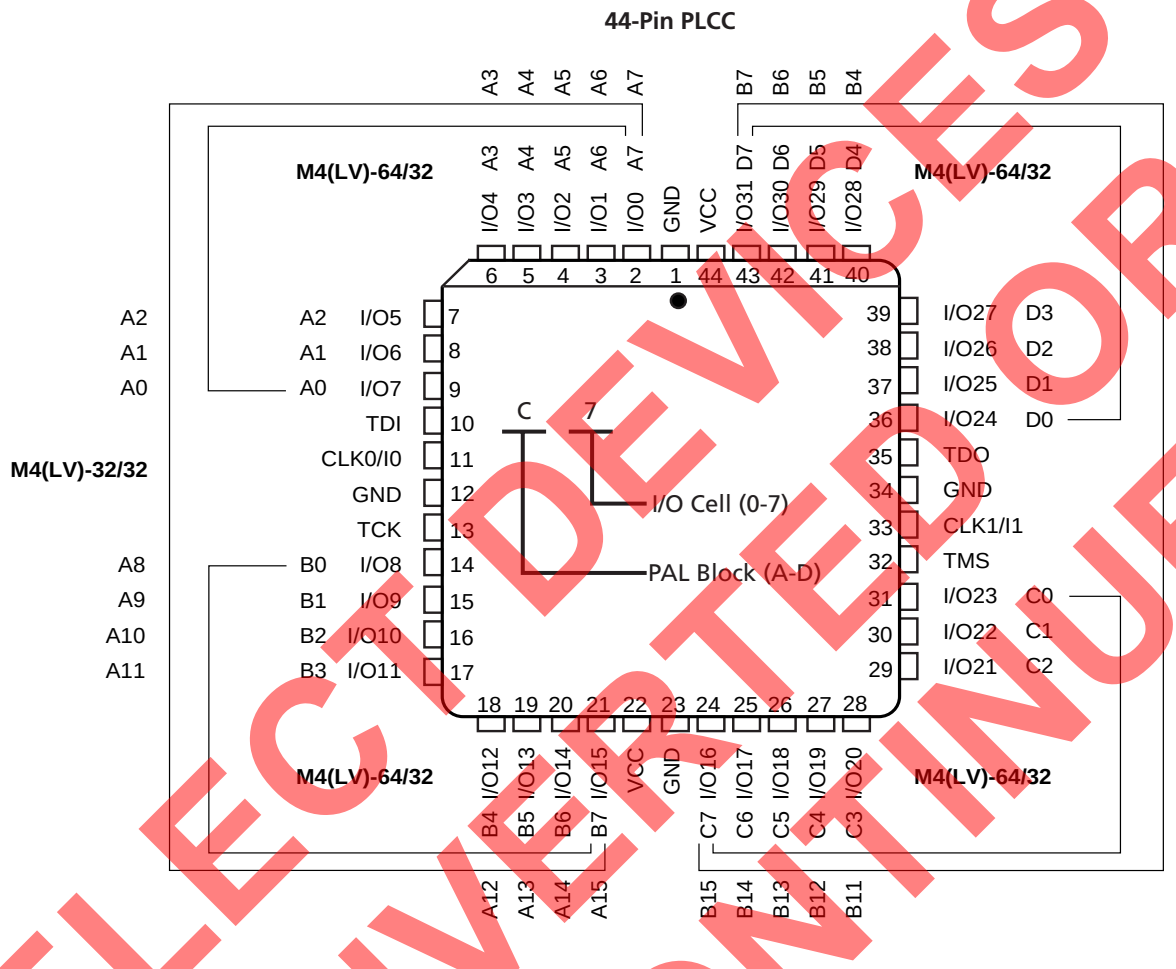


Figure 19. MACH 4 I_{CC} Curves at Low Power Mode

44-PIN PLCC CONNECTION DIAGRAM (M4(LV)-32/32 AND M4(LV)-64/32)

Top View



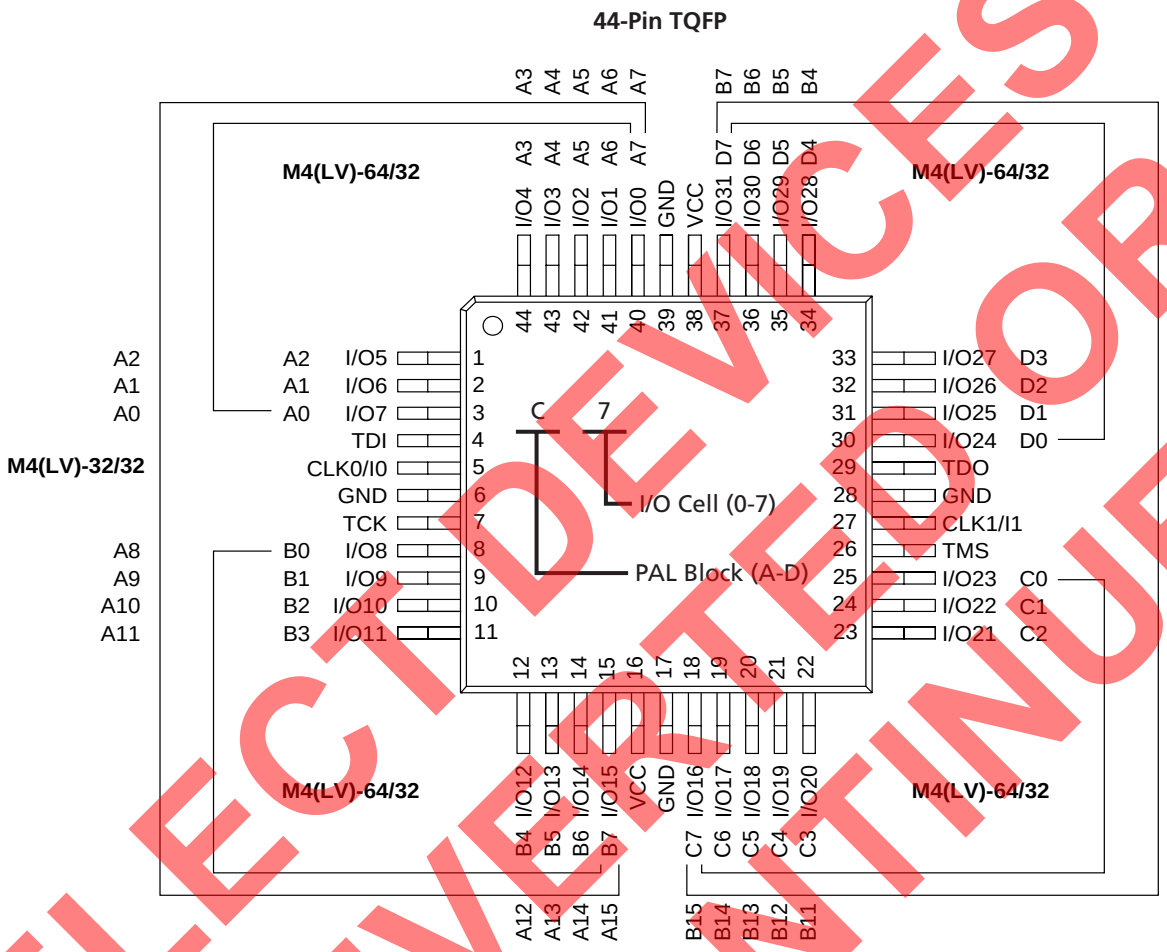
17

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

44-PIN TQFP CONNECTION DIAGRAM (M4(LV)-32/32 AND M4(LV)-64/32)

Top View



PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

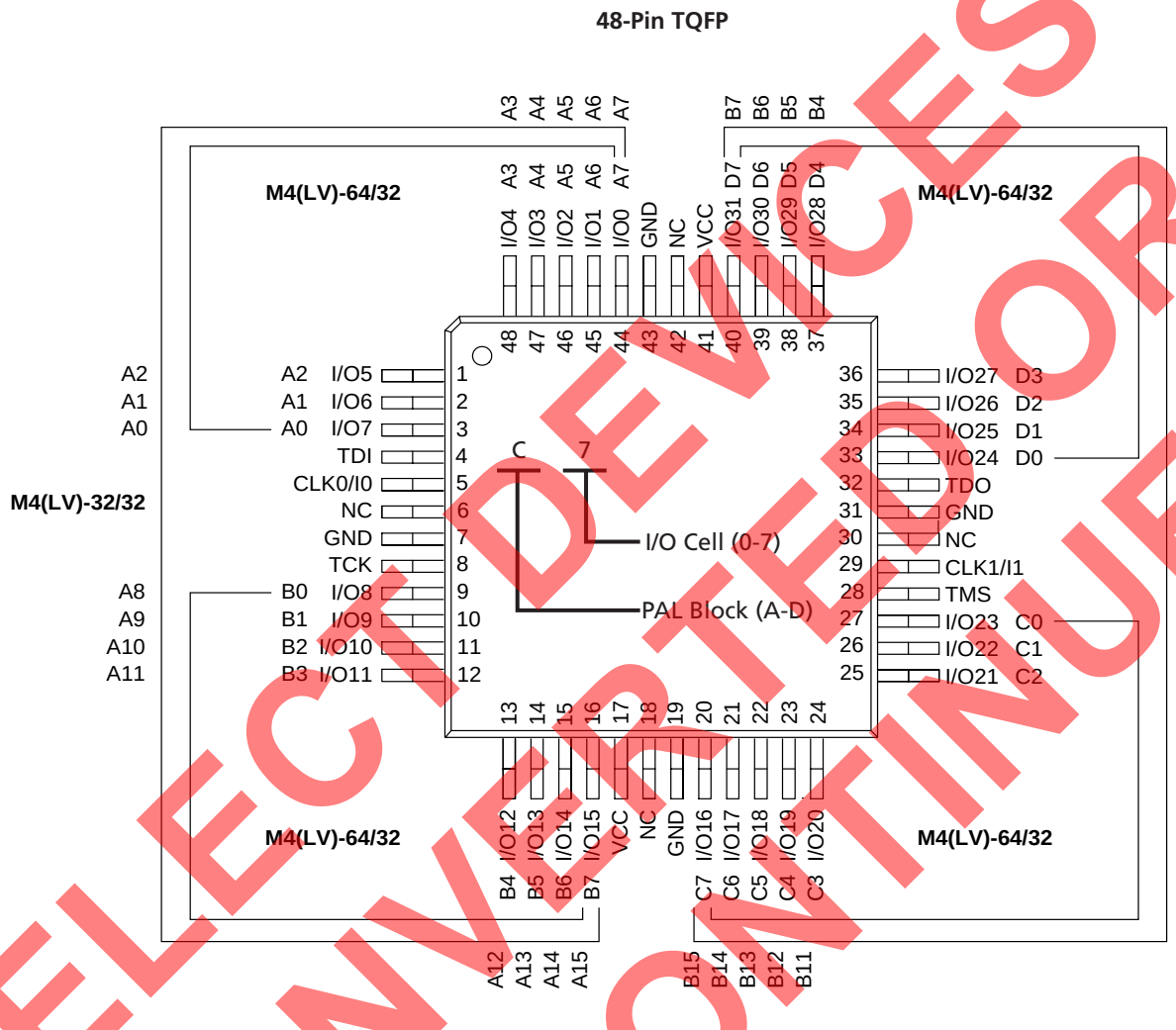
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

48-PIN TQFP CONNECTION DIAGRAM (M4(LV)-32/32 AND M4(LV)-64/32)

Top View



17

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

NC = No Connect

TDI = Test Data In

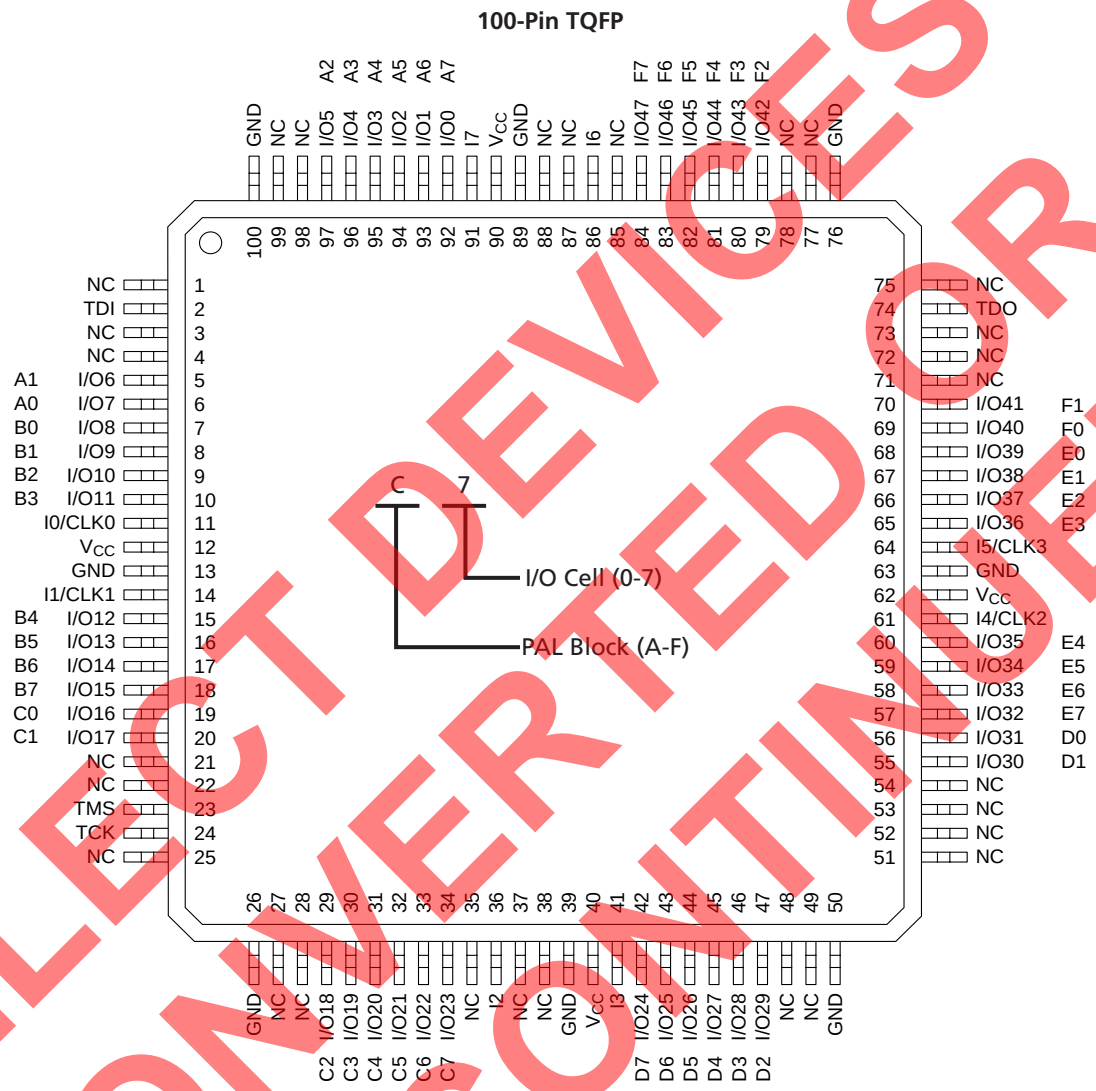
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

100-PIN TQFP CONNECTION DIAGRAM (M4(LV)-96/48)

Top View



PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

NC = No Connect

TDI = Test Data In

TCK = Test Clock

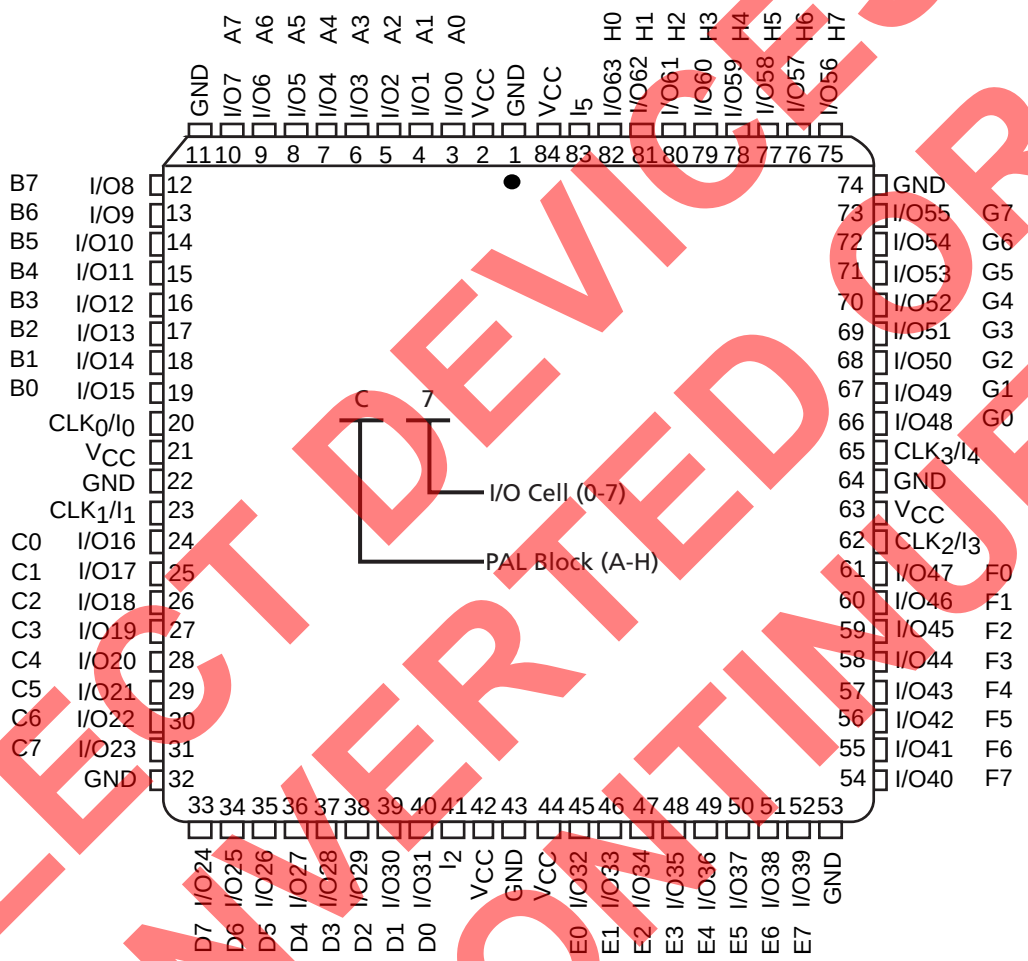
TMS = Test Mode Select

TDO = Test Data Out

84-PIN PLCC CONNECTION DIAGRAM (M4(LV)-128N/64)

Top View

84-Pin PLCC



17

Note:
Pin-compatible with the MACH131, MACH231, MACH435.

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

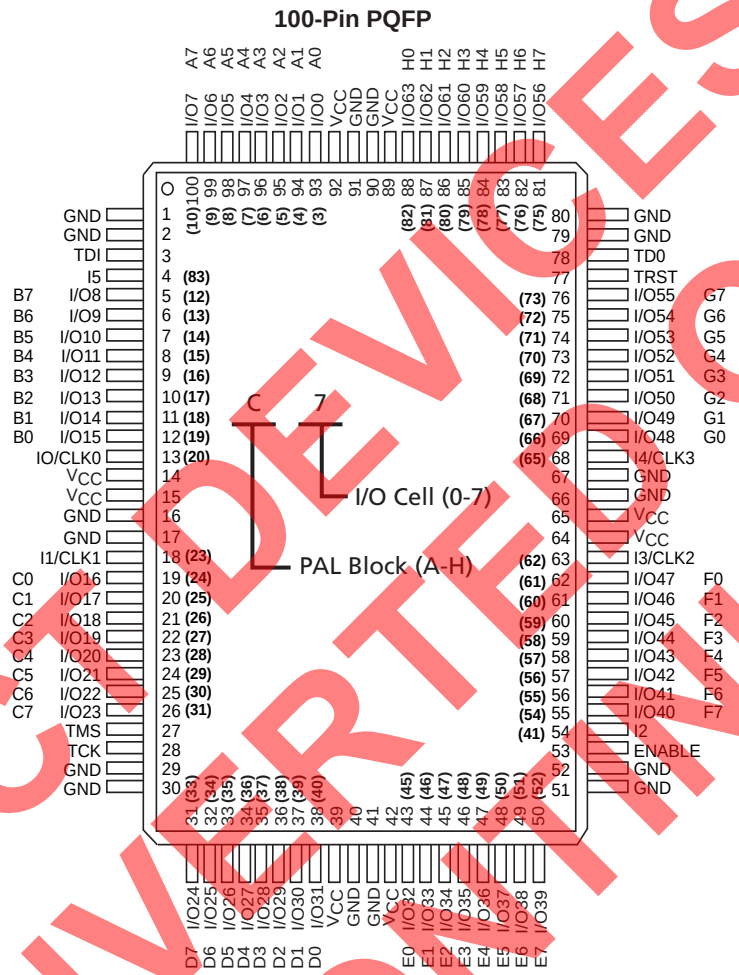
I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

100-PIN PQFP CONNECTION DIAGRAM (M4(LV)-128/64)

Top View



1746

Note:
The numbers in parentheses reflect compatible pin numbers for 84-pin PLCC.

PIN DESIGNATIONS

I/CLK = Input or Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

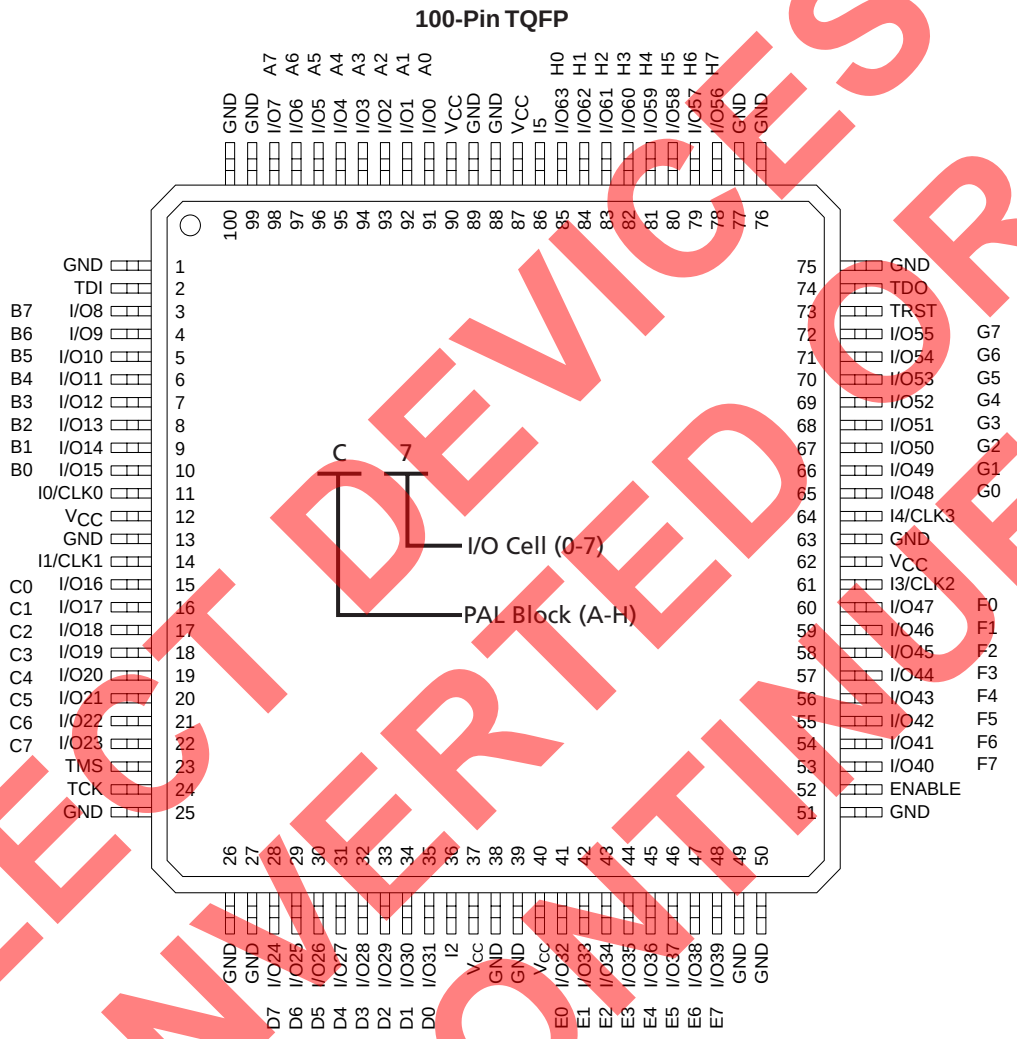
TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

100-PIN TQFP CONNECTION DIAGRAM (M4(LV)-128/64)

Top View



17

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

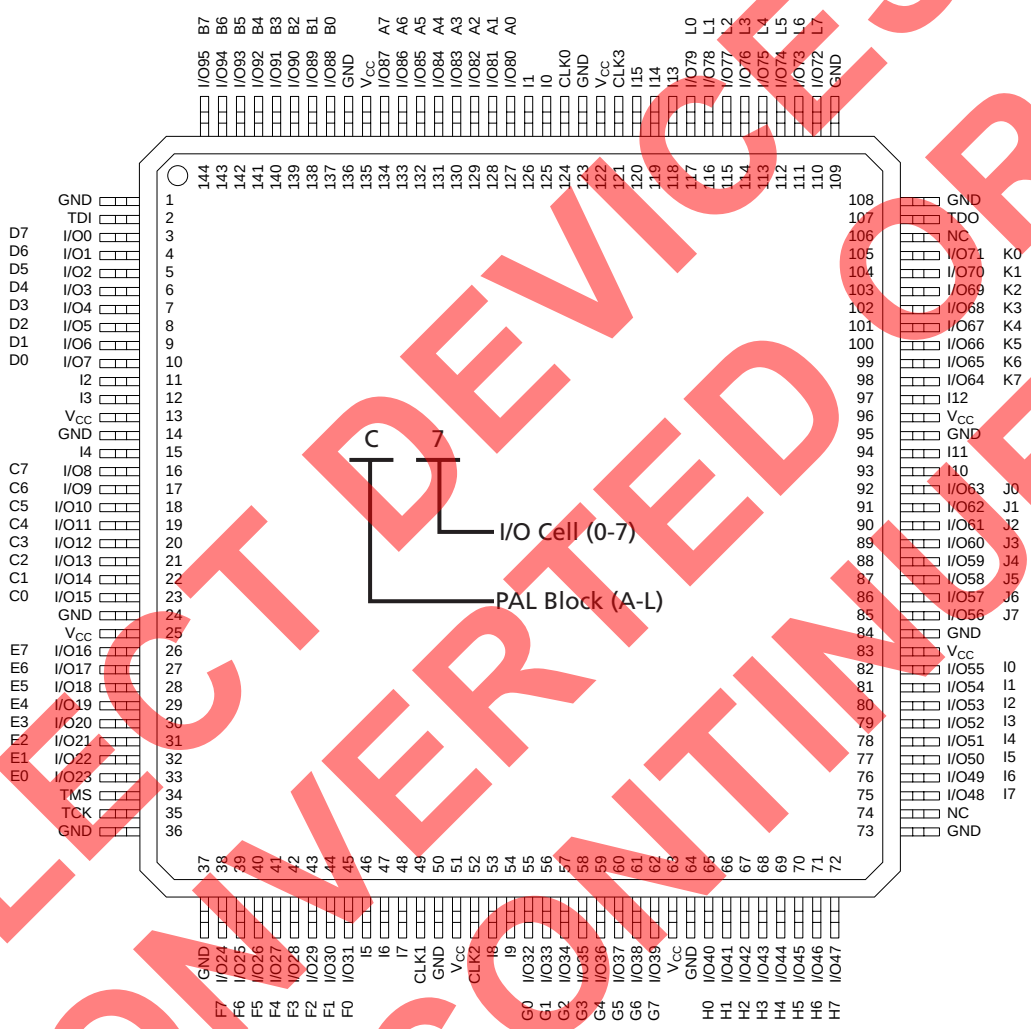
TRST = Test Reset

ENABLE = Program

144-PIN TQFP CONNECTION DIAGRAM (M4(LV)-192/96)

Top View

144-Pin TQFP



PIN DESIGNATIONS

CLK = Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

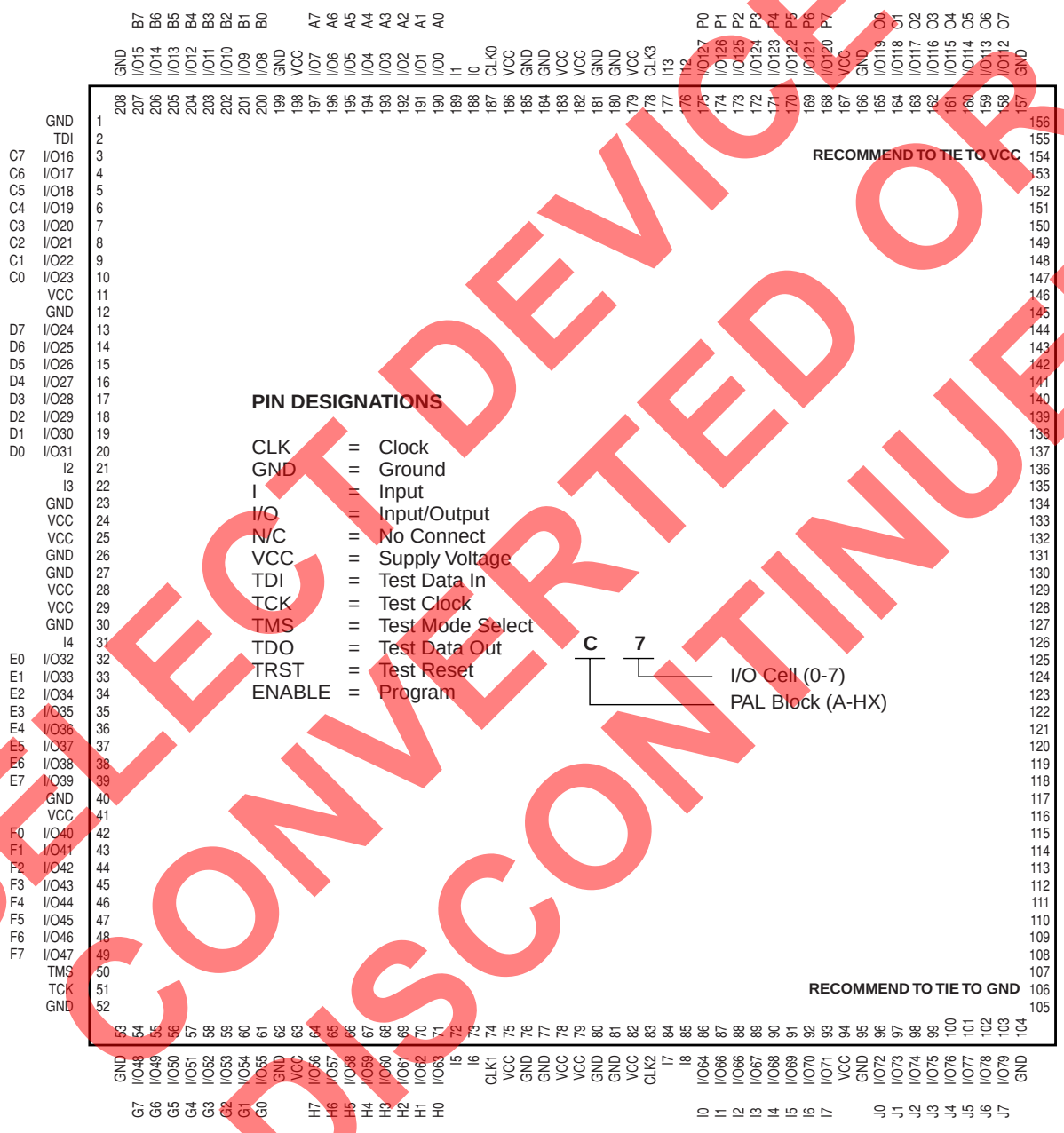
TMS = Test Mode Select

TDO = Test Data Out

208-PIN PQFP CONNECTION DIAGRAM (M4(LV)-256/128)

Top View

208-Pin PQFP



1746

17

256-BALL BGA CONNECTION DIAGRAM (M4LV-256/128)

Bottom View

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2
A	GND	N/C	GND	I/O108 N4	I/O105 N1	GND	I/O100 M4	I/O96 M0	GND	GND	GND	GND	I/O95 L0	I/O91 L4	GND	I/O87 K0	N/C	GND	GND
B	GND	I/O113 O6	N/C	I/O109 N5	I/O106 N2	I/O103 M7	I/O102 M6	I/O98 M2	N/C	I11	N/C	N/C	I/O93 L2	I/O89 L6	I/O88 L7	I/O85 K2	I/O83 K6	I/O82 K5	N/C
C	I/O116 O3	N/C	VCC	TRST	I/O111 N7	I/O107 N3	I/O104 N0	I/O101 M5	I/O97 M1	N/C	I10	I/O94 L1	I/O90 L5	I/O86 K1	I/O84 K3	I/O80 K7	ENABLE	VCC	I/O78 J6
D	I/O120 P7	I/O117 O2	I/O112 O7	VCC	VCC	I/O110 N6	VCC	N/C	I/O99 M3	N/C	I9	I/O92 L3	N/C	VCC	I/O81 K6	VCC	VCC	I/O79 J7	I/O75 J3
E	I/O123 P4	I/O119 O0	I/O114 O5	TDI													TDO	I/O77 J5	I/O72 J0
F	GND	I/O122 P5	I/O118 O1	I/O115 O4													I/O76 J4	I/O73 J1	I/O69 I5
G	I12	I/O125 P2	I/O121 P6	VCC													VCC	I/O70 I6	I/O65 I1
H	GND	I/O127 P0	I/O126 P1	I/O124 P3													I/O67 I3	I/O66 I2	I/O64 I0
J	N/C	N/C	N/C	I13													I7	N/C	N/C
K	GND	CLK3	N/C	N/C													N/C	N/C	CLK2
L	N/C	CLK0	N/C	N/C													N/C	N/C	CLK1
M	N/C	N/C	N/C	I0													I6	N/C	I/O63 H0
N	GND	I/O0 A0	I/O2 A2	I/O3 A3													I/O60 H3	I/O61 H2	I/O59 H4
P	I1	I/O1 A1	I/O6 A6	VCC													VCC	I/O57 H6	I/O58 H5
R	GND	I/O5 A5	I/O9 B1	N/C													I/O51 G4	I/O54 G1	I/O56 H7
T	I/O4 A4	I/O8 B0	I/O12 B4	TCK													TMS	I/O50 G5	I/O55 G0
U	I/O7 A7	I/O11 B3	I/O15 B7	VCC	VCC	I/O18 C5	VCC	I/O24 D7	I/O29 D2	I2	N/C	I/O35 E3	N/C	VCC	N/C	VCC	VCC	I/O48 G7	I/O53 G2
V	I/O10 B2	I/O13 B5	VCC	I/O16 C7	I/O17 C6	I/O21 C2	I/O23 C0	I/O27 D4	I/O31 D0	I3	N/C	I/O33 E1	I/O37 E5	I/O41 F1	I/O43 F3	I/O46 F6	I/O47 F7	VCC	I/O52 G3
W	GND	I/O14 B6	N/C	N/C	I/O19 C4	I/O22 C1	I/O25 D6	I/O28 D3	N/C	N/C	I4	N/C	I/O34 E2	I/O38 E6	I/O39 E7	I/O42 F2	I/O45 F5	N/C	I/O49 G6
Y	GND	GND	GND	N/C	I/O20 C3	GND	I/O26 D5	I/O30 D1	GND	GND	GND	GND	I/O32 E0	I/O36 E4	GND	I/O40 F0	I/O44 F4	GND	N/C
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2

PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
N/C	=	No Connect
VCC	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out
TRST	=	Test Reset
ENABLE	=	Program

C 7
- 7 — I/O Cell (0-7)
- C — PAL Block (A-P)

1746

MACH 4 PRODUCT ORDERING INFORMATION

MACH 4 Devices Commercial & Industrial - 3.3V and 5V

Lattice/Vantis programmable logic products are available with several ordering options. The order number (Va
bination) is formed by a combination of:

M4- 256 / 128 -7 Y C

FAMILY TYPE

M4- = MACH 4 Family (5-V V_{CC})
M4LV- = MACH 4 Family Low Voltage (3.3-V V_{CC})

MACROCELL DENSITY

32	= 32 Macrocells	128N	= 128 Macrocells, Non-ISP
64	= 64 Macrocells	192	= 192 Macrocells
96	= 96 Macrocells	256	= 256 Macrocells
128	= 128 Macrocells		

I/Os

/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP
/48 = 48 I/Os in 100-pin TQFP
/64 = 64 I/Os in 84-pin PLCC, 100-pin PQFP or 100-pin TQFP
/96 = 96 I/Os in 144-pin TQFP
/128 = 128 I/Os in 208-pin PQFP or 256-ball BGA

48 = 48-pin TQFP for M4(L
or M4(LV)-64/32

OPERATING CONDITIONS

C = Commercial (0°C to +
I = Industrial (-40°C to +

PACKAGE TYPE

A = Ball Grid Array (BGA
J = Plastic Leaded Chip C
(PLCC)
V = Thin Quad Flat Pack
Y = Plastic Quad Flat Pac

SPEED

-7 = 7.5 ns t_{PD}
-10 = 10 ns t_{PD}
-12 = 12 ns t_{PD}
-14 = 14 ns t_{PD}
-15 = 15 ns t_{PD}
-18 = 18 ns t_{PD}

Valid Combinations		
M4-32/32	-7, -10, -12, -15	JC, VC, VC48
M4LV-32/32		JC, VC, VC48
M4-64/32		JC, VC, VC48
M4LV-64/32		JC, VC, VC48
M4-96/48		VC
M4LV-96/48		VC
M4-128/64		YC, VC
M4LV-128/64		YC, VC
M4-128N/64		JC
M4LV-128N/64		JC
M4-192/96		VC
M4LV-192/96		VC
M4-256/128		YC
M4LV-256/128		YC, AC

All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4-256/128-7YC-10YI

Valid Combinations		
M4-32/32	-10, -12, -14, -18	JI, VI, V
M4LV-32/32		JI, VI, V
M4-64/32		JI, VI, V
M4LV-64/32		JI, VI, V
M4-96/48		VI
M4LV-96/48		VI
M4-128/64		YI, VI
M4LV-128/64		YI, VI
M4-128N/64		JI
M4LV-128N/64		JI
M4-192/96		VI
M4LV-192/96		VI
M4-256/128		YI
M4LV-256/128		YI, AI

Valid Combinations

Valid Combinations list configurations plann
supported in volume for this device. Consult
Lattice sales office to confirm availability of spe
combinations and to check on newly r
combinations.