Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max	V_{CC} = VG	42	V
Charge pump output voltage	VG max	VG pin	42	V
Output current	I_O max1	Pins UL, VL, WL	-15 to 15	mA
	I_O max2	Pins UH, VH, WH, UOUT, VOUT and WOUT	-15 to 15	mA
Allowable power dissipation	Pd max1	Independent IC	0.65	W
	Pd max2	Mounted on the specified board *	1.70	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified board:114.3mm × 76.1mm × 1.6mm, glass epoxy board.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{CC}		16 to 28	V
5V constant voltage output current	I_{REG}		0 to -10	mA
LD pin applied voltage	V_{LD}		0 to 6	V
LD pin output current	I_{LD}		0 to 5	mA
FGS pin applied voltage	V_{FGS}		0 to 6	V
FGS pin output current	I_{FGS}		0 to 5	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	$I_{CC}1$			6.5	8.2	mA
Supply current 2	$I_{CC}2$	At stop		3	3.8	mA
5V Constant-voltage Output (VREG pin)						
Output voltage	VREG	I_O = 5mA	5.2	5.6	6.0	V
Line regulation	ΔV (REG1)	V_{CC} = 16 to 28V		10	50	mV
Load regulation	ΔV (REG2)	I_O = -5 to -10mA		10	50	mV
Output block / Conditions : apply a VG voltage of 33V						
High level output voltage 1	$V_{OH}1$	Pins UL, VL and WL I_{OH} = -2mA	VREG-0.48	VREG-0.35	VREG-0.22	V
Low level output voltage 1	$V_{OL}1$	Pins UL, VL and WL I_{OL} = 2mA	0.19	0.30	0.41	V
High level output voltage 2	$V_{OH}2$	Pins UH, VH and WH I_{OH} = -2mA	VG-0.65	VG-0.5	VG-0.35	V
Low level output voltage 2	$V_{OL}2$	Pins UH, VH and WH I_{OL} = 2mA	0.45	0.6	0.8	V
PWM frequency	f (PWM)		16	20	24	kHz
Internal Oscillator						
Oscillation frequency	f (REF)		1.79	2.24	2.69	MHz
Charge Pump Output (VG pin)						
Output voltage	VGOUT		V_{CC}+7.9	V_{CC}+9.0	V_{CC}+10.0	V
CP1 pin						
High level output voltage	V_{OH} (CP1)	ICP1 = -2mA	V_{CC}-1.45	V_{CC}-1.1	V_{CC}-0.8	V
Low level output voltage	V_{OL} (CP1)	ICP1 = 2mA	0.5	0.65	0.8	V
Charge pump frequency	f (CP1)		112	140	168	kHz
Hall Amplifier						
Input bias current	I_B (HA)		-2	-0.1		μA
Common-mode input voltage range 1	VICM1	When using Hall elements	0.3		3.5	V
Common-mode input voltage range 2	VICM2	At one-side input bias (Hall IC application)	0		VREG	V
Hall input sensitivity		SIN wave	50			mVp-p
Hysteresis width	ΔV_{IN} (HA)		5	13	24	mV
Input voltage Low → High	VSLH		2	7	12	mV
Input voltage High → Low	VSHL		-12	-6	-2	mV

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
FG Amplifier						
Input offset voltage	V_{IO} (FG)		-10		10	mV
Input bias current	IB (FG)		-1		1	µA
Reference voltage	VB (FG)		-5%	VREG/2	5%	V
High level output voltage	V_{OH} (FG)	IFGI = -0.1mA, No load	3.95	4.4	4.85	V
Low level output voltage	V_{OL} (FG)	IFGI = 0.1mA, No load	0.75	1.2	1.65	V
FG input sensitivity		GAIN : 100 times	3			mV
Schmitt width of the next stage		One-side hysteresis comparator	120	200	280	mV
Operation frequency range					3	kHz
Open-loop gain		f_{FG} = 2kHz	45	48		dB
FGS output						
Output saturation voltage	V_{OL} (FGS)	I_{FGS} = 2mA		0.2	0.4	V
Output leakage current	IL (FGS)	V_O = 6V			10	µA
CSD oscillator						
High level output voltage	V_{OH} (CSD)		2.9	3.4	3.9	V
Low level output voltage	V_{OL} (CSD)		1.6	2.0	2.4	V
Amplitude	V (CSD)		1.15	1.4	1.65	Vp-p
External capacitor charge current	ICHG1		-13	-10	-7	µA
External capacitor discharge current	ICHG2		7.5	10.5	13.5	µA
Oscillation frequency	f (CSD)	C = 0.047µF		78		Hz
Speed Discriminator output						
High level output voltage	V_{OH} (D)		VREG-1.25	VREG-1.0	VREG-0.75	V
Low level output voltage	V_{OL} (D)		0.65	0.9	1.15	V
Counts				512		
LD output						
Output saturation voltage	V_{OL} (LD)	I_{LD} = 2mA		0.2	0.4	V
Output leakage current	I_L (LD)	V_O = 6V			10	µA
Lock range			-6.25		+6.25	%
Speed control PLL output						
High level output voltage	V_{OH} (P)		VREG-2.0	VREG-1.7	VREG-1.4	V
Low level output voltage	V_{OL} (P)		1.3	1.6	1.9	V
Current control circuit						
Drive gain	GDF		0.20	0.25	0.32	
Current limiter operation						
Limiter voltage	VRF		0.225	0.25	0.27	V
Integrator						
Input offset voltage	V_{IO} (INT)		-10		10	mV
Input bias current	I_B (INT)		-1		1	µA
Reference voltage	V_B (INT)		-5%	VREG/2	5%	V
High level output voltage	V_{OH} (INT)	I_{INT}I = -0.1mA, No load	3.95	4.4	4.85	V
Low level output voltage	V_{OL} (INT)	I_{INT}I = 0.1mA, No load	0.75	1.2	1.65	V
Open-loop gain		f_{INT} = 2kHz	45	48		dB
VCO Oscillator (C pin)						
Oscillation frequency range	f (C)	C = 120pF, R = 24kΩ	0.15		1.54	MHz
High level output voltage	V_{OH} (C)	FIL = 2.5V	2.71	3.16	3.61	V
Low level output voltage	V_{OL} (C)	FIL = 2.5V	2.20	2.60	3.00	V
Amplitude	V (C)	FIL = 2.5V	0.44	0.56	0.68	Vp-p
FIL pin						
Output source current	I_{OH} (FIL)		-15	-11	-6	µA
Output sink current	I_{OL} (FIL)		6	10	15	µA

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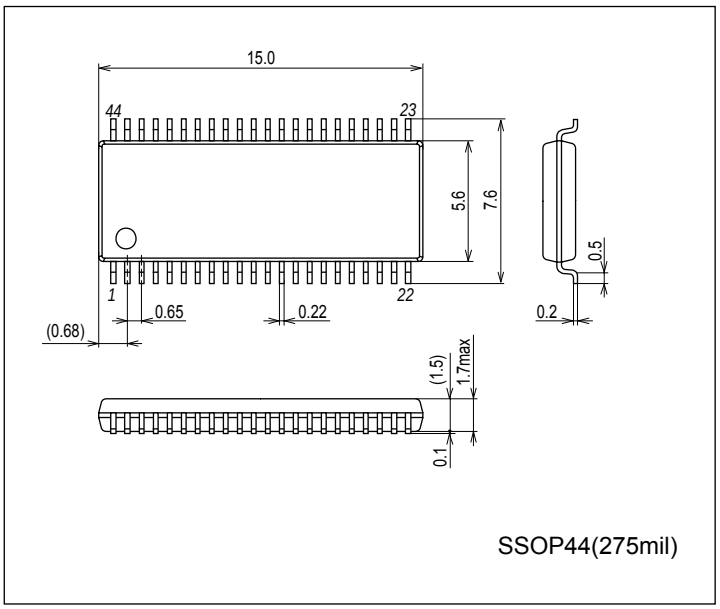
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Low-voltage protection circuit						
Operation voltage	VLVSD		10.0	10.7	11.4	V
Hysteresis width	ΔVLVSD		0.72	0.97	1.22	V
Thermal shutdown operation						
Thermal shutdown operation temperature	TSD	Design target value*	150	175		°C
Hysteresis width	ΔTSD	Design target value*		30		°C
CLK pin						
Input frequency	fl (CLK)				3	kHz
High level input voltage range	V_{IH} (CLK)		2.0		VREG	V
Low level input voltage range	V_{IL} (CLK)		0		1.0	V
Input open voltage	V_{IO} (CLK)		VREG-0.5		VREG	V
Hysteresis width	V_{IS} (CLK)	Design target value*	0.18	0.27	0.36	V
High level input current	I_{IH} (CLK)	VCLK = 5V	-22	-10	-3	μA
Low level input current	I_{IL} (CLK)	VCLK = 0V	-133	-93	-70	μA
Pull-up resistance	RU (CLK)		45	60	75	kΩ
S/S pin						
High level input voltage range	V_{IH} (S/S)		2.0		VREG	V
Low level input voltage range	V_{IL} (S/S)		0		1.0	V
Input open voltage	V_{IO} (S/S)		VREG-0.5		VREG	V
Hysteresis width	V_{IS} (S/S)		0.18	0.27	0.36	V
High level input current	I_{IH} (S/S)	VS/S = 5V	-22	-10	-3	μA
Low level input current	I_{IL} (S/S)	VS/S = 0V	-133	-93	-70	μA
Pull-up resistance	RU (S/S)		45	60	75	kΩ
F/R pin						
High level input voltage range	V_{IH} (F/R)		2.0		VREG	V
Low level input voltage range	V_{IL} (F/R)		0		1.0	V
Input open voltage	V_{IO} (F/R)		VREG-0.5		VREG	V
Hysteresis width	V_{IS} (F/R)		0.18	0.27	0.36	V
High level input current	I_{IH} (F/R)	VF/R = 5V	-22	-10	-3	μA
Low level input current	I_{IL} (F/R)	VF/R = 0V	-133	-93	-70	μA
Pull-up resistance	RU (F/R)		45	60	75	kΩ
BR pin						
High level input voltage range	V_{IH} (BR)		2.0		VREG	V
Low level input voltage range	V_{IL} (BR)		0		1.0	V
Input open voltage	V_{IO} (BR)		VREG-0.5		VREG	V
Hysteresis width	V_{IS} (BR)		0.18	0.27	0.36	V
High level input current	I_{IH} (BR)	VBR = 5V	-22	-10	-3	μA
Low level input current	I_{IL} (BR)	VBR = 0V	-133	-93	-70	μA
Pull-up resistance	RU (BR)		45	60	75	kΩ

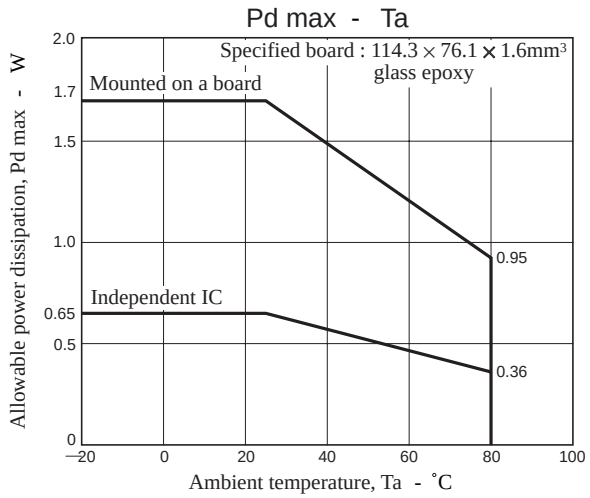
Note : * These items are design target values and are not tested.

Package Dimensions

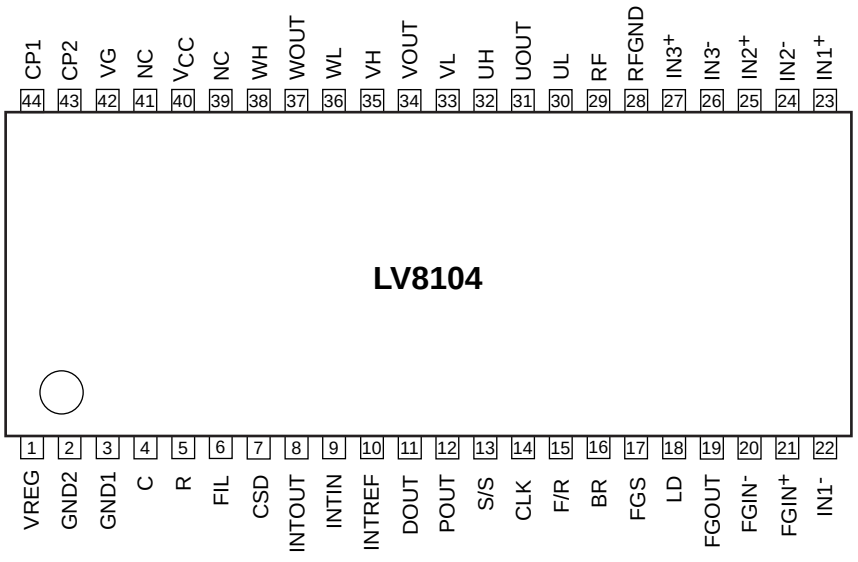
unit : mm (typ)

3277





Pin Assignment



Three-phase logic truth table (A high level input is the state where $IN^+ > IN^-$.)

	F/R = "L"			F/R = "H"			Drive output	
	IN1	IN2	IN3	IN1	IN2	IN3	Upper gate	Lower gate
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

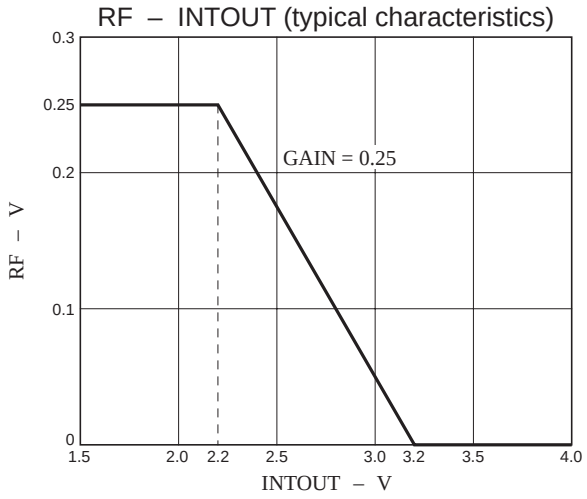
S/S Input

Input	Mode
High or Open	Stop
Low	Start

BR Input

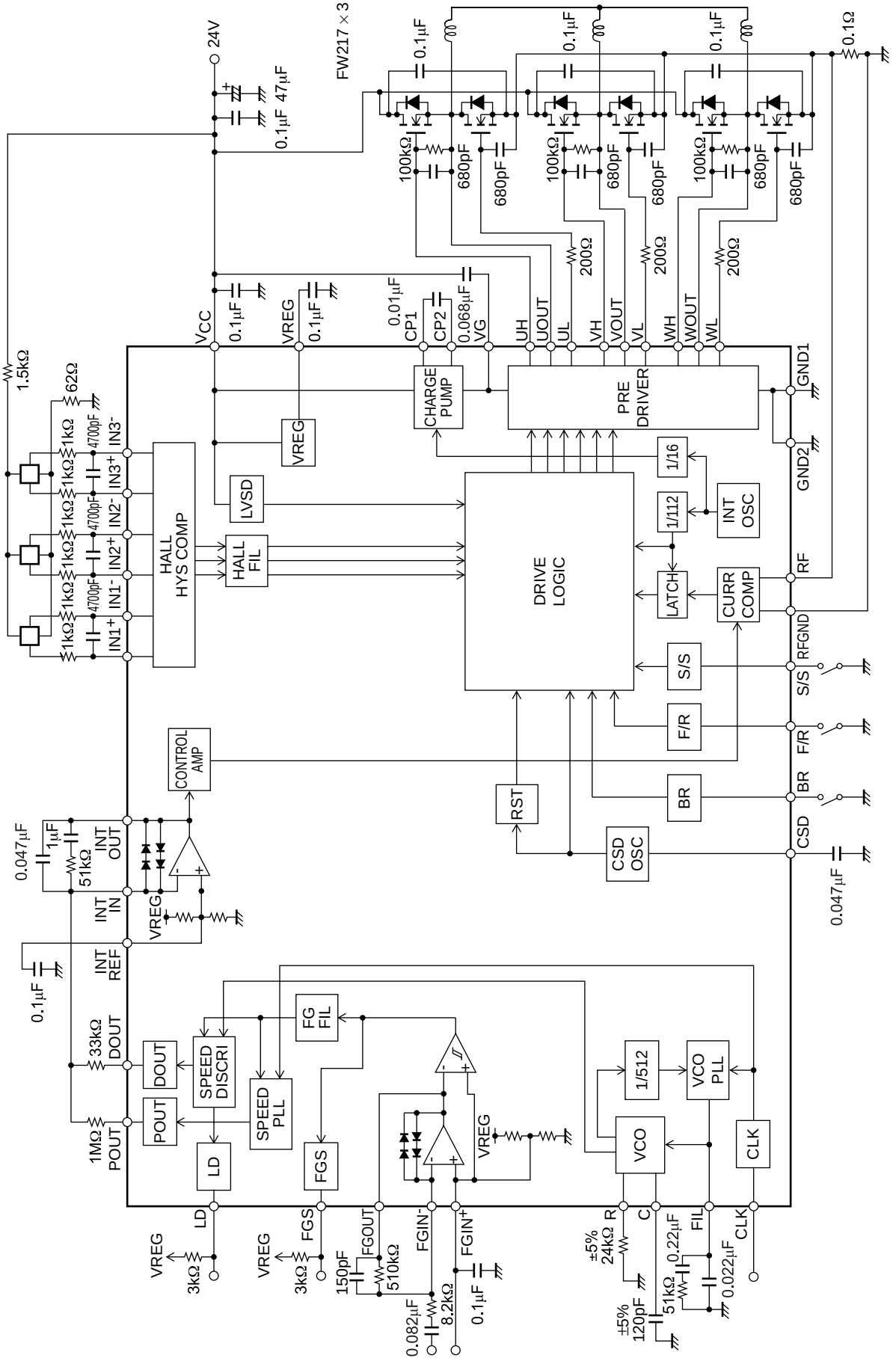
Input	Mode
High or Open	Brake
Low	Release

Current Control Characteristics



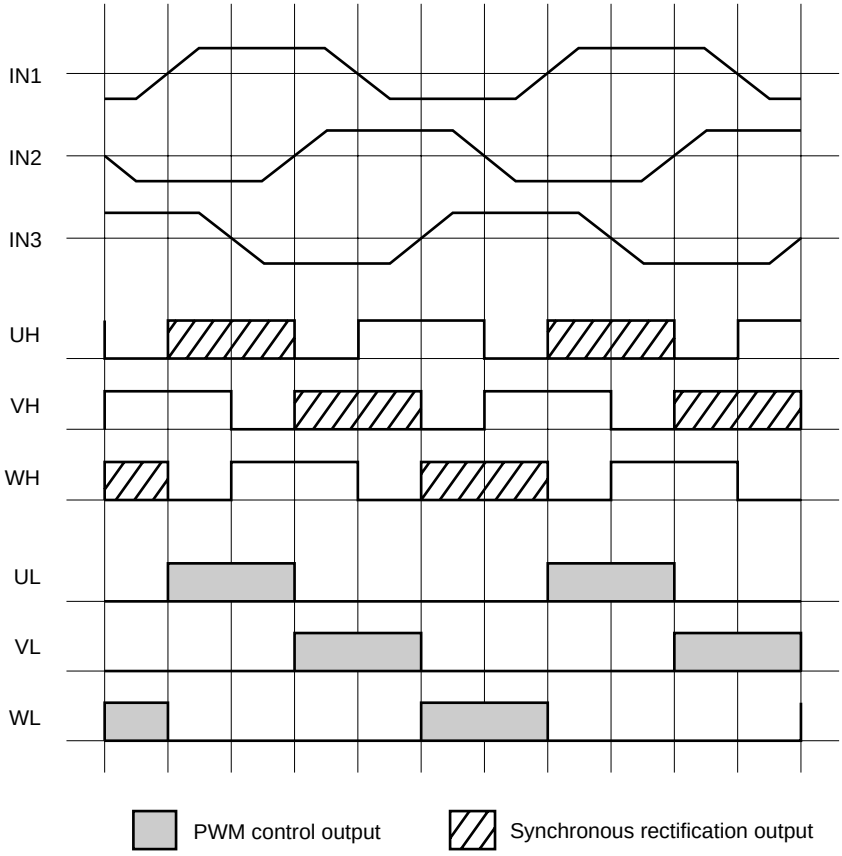
Block Diagram

(Referance constants)

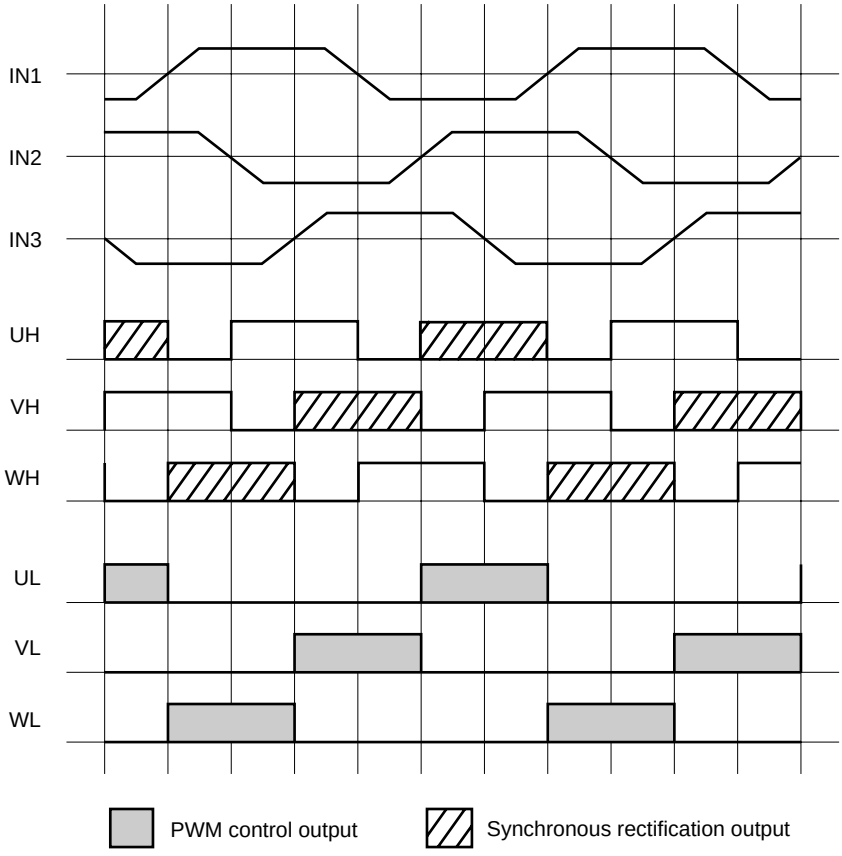


Relations Hall input with Drive output

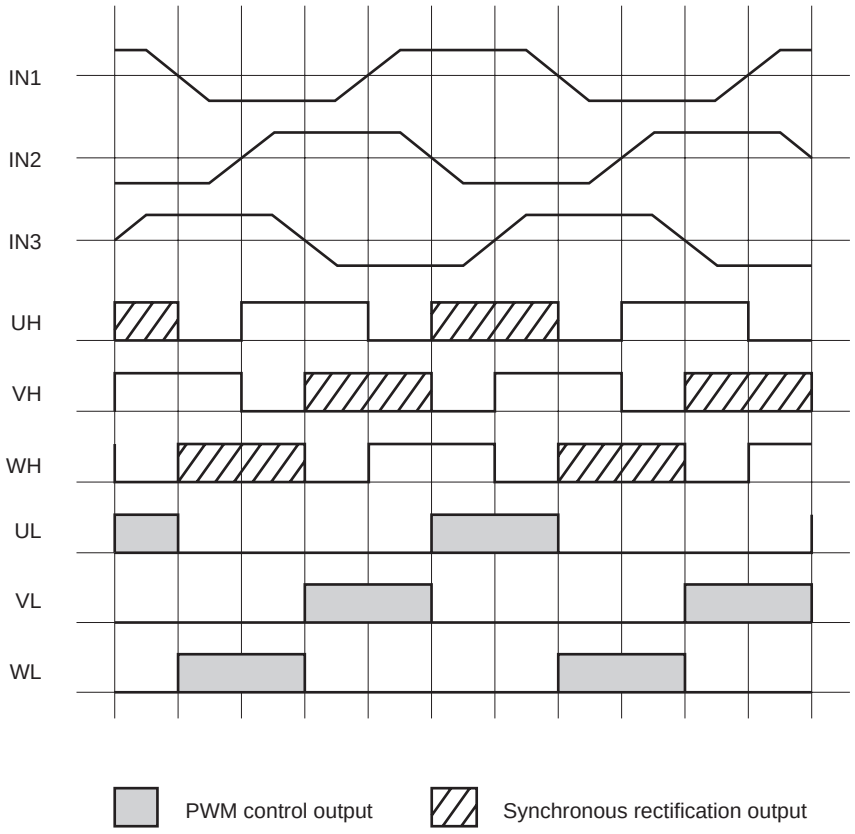
(1) When F/R = ”L”



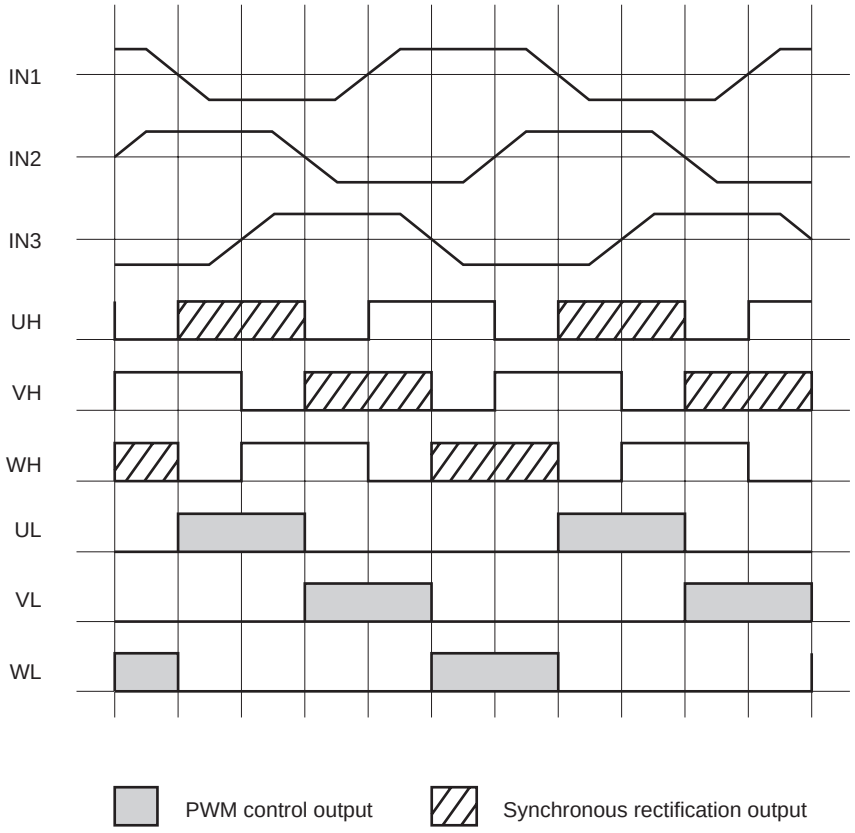
(2) When F/R = ”H”



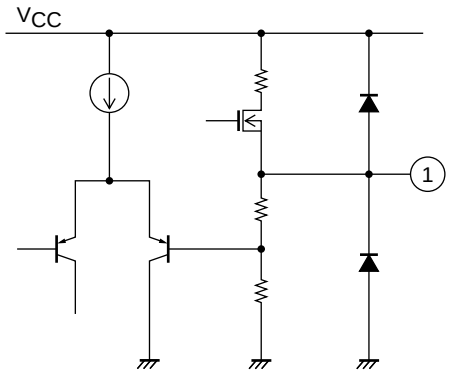
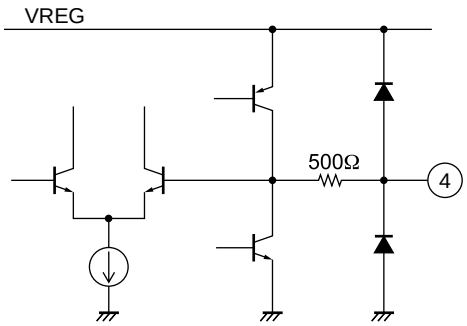
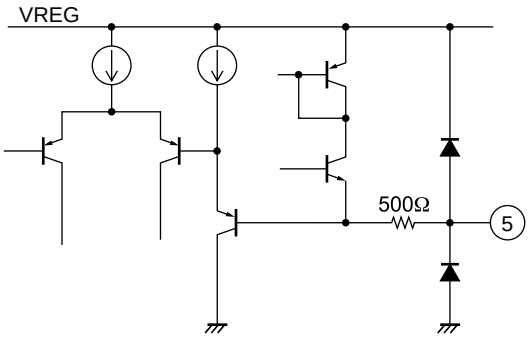
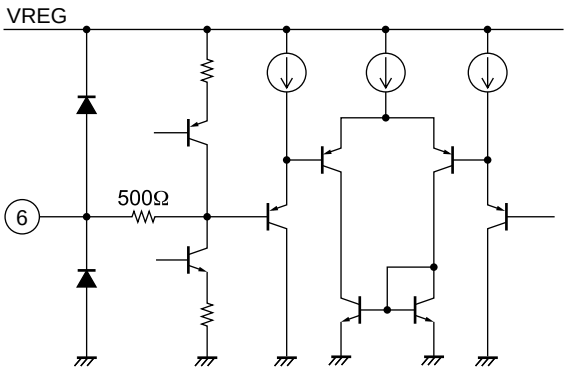
(3) When F/R = ”L” and the inverting phase input as against Hall input(2).



(4) When F/R=”H” and the inverting phase input as against Hall input(1).



Pin Functions

Pin No.	Pin name	Pin function	Equivalent circuit
1	VREG	5V constant voltage output pin(5.6V). Connect a capacitor between this pin and GND.	
2 3	GND2 GND1	GND pins. GND1 and GND2 are connected in the IC.	
4	C	VCO oscillation pin. Connect a capacitor between this pin and GND.	
5	R	Pin to set the charge / discharge current of the VCO circuit. Connect a resistor between this pin and GND.	
6	FIL	VCO PLL output filter pin.	

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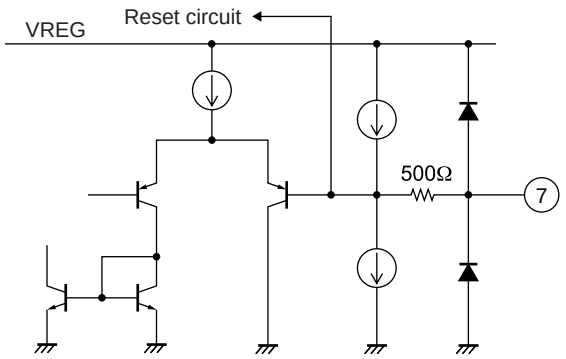
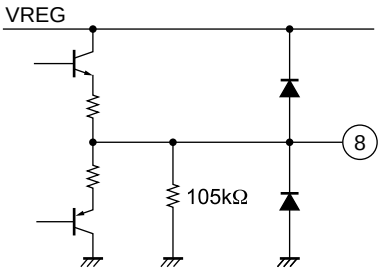
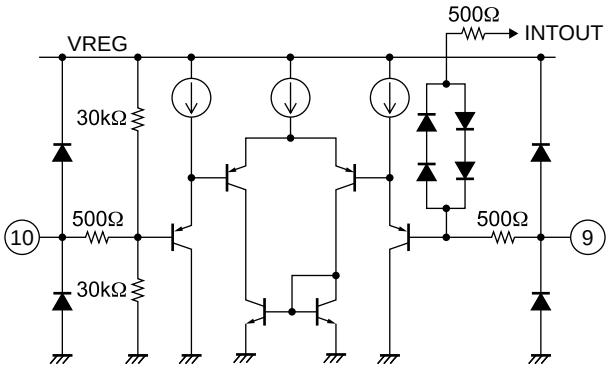
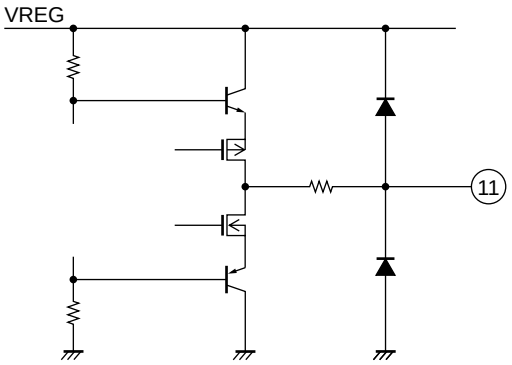
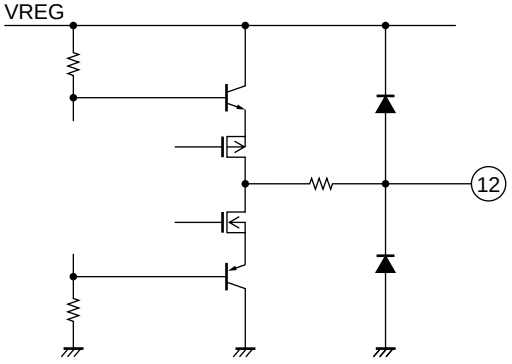
Pin No.	Pin name	Pin function	Equivalent circuit
7	CSD	Pin to set the operating time of the constraint protection. Connect a capacitor between this pin and GND. This pin combines also functions as the logic circuit block initial reset pin.	
8	INTOUT	Integrating amplifier output pin.	
9	INTIN	Integrating amplifier inverting input pin.	
10	INTREF	Integrating amplifier non-inverting input pin. 1/2 VREG potential. Connect a capacitor between this pin and GND.	
11	DOUT	Speed discriminator output pin. Acceleration → high, deceleration → low.	
12	POUT	Speed control PLL output pin. Outputs the phase comparison result for CLK and FG.	

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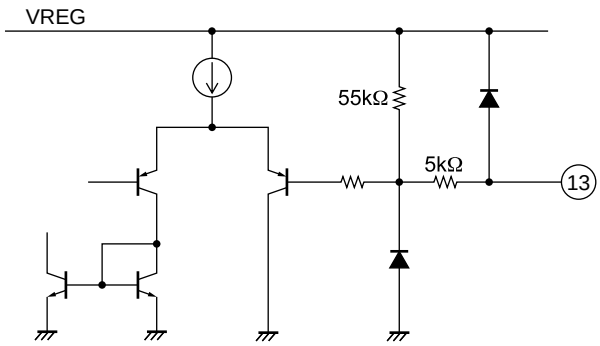
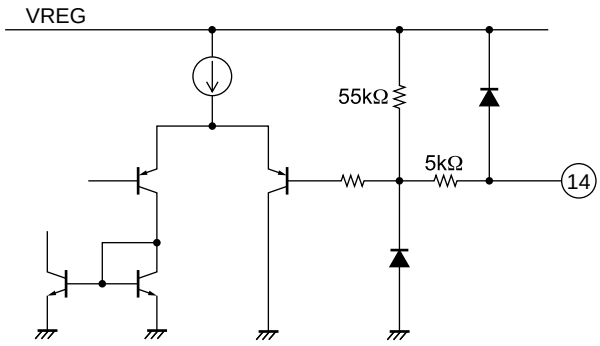
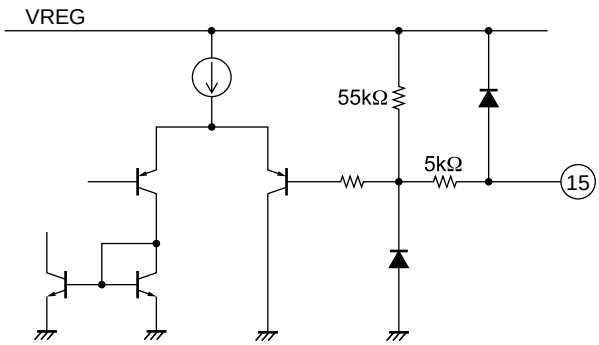
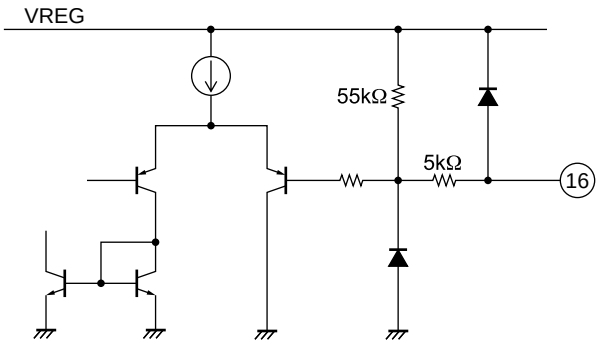
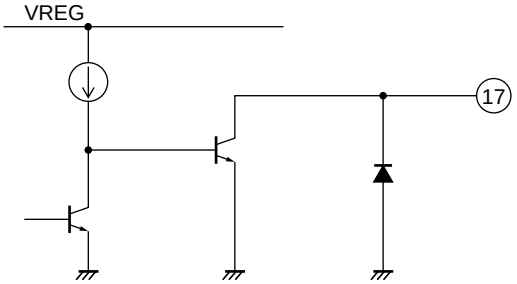
Pin No.	Pin name	Pin function	Equivalent circuit
13	S/S	Start / Stop control pin. Low : 0V to 1.0V High : 2.0V to VREG Goes high when left open. Low for start. The hysteresis width is about 0.27V.	
14	CLK	External clock signal input pin. Low : 0V to 1.0V High : 2.0V to VREG Goes high when left open. The hysteresis width is about 0.27V. f = 3kHz, maximum.	
15	F/R	Forward / reverse control pin. Low : 0V to 1.0V High : 2.0V to VREG Goes high when left open. Low for forward. The hysteresis width is about 0.27V.	
16	BR	Brake pin(short braking operation). Low : 0V to 1.0V High : 2.0V to VREG Goes high when left open. High or open for brake mode operation. The hysteresis width is about 0.27V.	
17	FGS	FG amplifier Schmitt output pin. This is an open collector output.	

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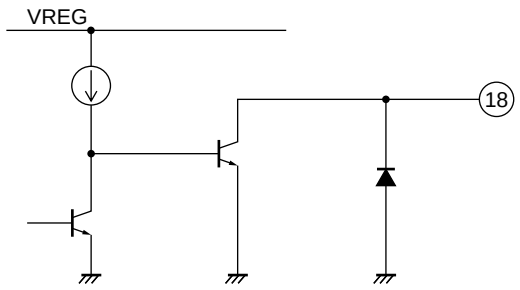
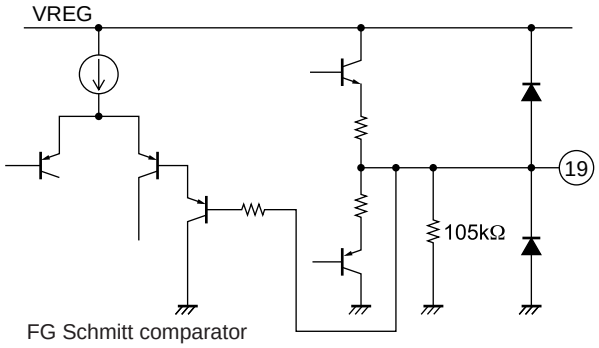
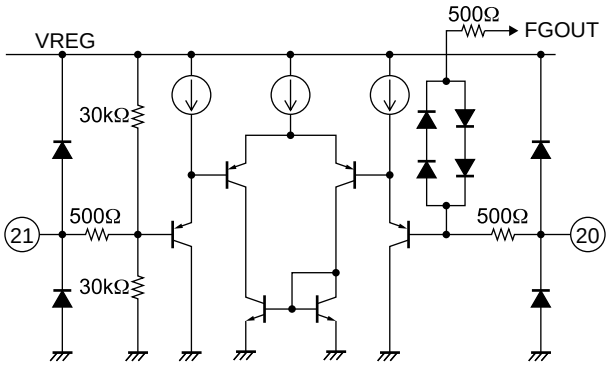
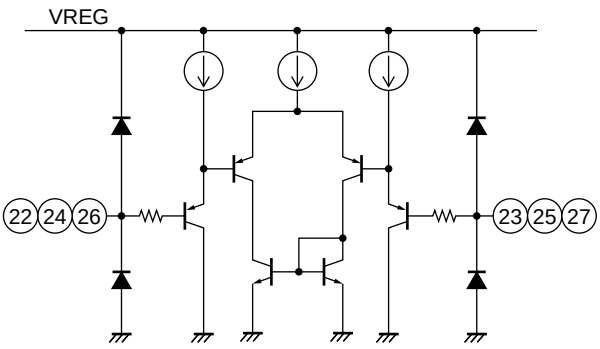
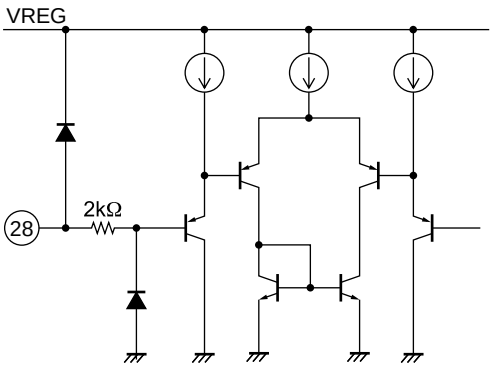
Pin No.	Pin name	Pin function	Equivalent circuit
18	LD	Speed lock detection output pin. This is an open collector output. Goes low when the motor speed is within the speed lock range(±6.25%)	
19	FGOUT	FG amplifier output pin. This pin is connected to the FG Schmitt comparator circuit internally in the IC.	
20	FGIN⁻	FG amplifier inverting input pin.	
21	FGIN⁺	FG amplifier non-inverting input pin. 1/2 VREG potential. Connect a capacitor between this pin and GND.	
22 23 24 25 26 27	IN1⁻ IN1⁺ IN2⁻ IN2⁺ IN3⁻ IN3⁺	Hall input pins. The input is seen as a high level input when IN⁺ > IN⁻, and as a low level input for the opposite state. If noise on the Hall signals is a problem, insert capacitors between the corresponding IN⁺ and IN⁻ inputs.	
28	RFGND	Output current detection reference pin. Connect to GND side of the current detection resistor Rf.	

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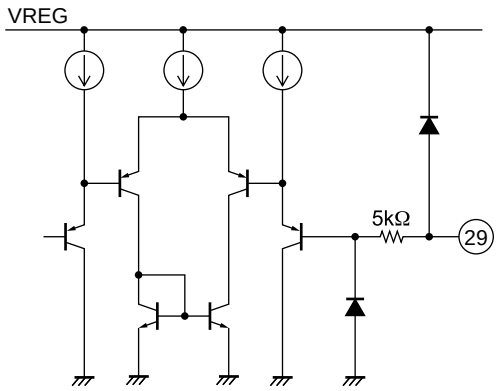
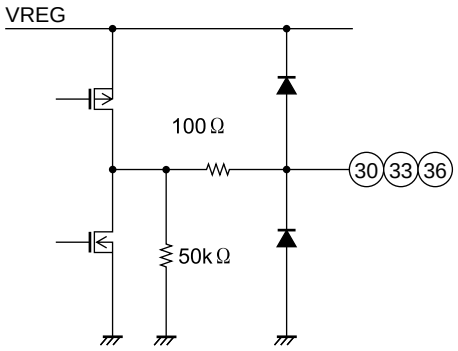
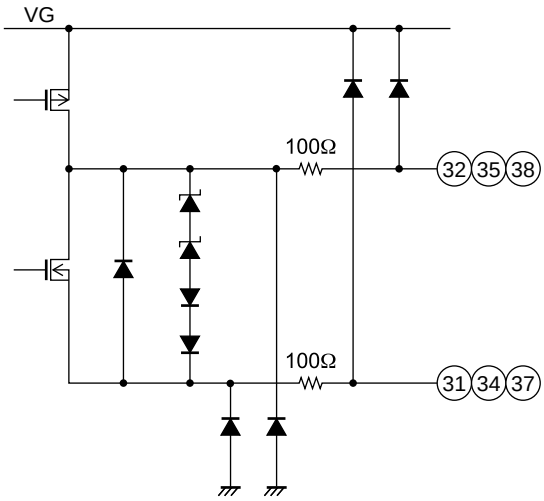
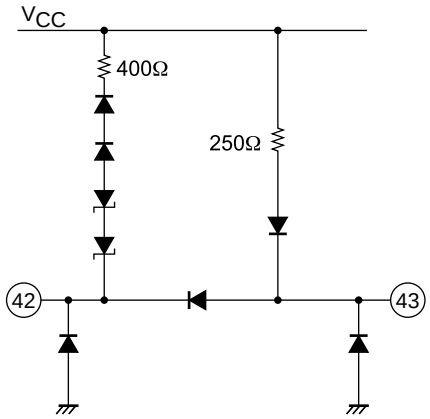
Pin No.	Pin name	Pin function	Equivalent circuit
29	RF	Output current detection pin. Connect to the current detection resistor Rf. Sets the the maximum output current IOUT to be 0.25/Rf.	
30 33 36	UL VL WL	Output pins for gate drive of the lower side N channel power FET.	
32 35 38	UH VH WH	Output pins for gate drive of the upper side N channel power FET.	
31 34 37	UOUT VOUT WOUT	Pins to detect the source voltage of the upper side N channel power FET.	
40	V_{CC}	Power supply pin. Connect a capacitor between this pin and GND for stabilization.	
42	VG	Charge pump output pin. Connect a capacitor between this pin and V_{CC}.	
43	CP2	Pin to connect the capacitor for charge pump. Connect a capacitor between this pin and CP1.	

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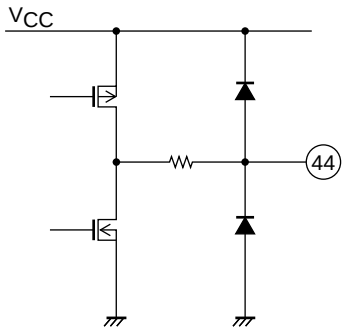
Pin No.	Pin name	Pin function	Equivalent circuit
44	CP1	Pin to connect the capacitor for charge pump. Connect a capacitor between this pin and CP2.	
39 41	NC	No connection pins.	

Description of LV8104V

1. Speed control circuit

This IC controls the speed with a combination of the speed discriminator circuit and the PLL circuit. Therefore, when a motor that has large load variation is used, it is possible to prevent the rotation variation as compared with the speed control method only the speed discriminator. The speed discriminator circuit and the PLL circuit outputs an error signal once every one FG period. The FG servo frequency signal (f_{FG}) is controlled to have the equal frequency with the clock signal (f_{CLK}) which is input through the CLK pin.

$$f_{FG} = f_{CLK}$$

2. VCO circuit

This IC has the VCO circuit to generate the reference signal of the speed discriminator circuit. The reference signal frequency is calculated as follows.

$f_{VCO} = f_{CLK} \times 512$ f_{VCO} : Reference signal frequency, f_{CLK} : Clock signal frequency

The components connected to the R, C and FIL pins must be connected to the GND1 pin (pin 3) with a line that is as short as possible to reduce influence of noise.

3. Output drive circuit

This IC can be used to implement both upper and lower output N channel power FET drive circuit using a built-in charge pump circuit. The upper side gate voltage is V_{CC}+9V. The lower side gate voltage is VREG(5.6V).
The PWM switching is performed on the UL, VL and WL pins. Therefore, it is performed on the lower output N channel power FET. The driving force of the motor is adjusted by changing the duty that the lower output N channel power FET is on. The PWM frequency is determined with 20kHz (typical) in the IC.
When the PWM switching of the lower output N channel power FET is off, the upper output N channel power FET is turned on (Synchronous rectification). Therefore, it is possible to reduce the temperature increase of the upper output N channel power FET.The off-time of the synchronous rectification is determined in the IC and varies from 1.7µs to 3.7µs.

4. Speed lock range

The speed lock range is less than ±6.25% of the fixes speed. When the motor speed is in the lock range, the LD pin (an open collector output) goes low. If the motor speed goes out of the lock range, the PWM output on-duty is adjusted according to the speed error to control the motor speed to be within the lock range.

5. Hall input signal

The input amplitude of 100mVp-p or more (differential) is desirable in the Hall sensor inputs. The closer the input wave-form is to a square wave, the required input amplitude is lower. Inversely, the closer the input waveform is to a triangular wave, the higher input amplitude is required. Also, note that the input DC voltage must be set to be within the common-mode input voltage range.
If a Hall sensor IC is used to provide the Hall inputs, those signals can be input to one side (either the + or - side) of the Hall sensor signal inputs as 0 to VREG level signals if the other side is held fixed at a voltage within the common-mode input voltage range that applies when the Hall sensors are used.
If noise on the Hall inputs is a problem, that noise must be excluded by inserting capacitors across the inputs. Those capacitors must be located as close as possible to the input pins. When the Hall inputs for all three phases are in the same state, all the outputs will be in the off state.

6. Current limiter circuit

The current limiter circuit limits the (peak) current at the value $I = V_{RF}/Rf$ (V_{RF} = 0.25V (typical), Rf : current detection resistor). The current limitation operation consists of reducing the PWM output on-duty to suppress the current.
High accuracy detection can be achieved by connecting the RF and RFGND pins lines near at the ends of the current detection resistor (Rf).

7. S/S switching circuit

When the S/S pin is set to the low level, S/S switching circuit is the start mode. Inversely, when the S/S pin is set to the high level or open, S/S switching circuit is the stop mode. This IC will be in the power save state of decreasing the supply current at the stop mode. The bias current to most of the circuit in the IC is cut off in the power save state. The operating circuit in the power save state are limited to the S/S switching circuit , the 5V constant voltage output, FG amplifier and FG amplifier Schmitt output. The other circuit do not operate. The upper side output transistors for all phases (the UH, VH and WH side) and the lower side output transistors for all phases (the UL, VL and WL side) are turned off in the power save state.

8. Braking circuit

When the BR pin is set to the high level or open, the brake is on. Inversely, when the BR pin is set to the low level, the brake is released. The brake becomes a short brake that turns on the upper side output transistors for all phases (the UH, VH and WH side) and turns off the lower side output transistors for all phases (the UL, VL and WL side). Note that the current limiter does not operate during braking. The current that flows in the output transistors during braking is determined by the motor back EMF voltage and the coil resistance. Applications must be designed so that this current does not exceed the ratings of the output transistors used. (The higher the motor speed at which braking is applied, the more severe this problem becomes).

The BR pin can be switching at the start mode. (This IC is designed to avoid through currents at changeover.) This means that motor startup and stop control can be performed using the BR pin with the S/S pin held at the low level (the start mode). If the startup time becomes excessive, it can be reduced by controlling the motor startup and stop with the BR pin rather than with the S/S pin (Since the IC will be in the power save state at the stop mode, enough time for the VCO circuit to stabilize will be required at the beginning of the motor start operation).

9. Forward/Reverse switching circuit

The motor rotation direction can be switched by using the F/R pin. However, the following notes must be observed if the F/R pin is switched while the motor is rotating.

- This IC is designed to avoid through currents at changeover. However, the rise in the motor supply voltage (due to instantaneous return of the motor current to the power supply) during direction switching may cause problems. If this rise is a problem, the value of the capacitor inserted between power and ground must be increased.
- If the motor current after direction switching exceeds the current limit value, the PWM drive side outputs will be turned off, but the opposite side output will be in the short-circuit braking state, and a current determined by the motor back EMF voltage and the coil resistance will flow. Applications must be designed so that this current does not exceed the ratings of the output transistors used. (The higher the motor speed at which the direction is switched, the more severe this problem becomes.)

10. Constraint protection circuit

This IC includes the constraint protection circuit to protect the motor and the output transistors in the motor constrained state. If the LD output remains high (indicating the unlocked state) for a fixed period in the motor drive state (the S/S pin : start, the BR pin : brake release), the lower side output transistors (the UL, VL and WL side) are turned off. This time can be set by adjusting the oscillation frequency of the CSD pin by using a external capacitor. By the value (C) of the capacitor attached to the CSD pin, the set time is calculated as follows.

$$\text{The set time (sec)} = 60.8 \times C\ (\mu F)$$

When a 0.047μF capacitor is connected with the CSD pin, the set time becomes about 2.9sec.
By the variance of the IC, “60.8” of the above formula has varied from 40.8 to 80.8.
To restart a motor by cancelling the constraint protection function, any of the following operation is necessary.

- Put the S/S pin into the start state again after the stop mode (about 1ms or more).
- Put the BR pin into the brake release state again after the braking state (about 1ms or more).
- Turn on the power supply again after the turn off state.

When the clock disconnect protection function, the thermal shutdown function and the low-voltage protection function are operating, the constraint protection function does not operate even if the motor does not rotate.
The oscillation waveform of the CSD pin is used as the reference signal for some circuits in addition to the motor constraint protection circuit. Therefore, it is desirable to oscillate the CSD pin even if the constraint protection function is unnecessary. If the constraint protection circuit is not used, the oscillation of the CSD pin must be stopped by connecting a 220kΩ resistor and a 0.01μF capacitor in parallel between the CSD pin and GND. However, in that case, the clock disconnection protection circuit does not operate too. And, the synchronous rectification does not operate in any of the following cases.

- When the motor does not rotate in the motor constrained state since the motor is started up by the S/S or the BR input, the PWM switching is performed by using the current limiter circuit. But, the synchronous rectification does not operate when the oscillation of the CSD pin is stopped.

The CSD pin combines also functions as the initial reset pin. The time that the CSD pin voltage is charged to about 1.25V is determined as the initial reset. At the initial reset, all the outputs will be in the off state.

11. Clock disconnection protection circuit

If the clock input through the CLK pin goes to the no input state in the motor drive state (the S/S pin : start, the BR pin : brake release), the lower side output transistors (the UL, VL and WL side) are turned off. If the clock is resupplied, the clock disconnection protection function is cancelled. When the clock period is longer than about thirty-fourth part of the constraint protection set time, the clock disconnection protection circuit judges the clock input to be the no input state and this protection function will operate.

12. Thermal shutdown circuit

If the junction temperature rises to the specified temperature (TSD) in the motor drive state (the S/S pin : start, the BR pin : brake release), the lower side output transistors (the UL, VL and WL side) are turned off. If the junction temperature falls to more than the hysteresis width (ΔTSD), the thermal shutdown function is cancelled.

13. Low-voltage protection circuit

The IC includes a low-voltage protection circuit to protect against incorrect operation when the V_{CC} power is applied or if the power supply voltage falls below its operating level. When the V_{CC} voltage falls under the specified voltage (VLVSD), all the outputs will be in the off state. If the V_{CC} voltage rises to more than the hysteresis width (ΔVLVSD), the low-voltage protection function is cancelled.

14. Power supply stabilization

Since this IC is used in applications that flow the large output current, the power supply line is subject to fluctuations. Therefore, capacitors with capacitance adequate to stabilize the power supply voltage must be connected between the V_{CC} pin and GND. If diodes are inserted in the power supply line to prevent the IC destruction due to reverse power supply connection, since this makes the power supply voltage even more subject to fluctuations, even larger capacitance will be required.

15. Ground lines

The signal system GND and the output system GND must be separated, and connected to one GND at the connector. As the large current flows to the output system GND, this GND line must be made as short as possible.

Output system GND : GND for Rf and V_{CC} line capacitors
Signal system GND : GND for the IC and external components

16. Integrating amplifier

The integrating amplifier integrates the speed error pulses and phase error pulses and converts them to the speed command voltage. At that time it also sets the control loop gain and the frequency characteristics. External components of the integrating amplifier must be placed as close to the IC as possible to reduce influence of noise.

17. FG amplifier

The FG amplifier normally makes up a filter amplifier to reject noise. Since a clamp circuit has been added at the FG amplifier output, the output amplitude is clamped at about 3.2Vp-p, even if the amplifier gain is increased.
After the FG amplifier, the Schmitt comparator on one side hysteresis(200mV (typical)) is inserted. The Schmitt comparator output (FGS output) becomes high level when the FG amplifier output is lower than the $FGIN^+$ voltage, and becomes low level when the FG amplifier output is higher to more than Schmitt width as compared with the $FGIN^+$ voltage. Therefore, it is desirable that the amplifier gain be set so that the output amplitude is over 1.0Vp-p at the lowest controlled speed to be used.
The capacitor connected between the $FGIN^+$ pin and GND is required for bias voltage stabilization. This capacitor must be connected to the GND1 pin (pin 3) with a line that is as short as possible to reduce influence of noise.
As the FG amplifier and the FGS output are operating even if the S/S pin is the stop state, it is possible to monitor the motor rotation by the FGS output.