ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V⁺ to V⁻) 5.5V
Amplifier Input Current (DC)
  (+IN, −IN, +TERM, −TERM) ....±10mA
Amplifier Input Power (AC)
  (+IN, −IN, +TERM, −TERM) 18dBm
Input Current (V$_{BIAS}$, $\overline{SHDN}$)...............................±10mA
Output Current (+OUT, −OUT) ....±50mA
Operating Temperature Range (Note 2)....–40°C to 85°C
Specified Temperature Range (Note 3) ....–40°C to 85°C
Storage Temperature Range...................–65°C to 150°C
Junction Temperature ....150°C
Lead Temperature (Soldering, 10 sec) ....300°C

PIN CONFIGURATION

TOP VIEW

V⁻	1		12	V⁻
V$_{BIAS}$	2	17	11	$\overline{SHDN}$
V⁺	3		10	V⁺
V⁻	4		9	V⁻

Top pins: 16 15 14 13 (+TERM, +IN, −IN, −TERM)
Bottom pins: 5 6 7 8 (V⁺, +OUT, −OUT, V⁺)

UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T$_{JMAX}$ = 150°C, θ$_{JA}$ = 68°C/W, θ$_{JC}$ = 4.2°C/W
EXPOSED PAD (PIN 17) IS V⁻, MUST BE SOLDERED TO PCB
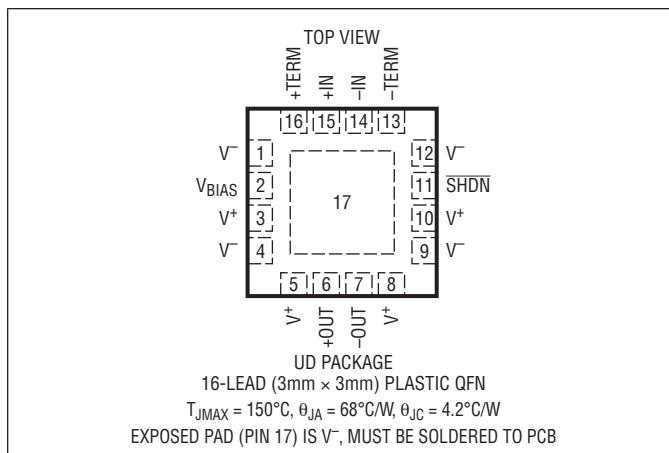
ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE (Notes 2, 3)
LTC6410CUD-6#PBF	LTC6410CUD-6#TRPBF	LDBG	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC6410IUD-6#PBF	LTC6410IUD-6#TRPBF	LDBG	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

3V DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T$_A$ = 25°C. V⁺ = 3V, V⁻ = 0V, $\overline{SHDN}$ = 2V, +IN is shorted to +TERM, −IN is shorted to −TERM, V$_{BIAS}$ = 1.5V, +IN = −IN = 1.5V, input source resistance (R$_S$) is 25Ω on each input (50Ω differential), R$_L$ = 50Ω from +OUT to −OUT, unless otherwise noted. V$_{BIAS}$ is defined as the voltage on the V$_{BIAS}$ pin. V$_{OUTCM}$ is defined as (+OUT + −OUT)/2. V$_{INCM}$ is defined as (+IN + −IN)/2. V$_{INDIFF}$ is defined as (+IN − −IN). V$_{OUTDIFF}$ is defined as (+OUT − −OUT). See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
G$_{DIFF}$	Differential Gain (Low Frequency S21)	V$_{INDIFF}$ = ±0.2V	●	5.0 4.7	6.0	6.7 7.0	dB dB
TC G$_{DIFF}$	Differential Gain Temperature Coefficient		●		0.003		dB/°C
V$_{SWINGDIFF}$	Differential Output Voltage Swing	V$_{OUTDIFF}$, V$_{INDIFF}$ = ±2V	●	2.2 2.0	2.8		V$_{P-P}$ V$_{P-P}$
V$_{SWINGMIN}$	Output Swing Low	Single-Ended +OUT, −OUT, V$_{INDIFF}$ = ±2V	●		0.7	0.9 1.0	V V
V$_{SWINGMAX}$	Output Swing High	Single-Ended +OUT, −OUT, V$_{INDIFF}$ = ±2V	●	1.9 1.8	2.1		V V
I$_{OUT}$	Output Current Drive	Short +OUT to −OUT, V$_{INDIFF}$ = ±2V (Note 4)	●	±38 ±36	±42		mA mA
V$_{OS}$	Input Offset Voltage		●	−2.0 −3.0	0.4	2.0 3.0	mV mV

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3V DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V⁺ = 3V, V⁻ = 0V, $\overline{SHDN}$ = 2V, +IN is shorted to +TERM, −IN is shorted to −TERM, V_{BIAS} = 1.5V, +IN = −IN = 1.5V, input source resistance (R_S) is 25Ω on each input (50Ω differential), R_L = 50Ω from +OUT to −OUT, unless otherwise noted. V_{BIAS} is defined as the voltage on the V_{BIAS} pin. V_{OUTCM} is defined as (+OUT + −OUT)/2. V_{INCM} is defined as (+IN + −IN)/2. V_{INDIFF} is defined as (+IN − −IN). $V_{OUTDIFF}$ is defined as (+OUT − −OUT). See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TC V_{OS}	Input Offset Voltage Drift		●		−0.3		µV/°C
V_{OSINCM}	Common Mode Offset Voltage	$V_{OUTCM} - V_{INCM}$		−40	13	40	mV
			●	−50		50	mV
A_V	Internal Voltage Gain				2.7		V/V
I_{VRMIN}	Input Common Mode Voltage Range, (Min)		●			1.0	V
I_{VRMAX}	Input Common Mode Voltage Range, (Max)		●	2.0			V
R_{INDIFF}	Differential Input Resistance	V_{INDIFF} = ±100mV (Note 4)		40	58	80	Ω
			●	30		100	Ω
X_{INDIFF}	Differential Input Reactance	f = 100MHz			1		pF
R_{INCM}	Input Common Mode Resistance				1000		Ω
CMRR	Common Mode Rejection Ratio	V_{BIAS} = 1.5V, +IN = −IN = 1V to 2V, ($\Delta V_{OUTDIFF}$/Gain)	●	45	60		dB
R_{ODIFF}	Differential Output Resistance	$V_{OUTDIFF}$ = ±100mV (Note 4)		17	22	38	Ω
			●	13		47	Ω
$X_{OUTDIFF}$	Differential Output Reactance	f = 100MHz			10		nH
R_{OUTCM}	Common Mode Output Resistance				7		Ω
Bias Voltage Control (V_{BIAS} Pin)							
G_{CM}	Common Mode Gain	V_{BIAS} = 1.2V to 1.8V (+IN and −IN floating), ΔV_{OUTCM}/(0.6V)		0.7	0.86	1.0	V/V
			●	0.6		1.0	V/V
V_{OCMMIN}	Output Common Mode Voltage Adjustment Range, (Min)		●		1.0	1.2	V
V_{OCMMAX}	Output Common Mode Voltage Adjustment Range, (Max)		●	1.8	2.0		V
V_{OSCM}	Output Common Mode Offset Voltage	$V_{OUTCM} - V_{BIAS}$		−200	100	300	mV
			●	−400		400	mV
R_{VOCM}	V_{BIAS} Input Resistance			2.4	3.0	3.6	kΩ
			●	2.0		4.0	kΩ
C_{VBIAS}	V_{BIAS} Input Capacitance				3		pF
$\overline{SHDN}$ Pin							
V_{IL}	$\overline{SHDN}$ Input Low Voltage		●	0.8	1.0		V
V_{IH}	$\overline{SHDN}$ Input High Voltage		●		1.8	2	V
I_{IL}	$\overline{SHDN}$ Input Low Current	$\overline{SHDN}$ = 0.8V	●	−200	−85	0	µA
I_{IH}	$\overline{SHDN}$ Input High Current	$\overline{SHDN}$ = 2V	●	−150	−30	0	µA
Power Supply							
V_S	Operating Range		●	2.8		5.25	V
I_S	Supply Current				104	130	mA
			●			140	mA
$I_{S\overline{SHDN}}$	Supply Current in Shutdown	$\overline{SHDN}$ = 0.8V	●		3	5	mA
PSRR	Power Supply Rejection Ratio	V⁺ = 2.8V to 5.25V, V_{BIAS} = +IN = −IN = V⁺/2	●	73	100		dB

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5V DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, $\overline{SHDN}$ = 3V, +IN is shorted to +TERM, −IN is shorted to −TERM, V_{INCM} = V_{BIAS} = 2.5V, +IN = −IN = 2.5V, input source resistance (R_S) is 25Ω on each input (50Ω differential), R_L = 50Ω from +OUT to −OUT, unless otherwise noted. V_{BIAS} is defined as the voltage on the V_{BIAS} pin. V_{OUTCM} is defined as (+OUT + −OUT)/2. V_{INCM} is defined as (+IN + −IN)/2. V_{INDIFF} is defined as (+IN − −IN). $V_{OUTDIFF}$ is defined as (+OUT − −OUT). See DC test circuit schematic.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
G_{DIFF}	Differential Gain (Low Frequency S21)	V_{IN} = ±0.2V	●	5 4.7	6.1	6.7 7.0	dB dB
$V_{SWINGDIFF}$	Differential Output Voltage Swing	$V_{OUTDIFF}$, V_{IN} = ±4V	●	4.1 3.5	4.8		V_{P-P} V_{P-P}
$V_{SWINGMIN}$	Output Swing Low	Single-Ended +OUT, −OUT, V_{IN} = ±4V	●		1.1	1.4 1.6	V V
$V_{SWINGMAX}$	Output Swing High	Single-Ended +OUT, −OUT, V_{IN} = ±4V	●	3.2 3.0	3.5		V V
I_S	Supply Current		●		125	150 160	mA mA
$\overline{SHDN}$ Pin							
V_{IL}	$\overline{SHDN}$ Input Low Voltage		●	1.8	2.0		V
V_{IH}	$\overline{SHDN}$ Input High Voltage		●		2.8	3	V
I_{IL}	$\overline{SHDN}$ Input Low Current	$\overline{SHDN}$ = 1.8V	●	−300	−110	0	μA
I_{IH}	$\overline{SHDN}$ Input High Current	$\overline{SHDN}$ = 3V	●	−200	−60	0	μA

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, $\overline{SHDN}$ = 2V, +IN is shorted to +TERM, −IN is shorted to −TERM, V_{INCM} = V_{BIAS} = 1.5V, input source resistance (R_S) is 25Ω on each input (50Ω differential), R_L = 50Ω from +OUT to −OUT, +IN and −IN are AC-coupled, unless otherwise noted. V_{BIAS} is defined as the voltage on the V_{BIAS} pin. V_{OUTCM} is defined as (+OUT + −OUT)/2. V_{INCM} is defined as (+IN + −IN)/2. V_{INDIFF} is defined as (+IN − −IN). $V_{OUTDIFF}$ is defined as (+OUT − −OUT).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
−3dBBW	−3dB Bandwidth	V_{INDIFF} = −10dBm		1	1.4		GHz
0.1dBBW	Bandwidth for 0.1dB Flatness	V_{INDIFF} = −10dBm			150		MHz
0.5dBBW	Bandwidth for 0.5dB Flatness	V_{INDIFF} = −10dBm			300		MHz
SR	Slew Rate				1.5		V/ns
t_S	1% Settling Time	1% Settling for a 1V_{P-P} $V_{OUTDIFF}$ Step			3		ns
t_{ON}	Turn-On Time	$\overline{SHDN}$ = 0V to 3V, +OUT and −OUT Within 10% of Final Values			30		ns
t_{OFF}	Turn-Off Time	$\overline{SHDN}$ = 3V to 0V, +OUT and −OUT Within 10% of Final Values			30		ns
Common Mode Voltage Control (V_{BIAS} Pin)							
−3dBBWCM	Common Mode Small-Signal −3dB Bandwidth	0.2V_{P-P} at V_{BIAS}, Measured V_{OUTCM}			1		GHz
SRCM	Common Mode Slew Rate				100		V/μs
Noise/Harmonic Performance Input/Output Characteristics							
10MHz Signal							
HD2	Second Harmonic Distortion	$V_{OUTDIFF}$ = 0dBm			−85		dBc
HD3	Third Harmonic Distortion	$V_{OUTDIFF}$ = 0dBm			−71		dBc

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AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V$^+$ = 3V, V$^-$ = 0V, $\overline{SHDN}$ = 2V, +IN is shorted to +TERM, −IN is shorted to −TERM, V_{INCM} = V_{BIAS} = 1.5V, input source resistance (R_S) is 25Ω on each input (50Ω differential), R_L = 50Ω from +OUT to −OUT, +IN and −IN are AC-coupled, unless otherwise noted. V_{BIAS} is defined as the voltage on the V_{BIAS} pin. V_{OUTCM} is defined as (+OUT + −OUT)/2. V_{INCM} is defined as (+IN + −IN)/2. V_{INDIFF} is defined as (+IN − −IN). $V_{OUTDIFF}$ is defined as (+OUT − −OUT).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IM3	Third Order Intermodulated Distortion	F1 = 9.5MHz, F2 = 10.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone			−72		dBc
		F1 = 9.5MHz, F2 = 10.5MHz, $V_{OUTDIFF}$ = −5dBm/Tone			−81		dBc
		F1 = 9.5MHz, F2 = 10.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone, V_{CC} = 5V, V_{BIAS} = 2.5V, $\overline{SHDN}$ = 3V			−66		dBc
OIP3	Output Third-Order Intercept	F1 = 9.5MHz, F2 = 10.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone			36		dBm
		F1 = 9.5MHz, F2 = 10.5MHz, $V_{OUTDIFF}$ = −5dBm/Tone			36		dBm
		F1 = 9.5MHz, F2 = 10.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone, V_{CC} = 5V, V_{BIAS} = 2.5V, $\overline{SHDN}$ = 3V			33		dBm
P1dB	Output 1dB Compression Point				12.8		dBm
NF	Noise Figure	Z_{IN} = 50Ω (Note 5) Z_{IN} = 200Ω			11 8		dB dB
70MHz Signal							
HD2	Second Harmonic Distortion	$V_{OUTDIFF}$ = 0dBm			−85		dBc
HD3	Third Harmonic Distortion	$V_{OUTDIFF}$ = 0dBm			−69		dBc
IM3	Third Order Intermodulated Distortion	F1 = 69.5MHz, F2 = 70.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone			−72		dBc
		F1 = 69.5MHz, F2 = 70.5MHz, $V_{OUTDIFF}$ = −5dBm/Tone			−79		dBc
		F1 = 69.5MHz, F2 = 70.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone, V_{CC} = 5V, V_{BIAS} = 2.5V, $\overline{SHDN}$ = 3V			−72		dBc
OIP3	Output Third-Order Intercept	F1 = 69.5MHz, F2 = 70.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone			36		dBm
		F1 = 69.5MHz, F2 = 70.5MHz, $V_{OUTDIFF}$ = −5dBm/Tone			35		dBm
		F1 = 69.5MHz, F2 = 70.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone, V_{CC} = 5V, V_{BIAS} = 2.5V, $\overline{SHDN}$ = 3V			36		dBm
P1dB	Output 1dB Compression Point				12.8		dBm
NF	Noise Figure	Z_{IN} = 50Ω (Note 5) Z_{IN} = 200Ω			11 8		dB dB
140MHz Signal							
HD2	Second Harmonic Distortion	$V_{OUTDIFF}$ = 0dBm			−80		dBc
HD3	Third Harmonic Distortion	$V_{OUTDIFF}$ = 0dBm			−62		dBc
IM3	Third Order Intermodulated Distortion	F1 = 139.5MHz, F2 = 140.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone			−62		dBc
		F1 = 139.5MHz, F2 = 140.5MHz, $V_{OUTDIFF}$ = −5dBm/Tone			−70		dBc
		F1 = 139.5MHz, F2 = 140.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone, V_{CC} = 5V, V_{BIAS} = 2.5V, $\overline{SHDN}$ = 3V			−66		dBc
		F1 = 130MHz, F2 = 150MHz, $V_{OUTDIFF}$ = 0dBm/Tone, V_{CC} = 5V, V_{BIAS} = 2.5V, $\overline{SHDN}$ = 3V			−66	−56	dBc
OIP3	Output Third-Order Intercept	F1 = 139.5MHz, F2 = 140.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone			31		dBm
		F1 = 139.5MHz, F2 = 140.5MHz, $V_{OUTDIFF}$ = −5dBm/Tone			30		dBm
		F1 = 139.5MHz, F2 = 140.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone, V_{CC} = 5V, V_{BIAS} = 2.5V, $\overline{SHDN}$ = 3V			33		dBm
		F1 = 130MHz, F2 = 150MHz, $V_{OUTDIFF}$ = 0dBm/Tone, V_{CC} = 5V, V_{BIAS} = 2.5V, $\overline{SHDN}$ = 3V		28	33		dBm
P1dB	Output 1dB Compression Point				12.8		dBm

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AC ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, $\overline{SHDN}$ = 2V, +IN is shorted to +TERM, –IN is shorted to –TERM, V_{INCM} = V_{BIAS} = 1.5V, input source resistance (R_S) is 25Ω on each input (50Ω differential), R_L = 50Ω from +OUT to –OUT, +IN and –IN are AC-coupled, unless otherwise noted. V_{BIAS} is defined as the voltage on the V_{BIAS} pin. V_{OUTCM} is defined as (+OUT + –OUT)/2. V_{INCM} is defined as (+IN + –IN)/2. V_{INDIFF} is defined as (+IN – –IN). $V_{OUTDIFF}$ is defined as (+OUT – –OUT).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NF	Noise Figure	Z_{IN} = 50Ω (Note 5) Z_{IN} = 200Ω			11 7		dB dB
240MHz Signal							
HD2	Second Harmonic Distortion	$V_{OUTDIFF}$ = 0dBm			–66		dBc
HD3	Third Harmonic Distortion	$V_{OUTDIFF}$ = 0dBm			–52		dBc
IM3	Third Order Intermodulated Distortion	F1 = 239.5MHz, F2 = 240.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone			–54		dBc
		F1 = 239.5MHz, F2 = 240.5MHz, $V_{OUTDIFF}$ = –5dBm/Tone			–63		dBc
		F1 = 239.5MHz, F2 = 240.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone, V_{CC} = 5V, V_{BIAS} = 2.5V, $\overline{SHDN}$ = 3V			–64		dBc
OIP3	Output Third-Order Intercept	F1 = 239.5MHz, F2 = 240.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone			27		dBm
		F1 = 239.5MHz, F2 = 240.5MHz, $V_{OUTDIFF}$ = –5dBm/Tone			27		dBm
		F1 = 239.5MHz, F2 = 240.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone, V_{CC} = 5V, V_{BIAS} = 2.5V, $\overline{SHDN}$ = 3V			32		dBm
P1dB	Output 1dB Compression Point				12.8		dBm
NF	Noise Figure	Z_{IN} = 50Ω (Note 5) Z_{IN} = 200Ω			11 8		dB dB
380MHz Signal							
HD2	Second Harmonic Distortion	$V_{OUTDIFF}$ = 0dBm			–57		dBc
HD3	Third Harmonic Distortion	$V_{OUTDIFF}$ = 0dBm			–45		dBc
IM3	Third Order Intermodulated Distortion	F1 = 379.5MHz, F2 = 380.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone			–51		dBc
		F1 = 379.5MHz, F2 = 380.5MHz, $V_{OUTDIFF}$ = –5dBm/Tone			–64		dBc
		F1 = 379.5MHz, F2 = 380.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone, V_{CC} = 5V, V_{BIAS} = 2.5V, $\overline{SHDN}$ = 3V			–60		dBc
OIP3	Output Third-Order Intercept	F1 = 379.5MHz, F2 = 380.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone			26		dBm
		F1 = 379.5MHz, F2 = 380.5MHz, $V_{OUTDIFF}$ = –5dBm/Tone			27		dBm
		F1 = 379.5MHz, F2 = 380.5MHz, $V_{OUTDIFF}$ = 0dBm/Tone, V_{CC} = 5V, V_{BIAS} = 2.5V, $\overline{SHDN}$ = 3V			30		dBm
P1dB	Output 1dB Compression Point				10.8		dBm
NF	Noise Figure	Z_{IN} = 50Ω (Note 5) Z_{IN} = 200Ω			12 8		dB dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6410C-6/LTC6410I-6 is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 3: The LTC6410C-6 is guaranteed to meet specified performance from 0°C to 70°C. It is designed, characterized and expected to meet specified performance from –40°C and 85°C but is not tested or QA

sampled at these temperatures. The LT6410I-6 is guaranteed to meet specified performance from –40°C to 85°C.

Note 4: This parameter is pulse tested.

Note 5: e_n can be calculated from Z_{IN} = 50Ω NF with the formula:
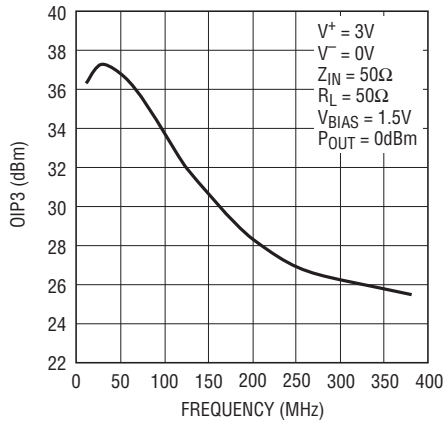
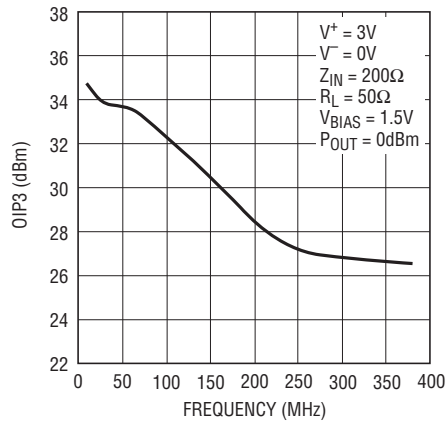$$e_n = \sqrt{(10^{\frac{NF}{10}} - 1)4kT50}$$

where
k = Boltzmann's constant and
T = absolute temperature

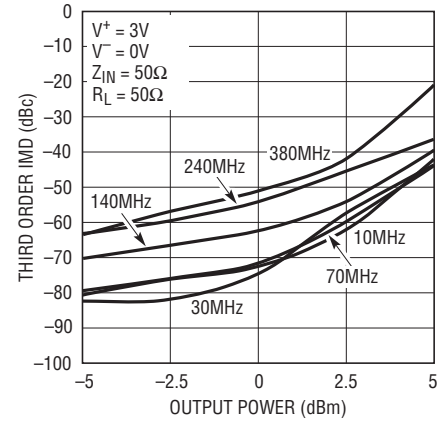64106fa

TYPICAL PERFORMANCE CHARACTERISTICS
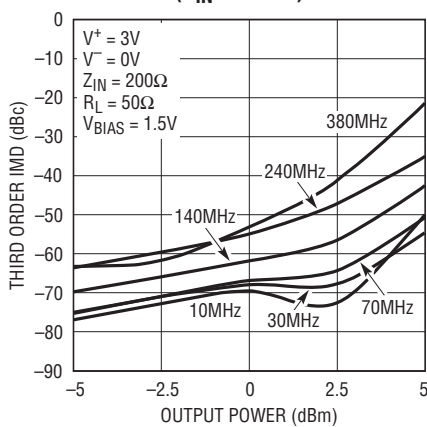
Output Third Order Intercept vs Frequency

V+ = 3V
V− = 0V
Z_IN = 50Ω
R_L = 50Ω
V_BIAS = 1.5V
P_OUT = 0dBm

64106 G01

Output Third Order Intercept vs Frequency (Z_IN = 200Ω)

V+ = 3V
V− = 0V
Z_IN = 50Ω
R_L = 50Ω
V_BIAS = 1.5V
P_OUT = 0dBm

64106 G02

Third Order Intermodulation Distortion vs Frequency vs Power

V+ = 3V
V− = 0V
Z_IN = 50Ω
R_L = 50Ω

64106 G03

Third Order Intermodulation Distortion vs Frequency vs Power (Z_IN = 200Ω)

V+ = 3V
V− = 0V
Z_IN = 200Ω
R_L = 50Ω
V_BIAS = 1.5V

64106 G04

Third Order Intermodulation Distortion vs Temperature

V+ = 3V
V− = 0V
Z_IN = 50Ω
R_L = 50Ω
FREQ = 139.5MHz, 140.5MHz
P_OUT = 0dBm
V_BIAS = 1.5V
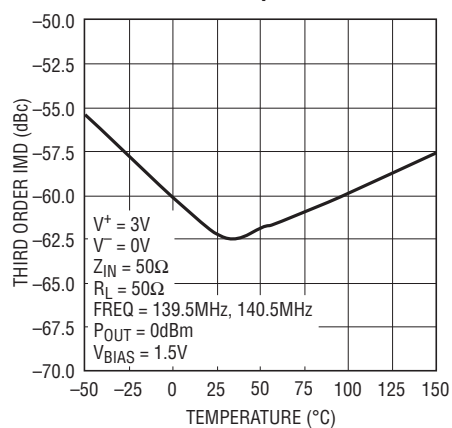
64106 G05

Output 1dB Compression vs Frequency

Z_IN = 50Ω
V+ = 3V
V− = 0V
V_BIAS = 1.5V
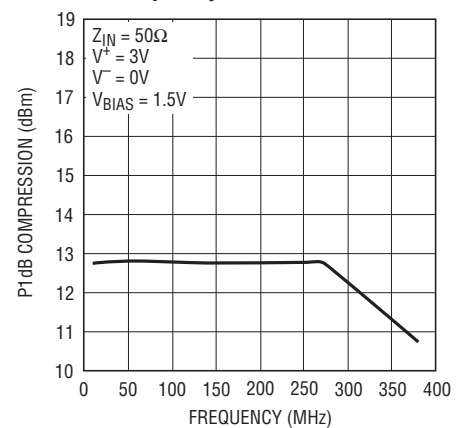
64106 G06

Output Third Order Intercept vs Frequency

V+ = 5V
V− = 0V
Z_IN = 50Ω
R_L = 50Ω
V_BIAS = 2.5V
P_OUT = 0dBm
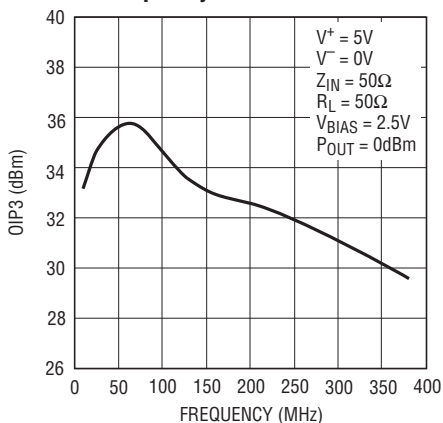
64106 G07

Output 1dB Compression vs Frequency

V+ = 5V
V− = 0V
V_BIAS = 2.5V
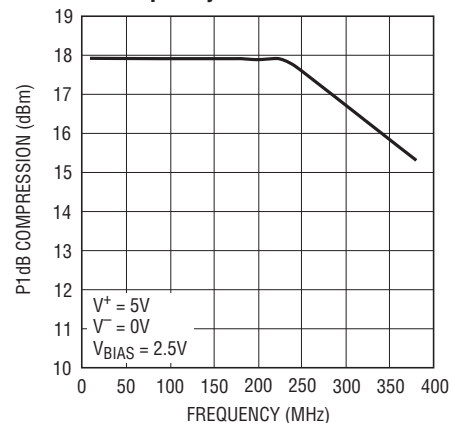
64106 G08

Distortion vs Common Mode Voltage

V+ = 3V
V− = 0V
Z_IN = 50Ω
R_L = 50Ω
FREQ = 139.5MHz, 140MHz
P_OUT = 0dBm

64106 G09

64106fa

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TYPICAL PERFORMANCE CHARACTERISTICS

**Differential Gain
vs Frequency (S21)**

64106 G10
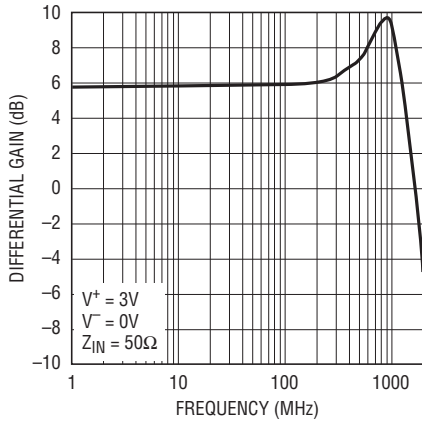
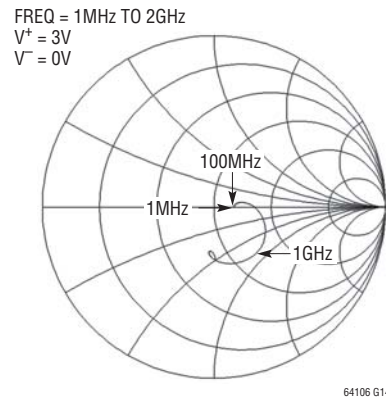**Differential Input Return Loss
vs Frequency (S11)**

64106 G11
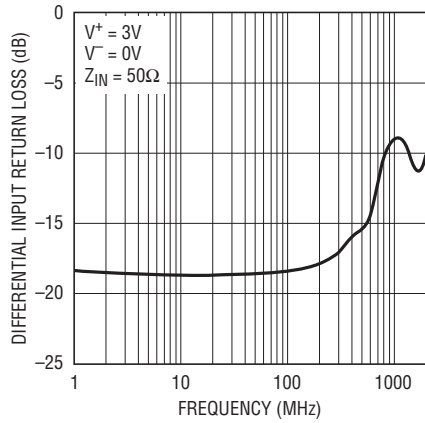
**Differential Output Return Loss
vs Frequency (S22)**

64106 G12
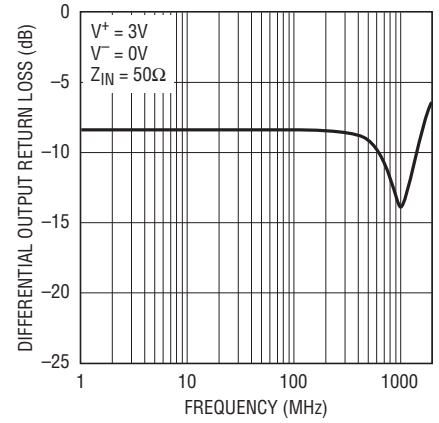
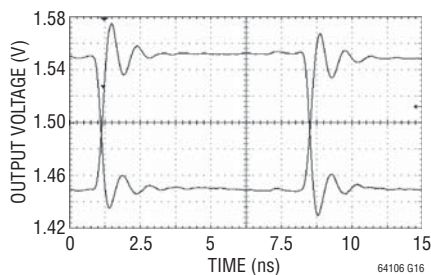**Differential Reverse Isolation
vs Frequency (S12)**

64106 G13
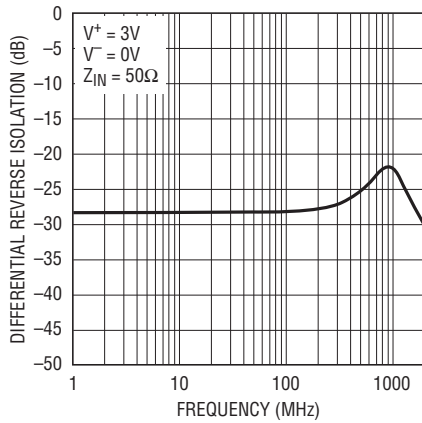
**Differential Input Return Loss
vs Frequency on a Smith Chart (S11)**

64106 G14

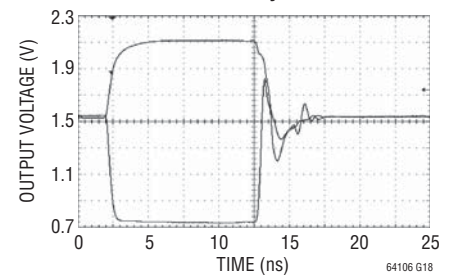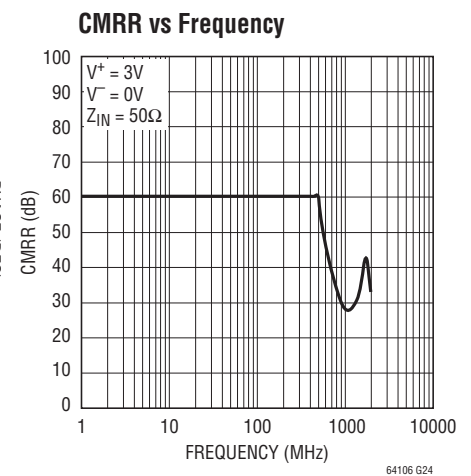**Differential Output Return Loss
vs Frequency on a Smith Chart (S22)**
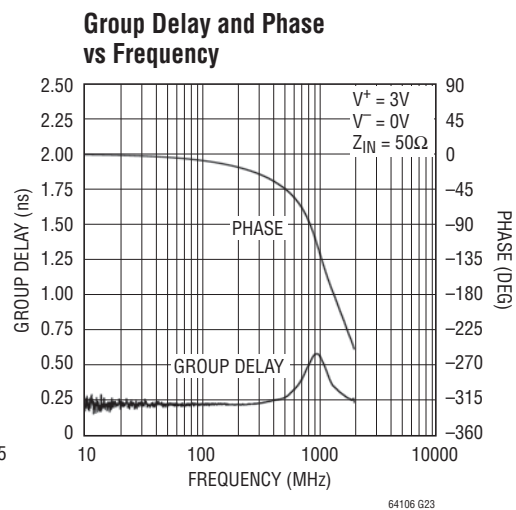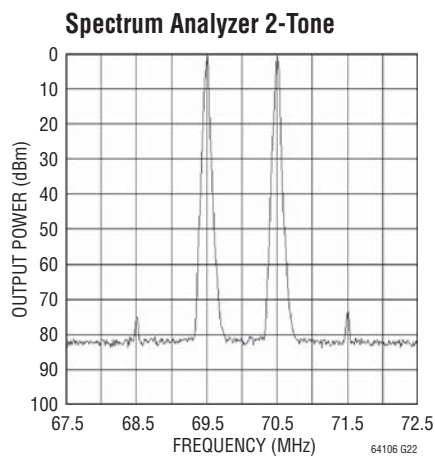

64106 G15
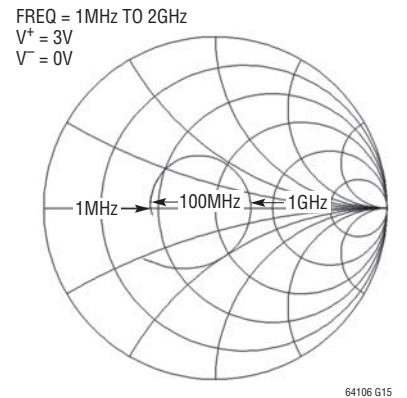
Small-Signal Transient

64106 G16

Large-Signal Transient
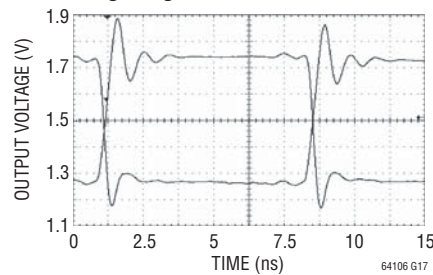
64106 G17

Overdrive Recovery

64106 G18

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Figure vs Frequency vs Z_IN

64106 G19

Turn-On Time

64106 G20

Turn-Off Time

64106 G21

Spectrum Analyzer 2-Tone

64106 G22

Group Delay and Phase vs Frequency

64106 G23

CMRR vs Frequency

64106 G24

DC TEST CIRCUIT SCHEMATIC

$V_{INDIFF} = +IN - -IN$

$V_{INCM} = \dfrac{+IN + -IN}{2}$

$V_{OUTDIFF} = +OUT - -OUT$

$V_{OUTCM} = \dfrac{+OUT + -OUT}{2}$

$R_L = 50\Omega$

LTC6410-6

64106 TC

64106fa
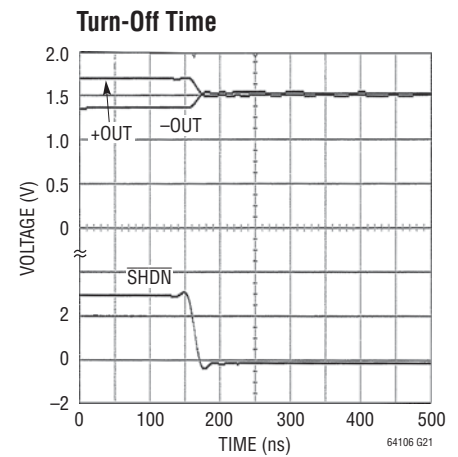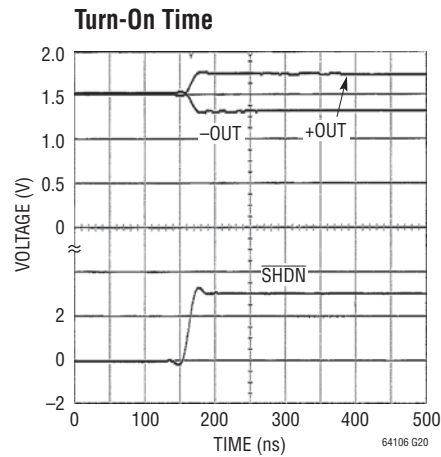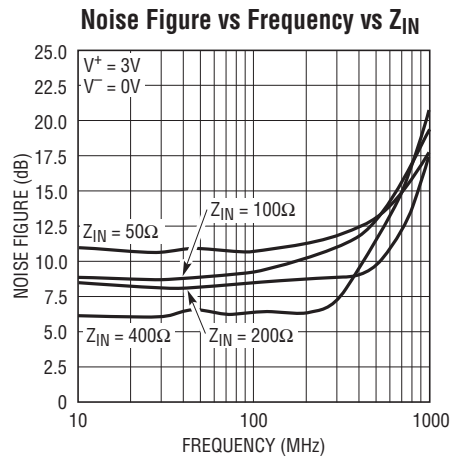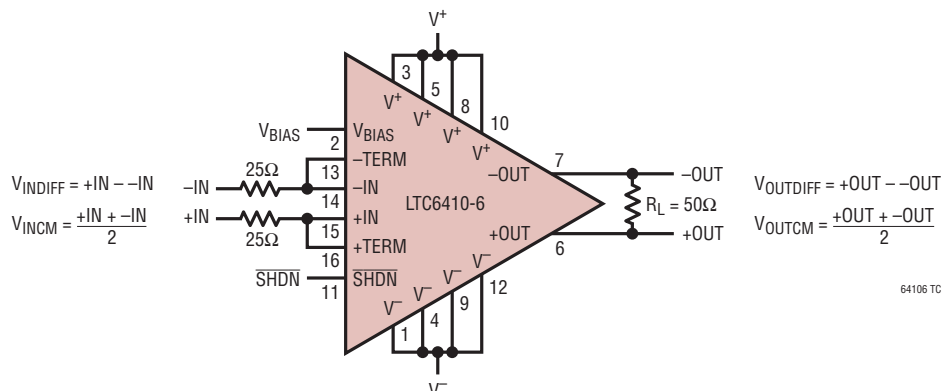
PIN FUNCTIONS

V⁻ (Pins 1, 4, 9, 12, 17): Negative Power Supply (Normally Tied to Ground). All 5 pins must be tied to the same voltage. V⁻ maybe tied to a voltage other than ground as long as the voltage between V⁺ and V⁻ is 2.8V to 5.5V. If the V⁻ pins are not tied to ground, bypass each with 680pF and 0.1µF capacitors as close to the package as possible.

V$_{BIAS}$ (Pin 2): This pin sets the input and output common mode voltage by driving the +IN and –IN through a buffer with a high output resistance of 1k. If the part is AC-coupled at the input, the V$_{BIAS}$ will set the V$_{INCM}$ and therefore the V$_{OUTCM}$ voltage. If the part is DC-coupled at the input, V$_{BIAS}$ should be left floating. Internal resistors bias V$_{BIAS}$ to 1.4V on a 3V supply.

V⁺ (Pins 3, 5, 8, 10): Positive Power Supply. All 4 pins must be tied to the same voltage. Split supplies are possible as long as the voltage between V⁺ and V⁻ is 2.8V to 5.5V. Bypass capacitors of 680pF and 0.1µF as close to the part as possible should be used between supplies.

+OUT, –OUT (Pins 6, 7): Outputs. These pins each have internal series termination resistors forming a differential output resistance.

SHDN (Pin 11): This pin is internally pulled high by a typically 30k resistor to V⁺. By pulling this pin low the supply current will be reduced to typically 3mA. See DC Electrical Characteristics table for the specific logic levels.

–TERM (Pin 13): Negative Input Termination. When tied directly to –IN, it provides an active 50Ω differential termination when +TERM is also tied directly to +IN.

–IN (Pin 14): Negative Input. This pin is normally tied to –TERM, the input termination pin. If AC-coupled, this pin will self bias by V$_{BIAS}$.

+IN (Pin 15): Positive Input. This pin is normally tied to +TERM, the input termination pin. If AC-coupled, this pin will self bias by V$_{BIAS}$.

+TERM (Pin 16): Positive Input Termination. When tied directly to +IN, it provides an active 50Ω differential termination when –TERM is also tied directly to –IN.

Exposed Pad (Pin 17): V⁻. The Exposed Pad must be soldered to the PCB metal.

BLOCK DIAGRAM

64106 BD

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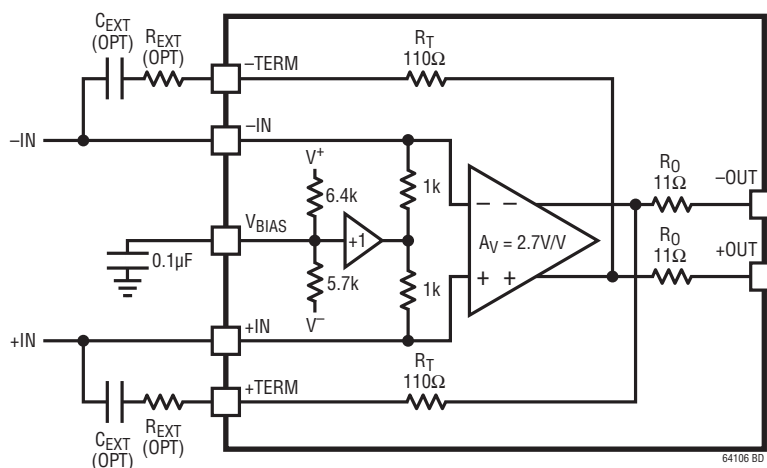
APPLICATIONS INFORMATION

Introduction

The LTC6410-6 is a low noise differential high speed amplifier. By default, the LTC6410-6 has 6dB voltage gain and is designed to operate with 50Ω differential input and output impedances. By changing (R_{EXT}), alternative configurations provide input resistances of up to 400Ω, with correspondingly lower noise figure and higher power gain. The Block Diagram shows the basic circuit along with key external components while Table 1 provides configuration information. If the input is AC-coupled, the V_{BIAS} pin sets the input common mode voltage and therefore the output common mode voltage.

Input Impedance

LTC6410-6 has been designed with very flexible input termination circuitry. By default, with the termination pins connected directly to the inputs, the input impedance is 58Ω, see the Block Diagram. Internally, there is 110Ω between each input and the opposite output (R_T). Dividing the resistor by the internal noise gain of 2.7 + 1 = 3.7, 29.5Ω input impedance is created (59Ω differential). In parallel with the 2k common mode resistance, a total of 58Ω differential input impedance is achieved. This method of termination is used to provide lower noise figure through the use of feedback which reduces the effective noise of the termination resistor. By adding additional resistance in series with the termination pins, higher input impedances can be obtained (see Table 1). The optimum impedance for minimizing the noise figure of the LTC6410-6 is close to 400Ω. Because the amplifier is inherently a voltage amplifier, the difference between the impedance at the input and the output adds additional power gain as can be seen in Table 1. These higher impedance levels can be useful in interfacing with active mixers which can have output impedance of 400Ω and beyond.

Input and Output Common Mode Bias

The LTC6410-6 is internally self-biased through the V_{BIAS} pin (see the Block Diagram). Therefore the LTC6410-6 can be AC-coupled with no external biasing circuitry. The output will have approximately the same common mode voltage as the input.

In the case of a DC-coupled input connection, the input DC common mode voltage will also set the output common mode voltage. Note that a voltage divider is formed between the V_{BIAS} buffer output and the DC input source impedance.

The V_{BIAS} pin has an internal voltage divider which will self bias to approximately 1.4V on a 3V supply (0.47 • V_{SUPPLY}). An external capacitor of 0.1µF to ground is recommended to bypass the pin. The resistance of the pin is 3k. See Distortion vs Common Mode graph.

For increased common mode accuracy, the +TERM and –TERM pins can be AC-coupled to the inputs with capacitors (C_{EXT}). This coupling prevents the feedback from the termination resistance from creating additional DC common mode voltage error. The G_{CM} and V_{OSCM} of the DC Electrical Characteristics table reflect the less accurate DC-coupled scenario.

The termination inputs are part of a high speed feedback loop. The physical length of the termination loop (R_{EXT} and C_{EXT}) must be minimized to maintain stability and minimize gain peaking.

Gain

Internally, the LTC6410-6 has a voltage gain of 2.7V/V. The default source and load resistances in most of the data sheet are assumed to be 50Ω differential. Due to the input and output resistance of the LTC6410-6 being 58Ω and 22Ω respectively, the overall voltage gain in a 50Ω system is 6dB (2V/V). Other source and load resistances will produce different gains due to the resistive dividers. Figure 1 is a system diagram for calculating gain.
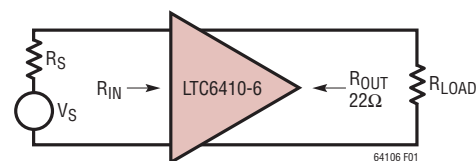

Figure 1

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APPLICATIONS INFORMATION

Therefore the differential voltage gain can be calculated as follows:

$$\text{Voltage Gain} = 2 \bullet \frac{R_{IN}}{R_{IN} + R_S} \bullet 2.7 \bullet \frac{R_L}{R_L + R_{OUT}}$$

The following is an example of the 50Ω gain calculation:

$$\text{Voltage Gain} = 2 \bullet \frac{58}{58+50} \bullet 2.7 \bullet \frac{50}{50 + 22}$$
$$= 2.0\text{V/V} = 6.0\text{dB}$$

The part also can be used with different input impedances providing no additional voltage gain, but a higher power gain.

For example, the calculation for a 100Ω input impedance shows the effect of an impedance conversion. The voltage gain is calculated as follows:

$$\text{Voltage Gain} = 2 \bullet \frac{83}{83+100} \bullet 2.7 \bullet \frac{50}{50 + 22}$$
$$= 1.7\text{V/V} = 4.6\text{dB}$$

However the power gain is:

$$\text{Power Gain} = \left(2 \bullet \frac{83}{83+100} \bullet 2.7 \bullet \frac{50}{50 + 22} \bullet \sqrt{2} \right)^2$$
$$= 5.8\text{mW/mW} = 7.6\text{dB}$$

Output Impedance

The LTC6410-6 is designed to drive a differential load of 50Ω with a total differential output resistance of 22Ω. While the LTC6410-6 can source and sink approximately 50mA, large DC output current should be avoided. To test the part on traditional 50Ω test equipment, AC coupling or balun transformers (or both) may be necessary at the input and output.

Supply Rails

Inductance in the supply path can severely effect the performance of the LTC6410-6. Therefore it is recommended that low inductance bypass capacitors are installed very close to the part. 680pF and 0.1µF sized capacitors are recommended. Additionally, the exposed pad of the part must be connected to V⁻ for low inductance and low thermal resistance. Failure to provide a low impedance supply at high frequencies can cause oscillations and increased distortion.

$\overline{\text{SHDN}}$

The $\overline{\text{SHDN}}$ pin self-biases to V⁺ through a 30k resistor. The pin must be pulled below 0.8V in order to shut down the part.
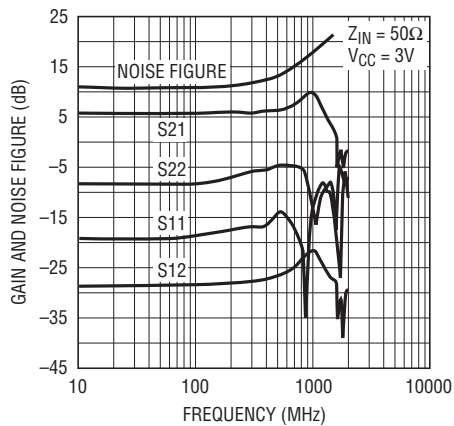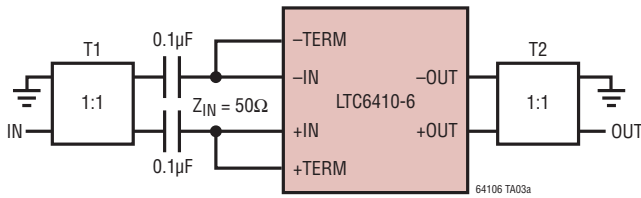
Applications Circuits

The graphs on the following page are examples of the four differential input resistances used on the DC1103A demo board with balun transformers for interfacing with the 50Ω single-ended measurement equipment.

Table 1. Input Impedance

| DIFFERENTIAL SOURCE RESISTANCE (Ω) (R_S)	EXTERNAL TERMINATION RESISTOR (Ω) (R_{EXT})	EFFECTIVE DIFFERENTIAL INPUT IMPEDANCE (Ω) (R_{IN})	DIFFERENTIAL LOAD RESISTANCE (Ω)	OUTPUT RESISTANCE (Ω)	POWER GAIN (dB)	VOLTAGE GAIN (SOURCE AND LOAD RESISTANCE AS STATED (V/V)	NF AT 10MHz (dB)
50	0	58	50	22	6.0	2.0	11
100	49.9	83	50	22	7.6	1.7	9
200	249	177	50	22	10.9	1.8	7
400	750	377	50	22	14.2	1.8	6
2000	Open	2000	50	22	21.5	1.9	–

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LINEAR TECHNOLOGY

APPLICATIONS INFORMATION

Z_{IN} = 50Ω, T1 = ETC1-1-13, T2 = ETC1-1-13

64106 TA03a

64106 TA02b

Z_{IN} = 100Ω, T1 = WBC2-1TL, T2 = ETC1-1-13
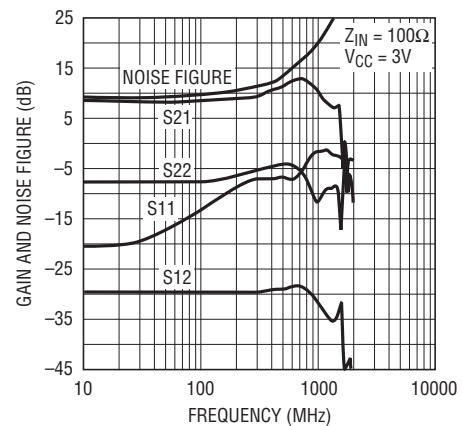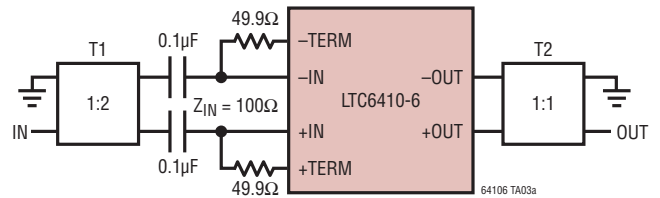
64106 TA03a

64106 TA03b

Z_{IN} = 200Ω, T1 = WBC4-14L, T2 = ETC1-1-13
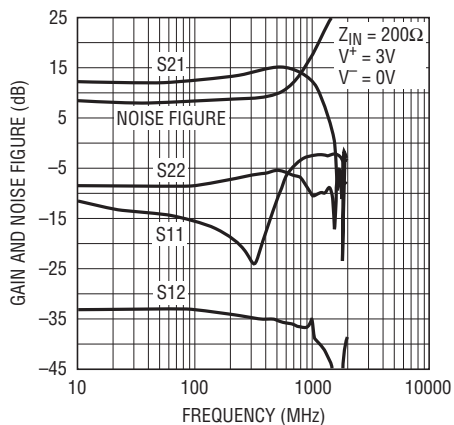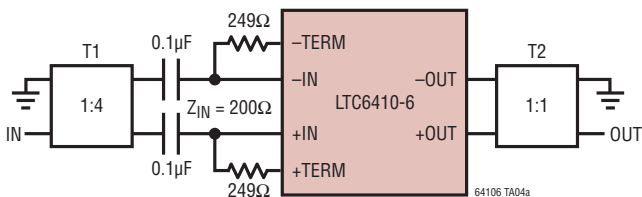
64106 TA04a

64106 TA04b

Z_{IN} = 400Ω, T1 = WBC8-1L, T2 = ETC1-1-13
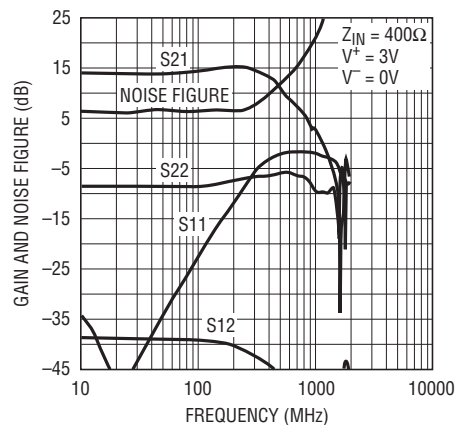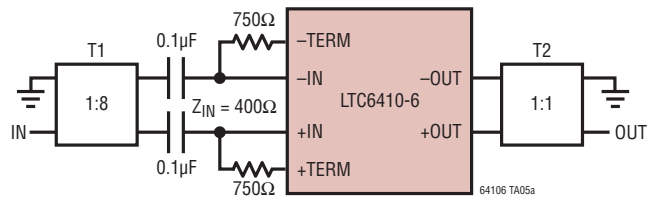
64106 TA05a

64106 TA05b

APPLICATIONS INFORMATION

Demoboard DC1103A Top Silkscreen
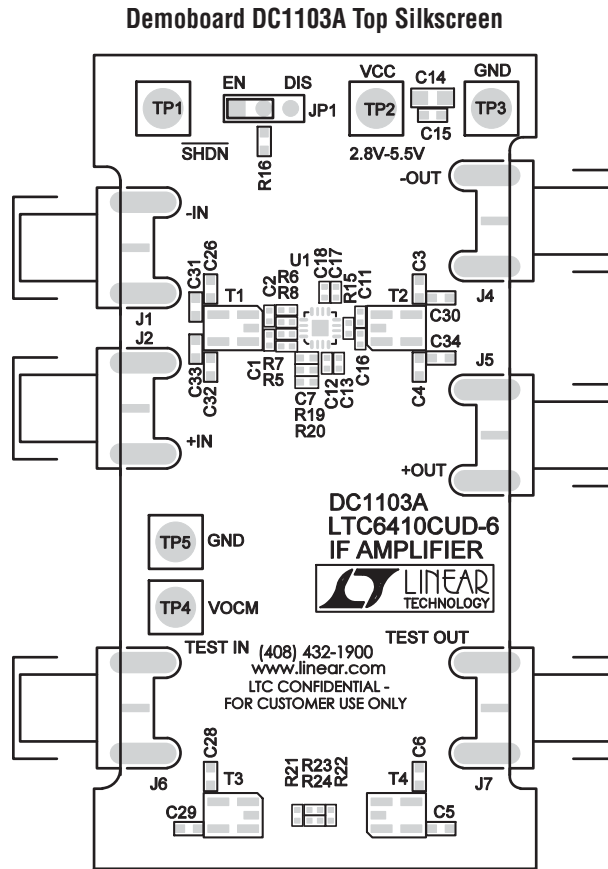
TYPICAL APPLICATION

SAW Filter Application
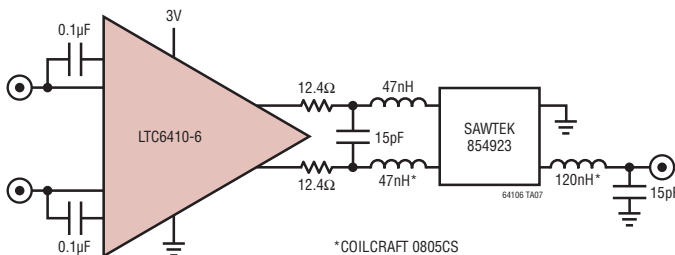
The schematic above shows a typical signal chain application with the LTC6410-6 in combination with a 140MHz center frequency 24MHz bandwidth SAW filter. Without the LTC6410-6, the attenuation of the SAW would be –11.5dB. The networks between the LTC6410-6 and the SAW filter, and after the SAW filter are for proper impedance matching.

The differential output of the LTC6410-6 allows differential driving of the SAW filter without the need for a transformer. The differential nature of the LTC6410-6 allows for ease of use in differential signal chains, and may reduce the need for transformers.

SAW Filter Application

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PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

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TYPICAL APPLICATION

Demoboard DC1103A Schematic

NOTE: UNLESS OTHERWISE SPECIFIED
(1) NOT POPULATED

64106 TA06
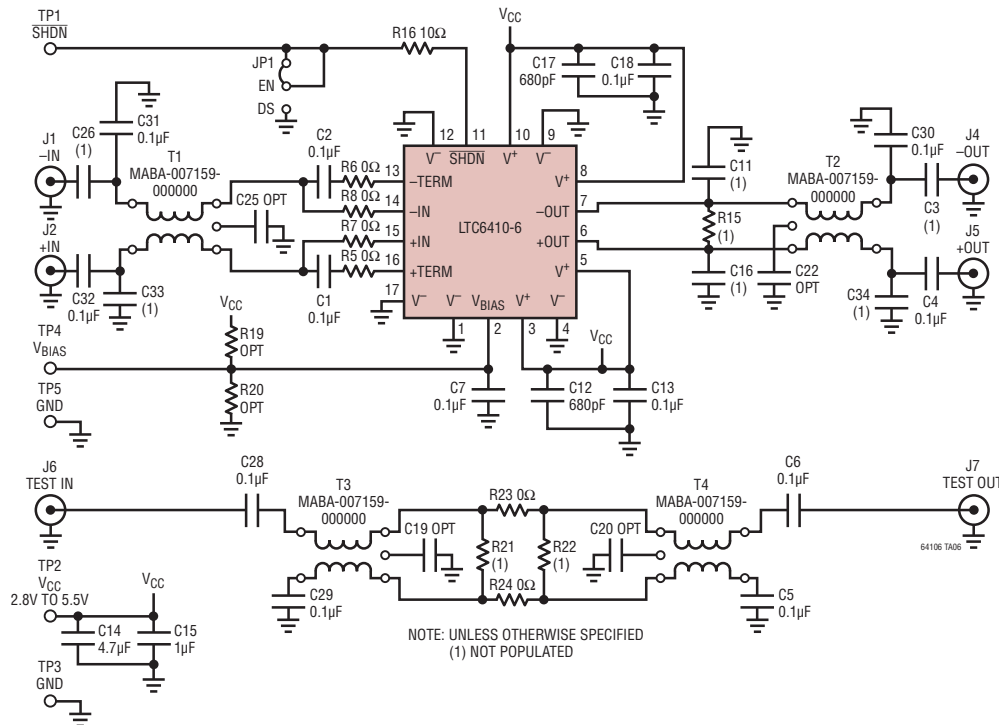
RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1993-2	800MHz Differential Amplifier/ADC Driver	A_V = 2V/V, NF = 12.3dB, OIP3 = 38dBm at 70MHz
LT1993-4	900MHz Differential Amplifier/ADC Driver	A_V = 4V/V, NF = 14.5dB, OIP3 = 40dBm at 70MHz
LT1993-10	700MHz Differential Amplifier/ADC Driver	A_V = 10V/V, NF = 12.7dB, OIP3 = 40dBm at 70MHz
LT5514	Ultralow Distortion IF Amplifier/ADC Driver	Digitally Controlled Gain Output IP3 47dBm at 100MHz
LT5522	600MHz to 2.7GHz High Signal Level Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports, R_{OUT} = 400Ω
LT5524	Low Power, Low Distortion ADC Driver with Digitally Programmable Gain	450MHz Bandwidth, 40dBm OIP3, 4.5dB to 27dB Gain Control
LT5525	High Linearity, Low Power Downconverting Mixer	Single-Ended 50Ω RF and LO Ports, 17.6dBm IIP3 at 1900MHz, I_{CC} = 28mA
LT5526	High Linearity, Low Power Downconverting Mixer	3V to 5.3V Supply, 16.5dBm IIP3, 100kHz to 2GHz RF, NF = 11dB, I_{CC} = 28mA, −65dBm LO-RF Leakage
LT5527	400MHz to 3.7GHz High Signal Level Downconverting Mixer	CG = 2.3dB at 1900MHz, IIP3 = 23.5dBm at 1900MHz, 440mW, R_{OUT} = 415Ω
LT5557	400MHz to 3.8GHz High Signal Level Downconverting Mixer	CG = 2.9dB at 1950MHz, IIP3 = 24.7dBm at 1950MHz, 300mW, R_{OUT} = 560Ω
LTC6400-20	1.8GHz Low Noise, Low Distortion ADC Driver for 300MHz IF	A_V = 20dB, Z_{IN} = 200Ω, $I_{S(MAX)}$ = 105mA at 25°C
LTC6401-20	1.4GHz Low Noise, Low Distortion ADC Driver for 140MHz IF	A_V = 20dB, Z_{IN} = 200Ω, $I_{S(MAX)}$ = 62mA at 25°C
LT6402-6	300MHz Differential Amplifier/ADC Driver	A_V = 6dB, e_n = 3.8nV/$\sqrt{Hz}$ at 20MHz, 150mW
LT6402-12	300MHz Differential Amplifier/ADC Driver	A_V = 12dB, e_n = 2.6nV/$\sqrt{Hz}$ at 20MHz, 150mW
LT6402-20	300MHz Differential Amplifier/ADC Driver	A_V = 20dB, e_n = 1.9nV/$\sqrt{Hz}$ at 20MHz, 150mW
LT6411	650MHz Differential ADC Driver/Dual Selectable Gain Amplifier	3300V/μs Slew Rate, 16mA Current Consumption, Selectable Gain: A_V = −1, 1, 2

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