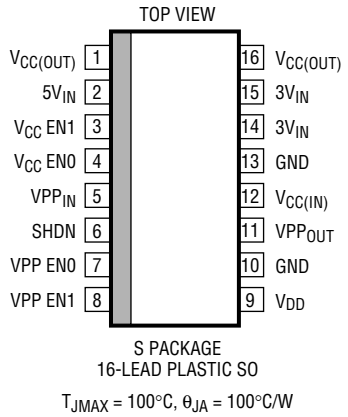
ABSOLUTE MAXIMUM RATINGS

(Note 1)

$5V_{IN}$ Supply Voltage ..... –0.3V to 7V
$3V_{IN}$ Supply Voltage ..... –0.3V to 7V
VPP_{IN} Supply Voltage ..... –0.3V to 13.2V
$V_{CC(IN)}$ Supply Voltage ..... –0.3 to 7V
$V_{DD(IN)}$ Supply Voltage ..... –0.3V to 7V
VPP_{OUT} (OFF) ..... –0.3V to 13.2V
$V_{CC(OUT)}$ (OFF) ..... –0.3V to 7V
Enable Inputs ..... –0.3V to $5V_{IN}$
VPP_{OUT} Short-Circuit Duration ..... Indefinite
$V_{CC(OUT)}$ Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Junction Temperature ..... 100°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC1472CS

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

(V_{CC} Switch Section) The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $5V_{IN}$ = 5V, $3V_{IN}$ = 3.3V, VPP EN0 = VPP EN1 = 0V, (Note 2) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$5V_{IN}$	$5V_{IN}$ Supply Voltage Range	(Note 3)		4.75		5.25	V
$3V_{IN}$	$3V_{IN}$ Supply Voltage Range	(Note 4)		0		3.60	V
I_{5VIN}	$5V_{IN}$ Supply Current	Program to Hi-Z Program to 5V, No Load Program to 3.3V, No Load	● ● ●		0.01 140 100	10 200 160	µA µA µA
I_{3VIN}	$3V_{IN}$ Supply Current	Program to Hi-Z. Program to 5V, No Load Program to 3.3V, No Load	● ● ●		0.01 0.01 40	10 10 80	µA µA µA
R_{ON}	5V Switch On Resistance 3.3V Switch On Resistance	Program to 5V, I_{OUT} = 500mA Program to 3.3V, I_{OUT} = 500mA			0.14 0.12	0.18 0.16	Ω Ω
I_{LKG}	Output Leakage Current OFF	V_{CC} EN0 = V_{CC} EN1 = 0V or 5V, 0V ≤ $V_{CC(OUT)}$ ≤ 5V	●			±10	µA
I_{LIM5V}	$V_{CC(OUT)}$ 5V Current Limit	Program to 5V, $V_{CC(OUT)}$ = 0V (Note 5)			1		A
I_{LIM3V}	$V_{CC(OUT)}$ 3.3V Current Limit	Program to 3.3V, $V_{CC(OUT)}$ = 0V (Note 5)			1		A
V_{CCENH}	V_{CC} Enable Input High Voltage		●	2			V
V_{CCENL}	V_{CC} Enable Input Low Voltage		●			0.8	V
I_{VCCEN}	V_{CC} Enable Input Current	0V ≤ V_{CCEN} ≤ 5V				±1	µA
t_{VCC1}	Delay + Rise Time	From 0V to 3.3V, R_{LOAD} = 100Ω, C_{LOAD} = 1µF (Note 6)		0.2	0.32	1	ms
t_{VCC2}	Delay + Rise Time	From 3.3V to 5V, R_{LOAD} = 100Ω, C_{LOAD} = 1µF (Note 6)		0.2	0.52	1	ms
t_{VCC3}	Delay + Rise Time	From 0V to 5V, R_{LOAD} = 100Ω, C_{LOAD} = 1µF (Note 6)		0.2	0.38	1	ms

ELECTRICAL CHARACTERISTICS

(VPP Switch Section) The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V, $V_{CC(IN)}$ = 5V, VPP_{IN} = 12V, V_{CCEN0} = V_{CCEN1} = 0V, (Note 2) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CC(IN)}$	V_{CC} Input Voltage Range		●	3		5.5	V
VPP_{IN}	VPP Input Voltage Range	(Note 7)	●	0		12.6	V
V_{DD}	Logic Supply Voltage Range	(Note 8)	●	4.5		5.5	V
I_{CCIN}	$V_{CC(IN)}$ Supply Current, No Load	Program to VPP_{IN} or $V_{CC(IN)}$ VPP_{IN} = 12V Program to 0V or Hi-Z	● ●		35 0.01	60 10	µA µA
I_{PPIN}	VPP_{IN} Supply Current, No Load	Program to VPP_{IN} or $V_{CC(IN)}$ Program to 0V or Hi-Z	● ●		40 0.01	80 10	µA µA
I_{DD}	V_{DD} Supply Current, No Load	Program to VPP_{IN} Program to $V_{CC(IN)}$, VPP_{IN} = 0V Program to $V_{CC(IN)}$, VPP_{IN} = 12V Program to 0V or Hi-Z	● ● ● ●		70 85 40 0.01	120 150 80 10	µA µA µA µA
I_{VPPOUT}	Hi-Z Output Leakage Current	Program to Hi-Z, 0V < VPP_{OUT} < 12V	●		0.01	10	µA
R_{ON}	On Resistance VPP_{OUT} to VPP_{IN} On Resistance VPP_{OUT} to $V_{CC(IN)}$ On Resistance VPP_{OUT} to GND	VPP_{IN} = 12V, I_{LOAD} = 120mA $V_{CC(IN)}$ = 5V, I_{LOAD} = 5mA V_{DD} = 5V, I_{SINK} = 1mA			0.50 1.70 100	1 5 250	Ω Ω Ω
VPP_{ENH}	VPP Enable Input High Voltage	V_{DD} = 5V	●	2			V
VPP_{ENL}	VPP Enable Input Low Voltage	V_{DD} = 5V	●			0.8	V
I_{VPPEN}	VPP Enable Input Current	0V < VPP EN < VDD	●			±1	µA
V_{SDH}	SHDN Output High Voltage	Program to 0V, $V_{CC(IN)}$ or Hi-Z, I_{LOAD} = 400µA	●	3.5			V
V_{SDL}	SHDN Output Low Voltage	Program to VPP_{IN}, I_{SINK} = 400µA	●			0.4	V
I_{LIMVCC}	VPP_{OUT} Current Limit, $V_{CC(IN)}$	Program to $V_{CC(IN)}$, VPP_{OUT} = 0V (Note 5)			60		mA
I_{LIMVPP}	VPP_{OUT} Current Limit, VPP_{IN}	Program to VPP_{IN}, VPP_{OUT} = 0V (Note 5)			100		mA
t_{VPP1}	Delay and Rise Time	From 0V to $V_{CC(IN)}$,VPP_{IN} = 0V (Note 9)		5	15	50	µs
t_{VPP2}	Delay and Rise Time	From 0V to VPP_{IN} (Note 9)		25	85	250	µs
t_{VPP3}	Delay and Rise Time	From $V_{CC(IN)}$ to VPP_{IN} (Note 9)		30	100	300	µs
t_{VPP4}	Delay and Fall Time	From VPP_{IN} to $V_{CC(IN)}$ (Note 10)		5	15	50	µs
t_{VPP5}	Delay and Fall Time	From VPP_{IN} to 0V (Note 11)		10	35	100	µs
t_{VPP6}	Delay and Fall Time	From $V_{CC(IN)}$ to 0V, VPP_{IN} = 0V (Note 11)		10	30	100	µs
t_{VPP7}	Output Turn-On Delay	From Hi-Z to $V_{CC(IN)}$ (Note 9)		5	15	50	µs
t_{VPP8}	Output Turn-On Delay	From Hi-Z to VPP_{IN} (Note 9)		25	85	250	µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: V_{ENH} = 5V, V_{ENL} = 0V. See V_{CC} and VPP Switch Truth Tables for programming enable inputs for desired output states.

Note 3: Power for the V_{CC} input logic and charge pump circuitry is derived from the $5V_{IN}$ power supply which must be continuously powered. 12V and 3.3V power is not required to control the NMOS V_{CC} switches. (See Applications Information.)

Note 4: The two $3V_{IN}$ supply input pins (14 and 15) must be connected together and the two $V_{CC(OUT)}$ output pins (1 and 16) must be connected together. The $3V_{IN}$ supply pins do not need to be continuously powered and may drop to 0V when not required.

Note 5: The V_{CC} and VPP output are protected with foldback current limit which reduces the short-circuit (0V) currents below peak permissible current levels at higher output voltages.

Note 6: To 90% of final value.

Note 7: 12V power is only required when VPP_{OUT} is programmed to 12V. The external 12V regulator can be shutdown at all other times. Built-in charge pumps power the internal NMOS switches from the 5V V_{DD} supply when 12V is not present.

Note 8: Power for the VPP input logic and charge pump circuitry is derived from the V_{DD} power supply which must be continuously powered.

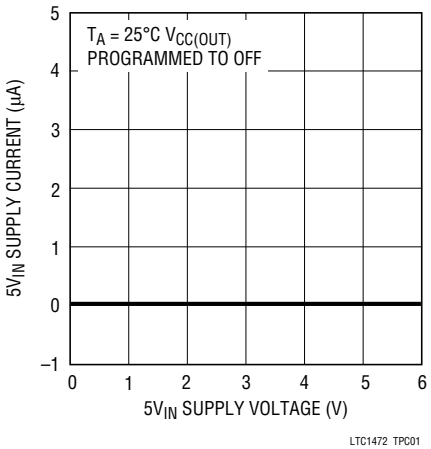
Note 9: To 90% of the final value, C_{OUT} = 0.1µF, R_{OUT} = 2.9k.

Note 10: To 10% of the final value, C_{OUT} = 0.1µF, R_{OUT} = 2.9k.

Note 11: To 50% of the initial value, C_{OUT} = 0.1µF, R_{OUT} = 2.9k.

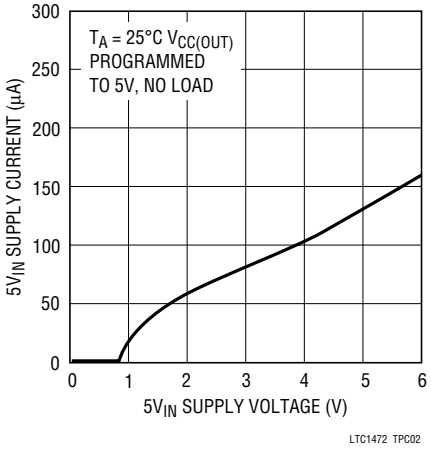
TYPICAL PERFORMANCE CHARACTERISTICS (V_{CC} Section) VPP EN0 = VPP EN1 = 0V

$5V_{IN}$ Supply Current (OFF)



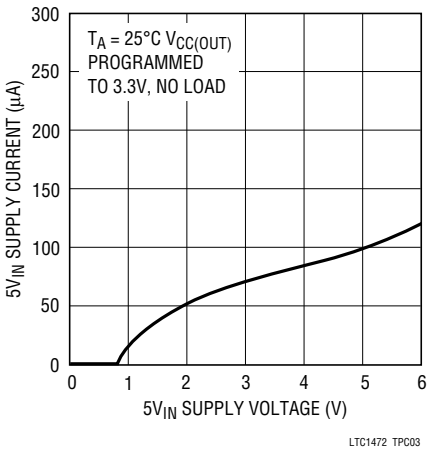
LTC1472 TPC01

$5V_{IN}$ Supply Current (5V ON)



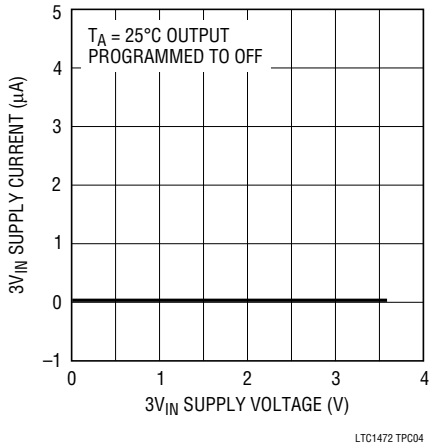
LTC1472 TPC02

$5V_{IN}$ Supply Current (3.3V ON)



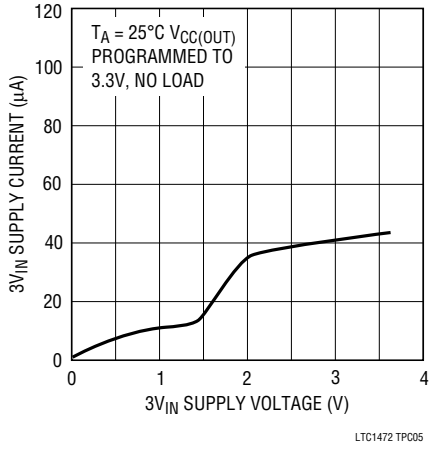
LTC1472 TPC03

$3V_{IN}$ Supply Current (OFF)



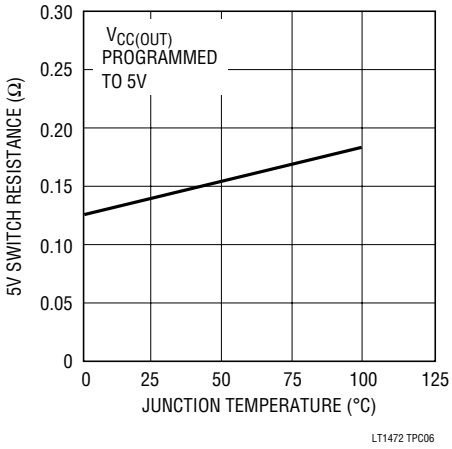
LTC1472 TPC04

$3V_{IN}$ Supply Current (3.3V ON)



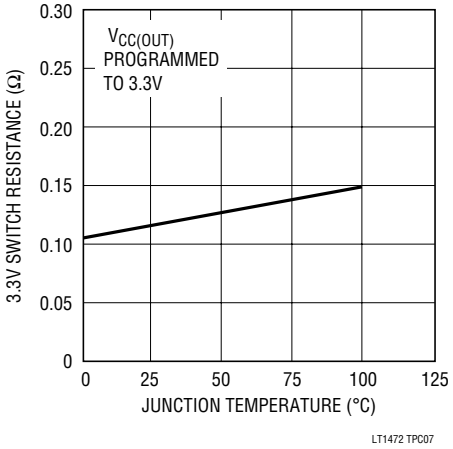
LTC1472 TPC05

5V Switch Resistance



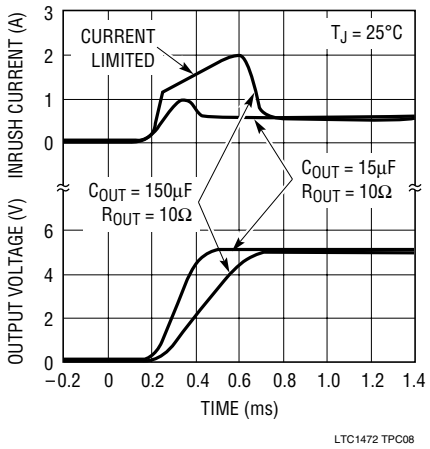
LT1472 TPC06

3.3V Switch Resistance



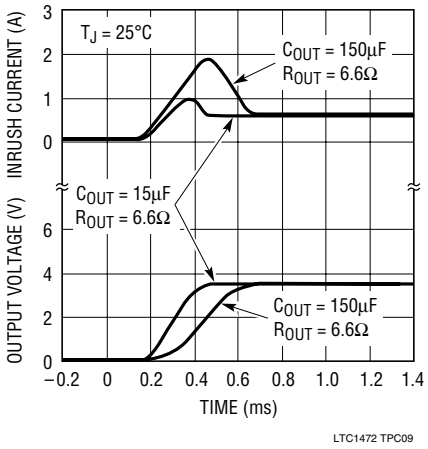
LT1472 TPC07

Inrush Current (5V Switch)



LTC1472 TPC08

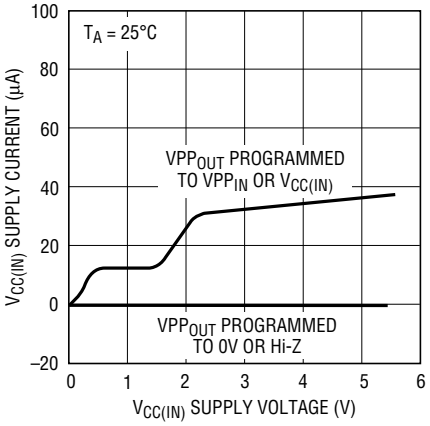
Inrush Current (3.3V Switch)



LTC1472 TPC09

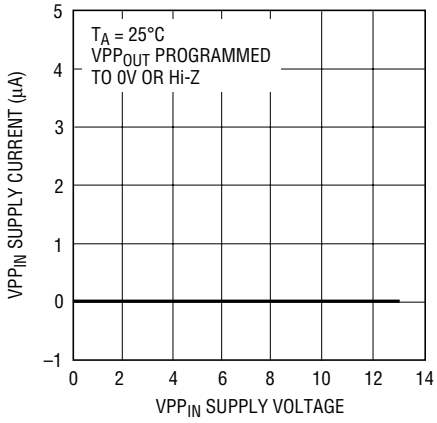
TYPICAL PERFORMANCE CHARACTERISTICS (VPP Section) V_{CC} EN0 = V_{CC} EN1 = 0V

$V_{CC(IN)}$ Supply Current (No Load)



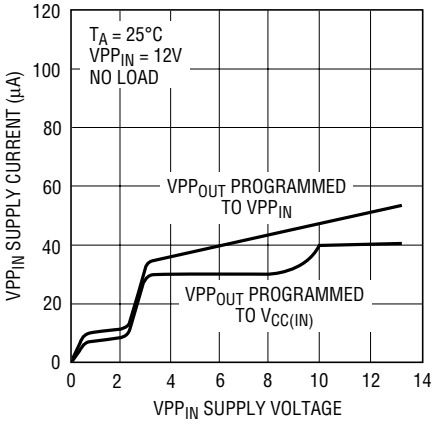
LTC1472 TPC10

VPP_{IN} Supply Current (OFF)



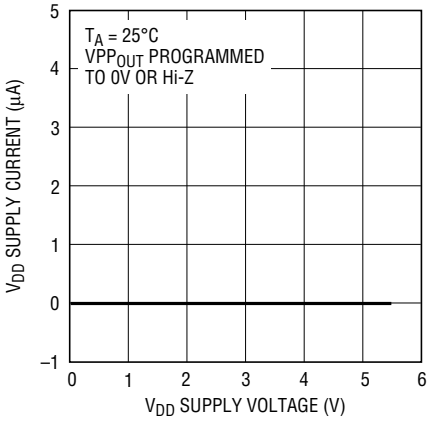
LTC1472 TPC11

VPP_{IN} Supply Current (No Load)



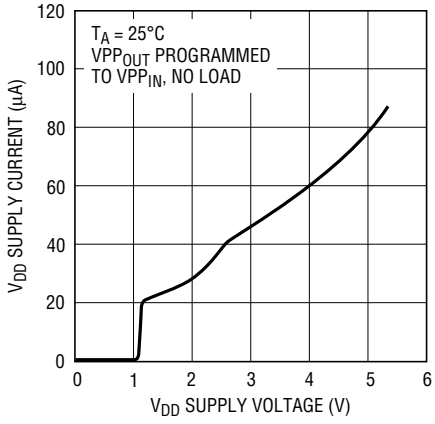
LTC1472 TPC12

V_{DD} Supply Current (OFF)



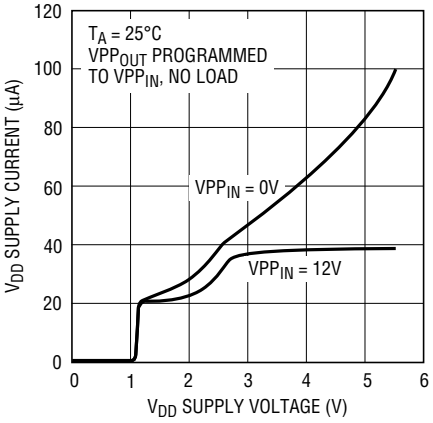
LTC1472 TPC13

V_{DD} Supply Current (No Load)



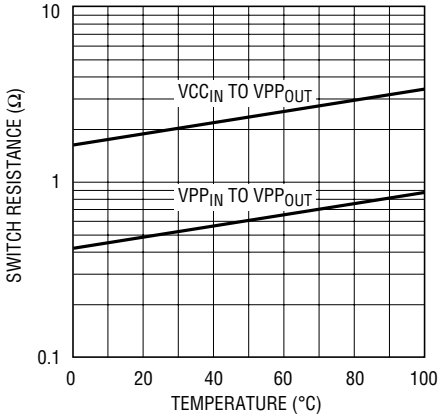
LTC1472 TPC14

V_{DD} Supply Current (ON)



LTC1472 TPC15

Switch Resistances



LTC1472 TPC16

PIN FUNCTIONS

Enable Input (Pins 3,4,7,8)

The two V_{CC} and two VPP Enable inputs are designed to interface directly with industry standard PCMCIA controllers. They are high impedance CMOS gates with ESD protection diodes to ground, and should not be forced above $5V_{IN}$ or below ground. Both sets of inputs have about 100mV of built-in hysteresis to ensure clean switching between operating modes.

Shutdown Output (Pin 6)

The LTC1472 is designed to operate *without* continuous 12V power. The gates of the V_{CC} NMOS switches are powered by charge pumps from the $5V_{IN}$ supply, and the gates of the VPP NMOS switches are powered by charge pumps powered from the V_{DD} supply when 12V is not present at the VPP_{IN} pin (see Application Information for more details). Therefore, the external 12V regulator can be shut down most of the time, and only turned on when programming the socket VPP pin to 12V.

The shutdown output is active high; i.e. the system 12V regulator is shut down when this output is held high and turned on when this output is held low.

VPP_{IN} Supply (Pin 5)

The VPP_{IN} supply pin serves two purposes. The first purpose is to provide power and gate drive for the VPP_{IN}-VPP_{OUT} switch. The second purpose is to provide optional 12V gate drive for the $V_{CC(IN)}$-VPP_{OUT} switch. If, however, this 12V power is not available, gate drive is obtained automatically from the 5V V_{DD} supply by an internal 5V to 12V charge pump converter.

V_{DD} Supply (Pin 9)

The V_{DD} pin provides power for the input, charge pump and control circuitry for the VPP section of the LTC1472 and therefore must be continuously powered. The standby quiescent current is typically 0.1µA when the VPP_{OUT} pin is programmed to 0V or Hi-Z and only rises to micropower levels when the VPP switches are active.

$V_{CC(IN)}$ Supply (Pin 12)

The $V_{CC(IN)}$ supply pin is typically connected directly to the $V_{CC(OUT)}$ pin from the V_{CC} switch section of the LTC1472. It can also be connected directly to a 3.3V or 5V power supply if desired. This supply pin does not provide any power to the internal control circuitry and is simply the input to the $V_{CC(IN)}$-VPP_{OUT} switch and therefore does not consume any power when unloaded or turned off.

$5V_{IN}$ Supply (Pin 2)

The $5V_{IN}$ supply pin serves two purposes. The first purpose is as the power supply input for the 5V NMOS switch. The second purpose is to provide power for the input, gate drive and protection circuitry for both the 3.3V and 5V V_{CC} switches, *this pin must be continuously powered*.

The enable inputs should be turned off (both asserted high or both asserted low) at least 100µs before the $5V_{IN}$ power is removed to ensure that both V_{CC} NMOS switch gates are fully discharged and both switches are in the high impedance mode.

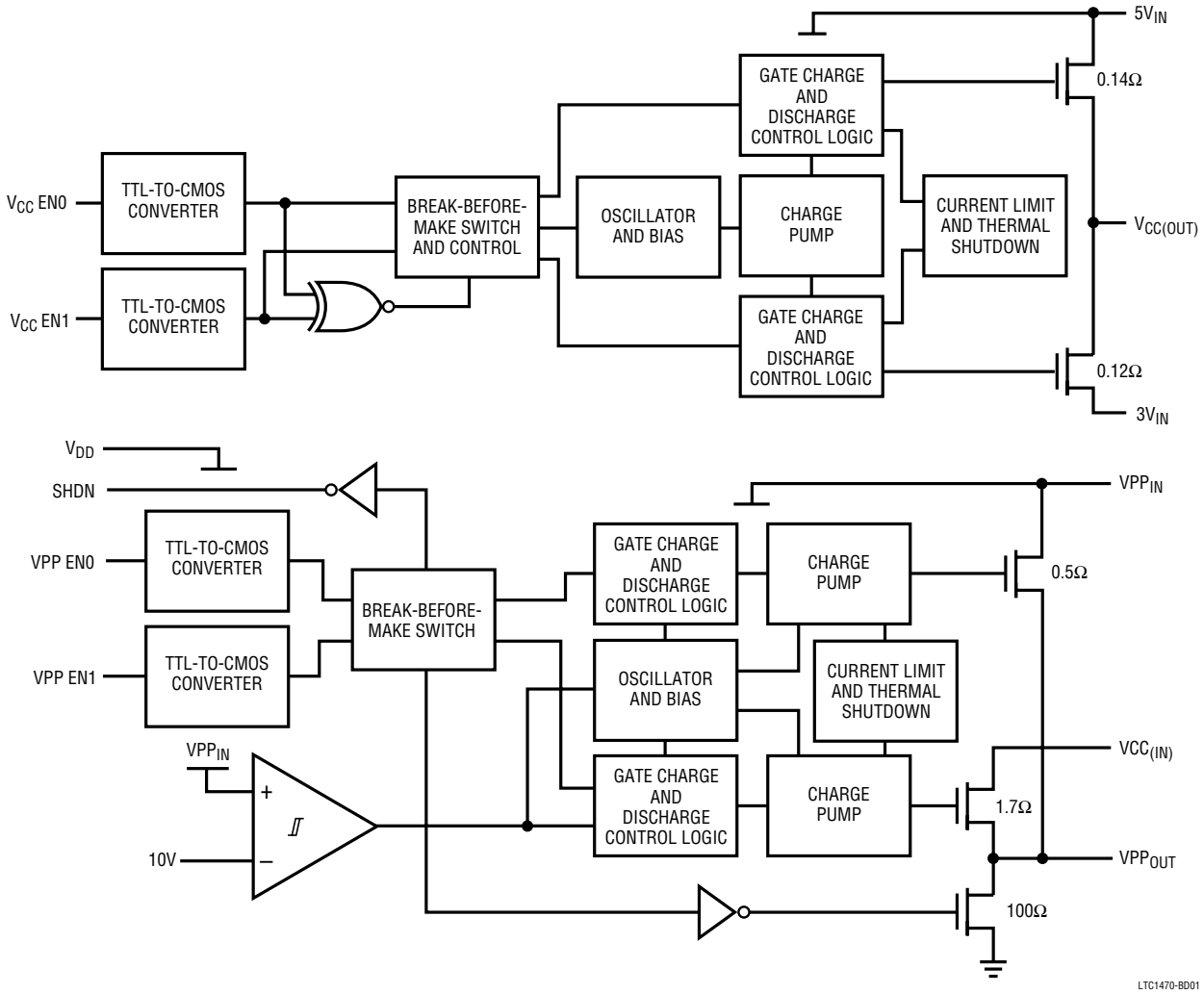
$3V_{IN}$ Supply (Pins 14,15)

The $3V_{IN}$ supply pin serves as the power supply input for the 3.3V switch. This pin does not provide any power to the internal control circuitry and therefore does not consume any power when unloaded or turned off.

$V_{CC(OUT)}$ and VPP_{OUT} Output (Pins 1,11,16)

The V_{CC} output of the LTC1472 is switched between the three operating states: OFF, 3.3V, and 5V. The VPP output is switched between four operating states: 0, V_{CC}, 12V and Hi-Z. Both pins are protected against accidental short-circuit conditions to ground by independent SafeSlot foldback current-limit circuitry which protects the socket, card and the system power supplies against damage. A second level of protection is provided by independent thermal shut down circuitry which protects each switch against overtemperature conditions.

BLOCK DIAGRAM



OPERATION

The LTC1472 protected switch matrix is designed to be a complete single slot solution for V_{CC} and VPP switching in a PCMCIA compatible card system. The LTC1472 consists of two independent functional sections: the V_{CC} switching section, and the VPP switching section.

THE V_{CC} SWITCHING SECTION

The V_{CC} switching section of the LTC1472 consist of the following functional blocks:

V_{CC} Switch Input TTL-CMOS Converters

The LTC1472 V_{CC} inputs are designed to accommodate a wide range of 3V and 5V logic families. The input threshold voltage is approximately 1.4V with approximately 100mV of hysteresis. The inputs enable the bias generator, the gate charge pumps and the protection circuity which are powered from the $5V_{IN}$ supply. Therefore, when the inputs are turned off, the entire circuit is powered down and the $5V_{IN}$ supply current drops below 1µA.

OPERATION

V_{CC} XOR Input Circuitry

The LTC1472 ensures that the 3.3V and 5V switches are never turned on at the same time by employing an XOR function which locks out the 3.3V switch when the 5V switch is turned on, and locks out the 5V switch when the 3.3V switch is turned on. This XOR function also makes it possible for the LTC1472 to work with either active-low or active-high PCMCIA V_{CC} switch control logic (see Applications Information for further details).

V_{CC} Break-Before-Make Switch Control

The LTC1472 has built-in delays to ensure that the 3.3V and 5V switch are non-overlapping. Further, the gate charge pumps include circuity which ramps the NMOS switches on slowly (400µs typical rise time) but turn off much more quickly (typically 10µs).

V_{CC} Bias, Oscillator and Gate Charge Pump

When either the 3.3V or 5V switch is enabled, a bias current generator and high frequency oscillator are turned on. An on-chip capacitive charge pump generates approximately 12V of gate drive for the internal low $R_{DS(ON)}$ NMOS V_{CC} switches from the $5V_{IN}$ power supply. Therefore, an external 12V supply is not required to switch the V_{CC} output. The $5V_{IN}$ supply current drops below 1µA when both switches are turned off.

V_{CC} Gate Charge and Discharge Control

Both V_{CC} switches are designed to ramp on slowly (400µs typical rise time). Turn off time is much quicker (typically 10µs).

To ensure that both V_{CC} NMOS switch gates are fully discharged, program the switch to the high impedance mode at least 100µs before turning off the $5V_{IN}$ power supply.

V_{CC} Switch Protection

Two levels of protection are designed into each of the power switches in the LTC1472. Both V_{CC} switches are protected against accidental short circuits with SafeSlot fold-back current limit circuits which limit the output current to typically 1A when the $V_{CC(OUT)}$ output is shorted to ground. Both switches also have independent thermal shutdown which limits the power dissipation to safe levels.

V_{CC} Switch Truth Table

V_{CC} EN0	V_{CC} EN1	$V_{CC(OUT)}$
0	0	OFF
1	0	5V
0	1	3.3V
1	1	OFF

THE VPP SWITCHING SECTION

The VPP switching section of the LTC1472 consists of the following functional blocks:

VPP Switch Input TTL-CMOS Converters

The VPP inputs are designed to accommodate a wide range of 3V and 5V logic families. The input threshold voltage is 1.4V with ≈ 100mV of hysteresis. The inputs enable the bias generator, the gate charge pumps and the protection circuitry. When the inputs are turned off, the entire circuit is powered down and the V_{DD} and VPP_{IN} supply currents drop below 1µA.

VPP Break-Before-Make Switch Control

The VPP input section has built-in delays to ensure that the VPP switchs are non-overlapping. Further, the gate charge pumps include circuitry which ramps the NMOS switches on slowly but turns them off quickly.

VPP Bias, Oscillator and Gate Charge Pump

When either the VPP_{IN}-VPP_{OUT} or $V_{CC(IN)}$-VPP_{OUT} switch is enabled, a bias current generator and high frequency oscillator are turned on. An on-chip capacitive charge pump generates approximately 23V of gate drive for the internal low $R_{DS(ON)}$ NMOS VPP_{IN}-VPP_{OUT} switch from the VPP_{IN} power supply. The gate of the $V_{CC(IN)}$-VPP_{OUT} NMOS switch is either powered by the external 12V regulator (if left on) or automatically from a built-in charge pump powered from the V_{DD} supply when the external 12V supply drops below 10V. The V_{DD} supply current drops below 1µA when switched to either the 0V or Hi-Z mode.

OPERATION

VPP Gate Charge and Discharge Control

The VPP switches are designed to ramp slowly (typically tens of µs) between output modes to reduce supply glitching when powering large capacitive loads.

VPP Switch Protection

Both VPP power switches are protected against accidental short circuits with SafeSlot fold-back current limit circuits which limit the short-circuit (0V) output current to typically 100mA when protecting the 12V VPP_{IN} supply and 60mA when protecting the $V_{CC(IN)}$ supply. (Higher operating currents are allowed at higher output voltages). Both switches also have thermal shutdown.

VPP Switch Truth Table

VPP EN0	VPP EN1	VPP_{OUT}
0	0	0V
0	1	$V_{CC(IN)}$
1	0	VPP_{IN}
1	1	Hi-Z

APPLICATIONS INFORMATION

The LTC1472 is a complete single slot V_{CC} and VPP power supply switch matrix with SafeSlot current limit protection on both outputs. It is designed to interface directly with industry standard PCMCIA card controllers and to industry standard 12V regulators.

Interfacing to the CL-PD6710 and the LT®1301

Figure 1 shows the LTC1472 interfaced to a standard PCMCIA slot controller and an LT1301 step-up switching regulator. The LTC1472 accepts logic control directly from the CL-PD6710 and in turn, controls the LT1301 to provide clean 12V VPP programming power when required. The LT1301 is then shutdown (10µA standby current) at all other times to conserve power.

The XOR V_{CC} input function allows the LTC1472 to interface directly to the active-low V_{CC} control outputs of the CL-PD6710 for 3.3V/5V voltage selection (see the V_{CC} Switch Truth Table). Therefore, no "glue" logic is required to interface to this PCMCIA compatible controller.

The LTC1472 provides SafeSlot current-limit protection for the LT1301 step-up regulator, the system 3.3V and 5V regulators, the socket and the card. Further, depending upon the system regulator's own current limits, it may allow the system power supplies to continue operation during a card/slot short circuit without losing data, etc.

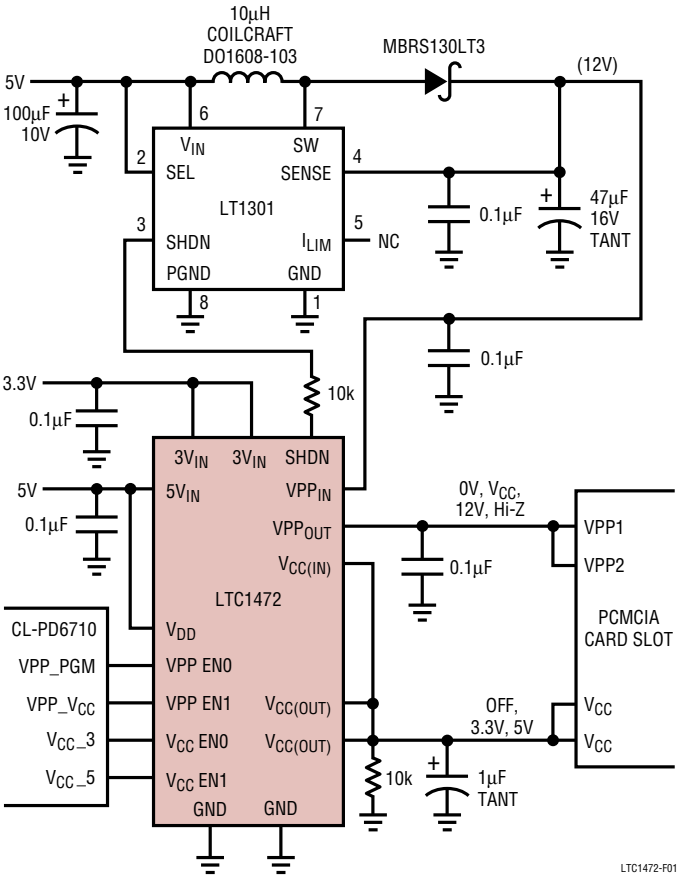


Figure 1. Direct Interface to Industry Standard PCMCIA Controller and LT1301 Step-Up Switching Regulator

APPLICATIONS INFORMATION

Interfacing to "365" Type Controllers

The LTC1472 also interfaces directly with "365" type controllers as shown in Figure 2. The V_{CC} Enable inputs are connected differently than to the CL-PD6710 controller because the "365" type controllers use active-high logic control of the V_{CC} switches (see the V_{CC} Switch Truth Table). No "glue logic" is required to interface to this type of PCMCIA compatible controller.

12V Power Requirements

Note that in Figure 2, a "local" 5V to 12V converter is not used. The LTC1472 works equally well with or without continuous 12V power. If the main power supply system has 12V continuously available, simply connect it to the VPP_{IN} pin. Internal circuitry automatically senses its presence and uses it to switch the internal VPP switches.

The 12V shutdown output can be used to shut down the system 12V power supply (if not required for any purpose other than VPP programming).

5V Power Requirements

The LTC1472 has been designed to operate without continuous 12V power, but continuous 5V power is required at the V_{DD} and $5V_{IN}$ supply pins for proper operation and should always be present when a card is powered (whether it is a 5V or 3.3V only card).

If the 5V power must be turned off, for example, to enter a 3.3V only full system "sleep" mode, the 5V supply must be turned off at least 100µs after the V_{CC} and VPP switches have been programmed to the Hi-Z or 0V states. This ensures that the gates of the NMOS switches are completely discharged.

Also, the V_{CC} switches cannot be operated properly without 5V power. They must be programmed to the off state at least 100µs prior to turning the 5V supply off, or they may be left in an indeterminate state.

Supply Bypassing

For best results, bypass the supply input pins with 1µF capacitors as close as possible to the LTC1472. Sometimes, much larger capacitors are already available at the outputs of the 3.3V, 5V and 12V power supply. In this case, it is still good practice to use 0.1µF capacitors as close as possible to the LTC1472, especially if the power supply output capacitors are more than 2" away on the printed circuit board.

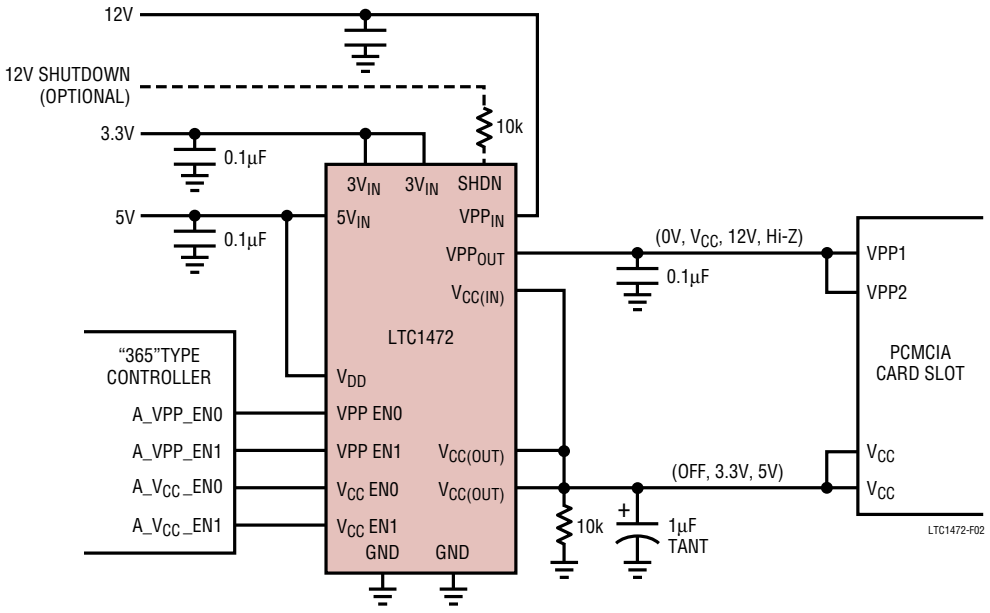


Figure 2. Direct Interface to Industry Standard PCMCIA Controller and LT1301 Step-Up Switching Regulator

APPLICATIONS INFORMATION

Output Capacitors

The $V_{CC(OUT)}$ pin is designed to ramp on slowly, typically 400µs rise time. Therefore, capacitors as large as 150µF can be driven without producing voltage spikes on the $5V_{IN}$ or $3V_{IN}$ supply pins (see graphs in Typical Performance Characteristics). The $V_{CC(OUT)}$ pin should have a 0.1µF to 1µF capacitor for noise reduction and smoothing.

The VPP_{OUT} pin should have a 0.01µF to 0.1µF capacitor for noise reduction. The VPP_{IN} capacitors should be at least equal to the VPP_{OUT} capacitors to ensure smooth transitions between output voltages without creating spikes on the system power supply lines.

Supply Sequencing

Because the 5V supply is the source of power for both the V_{CC} and VPP switch control logic, it is best to sequence the power supplies such that the 5V supply is powered before or simultaneous to the application of 3.3V or 12V power.

It is interesting to note however, that all of the switches in the LTC1472 are NMOS transistors which require charge pumps to generate gate voltages higher than the supply rails for full enhancement. Because the gate voltages start a 0V when the supplies are first activated, the switches always start in the off state and do not produce glitches at the output when powered.

Some PCMCIA switch matrix products employ PMOS switches for 12V VPP control and great care must be taken to ensure that the 5V control logic is powered before the 12V supply is turned on. If this sequence is not followed, the PMOS VPP switch gate may start at ground potential and the VPP output may be inadvertently forced to 12V.

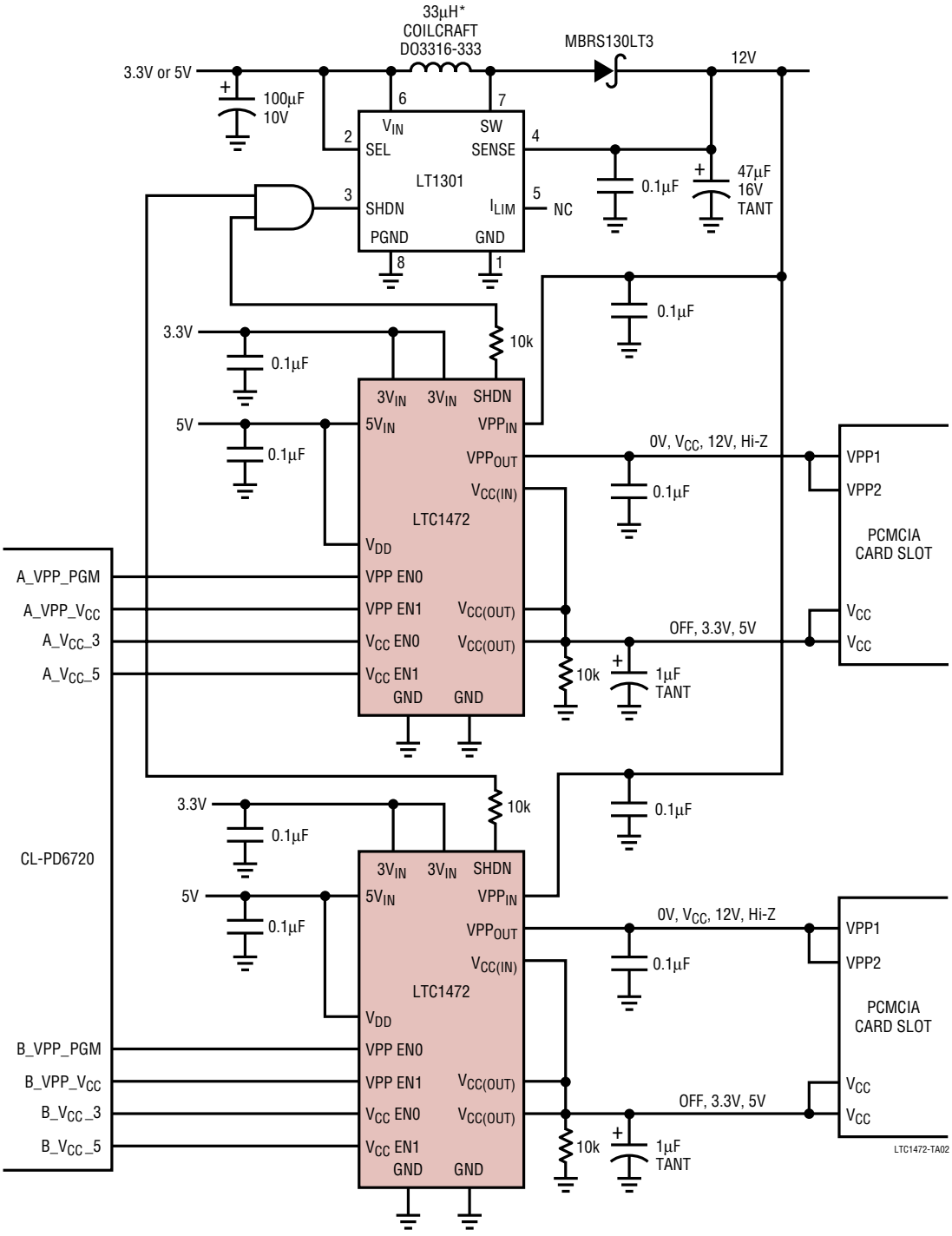
Although, not advisable, it is possible to power the 12V VPP_{IN} supply pin of the LTC1472 prior to application of 5V power. Only about 50µA flows to the VPP_{OUT} pin under these conditions.

If the 5V supply must be turned off, it is important to program all switches to the Hi-Z or 0V state at least 100µs before the 5V power is removed to ensure that all NMOS switch gates are fully discharged to 0V.

Whenever possible however, it is best to leave the $5V_{IN}$ and V_{DD} pins continuously powered. The LTC1472 quiescent current drops to <1µA with all the switches turned off and therefore no 5V power is consumed in the standby mode.

TYPICAL APPLICATIONS

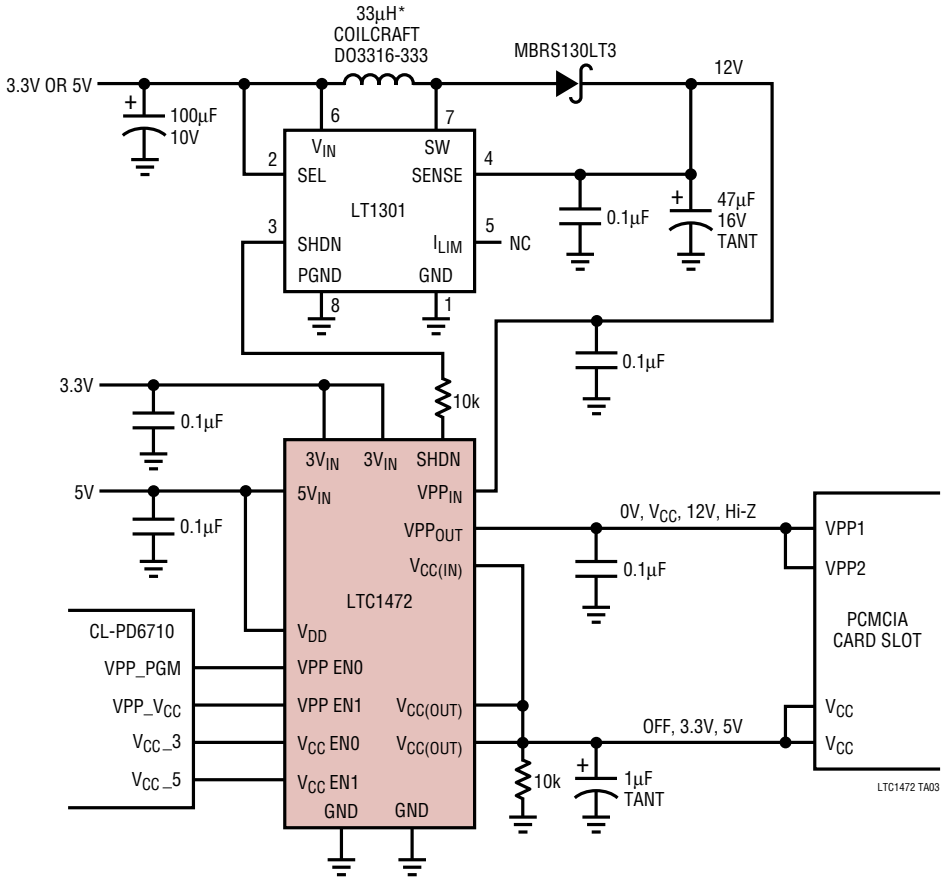
Dual Protected PCMCIA Power Management System



*FOR 5V TO 12V CONVERSION USE 10µH, COILCRAFT DO1608-103. SEE LT1301 DATA SHEET FOR MORE DETAILED INFORMATION ON INDUCTOR AND CAPACITOR SELECTION.

TYPICAL APPLICATIONS

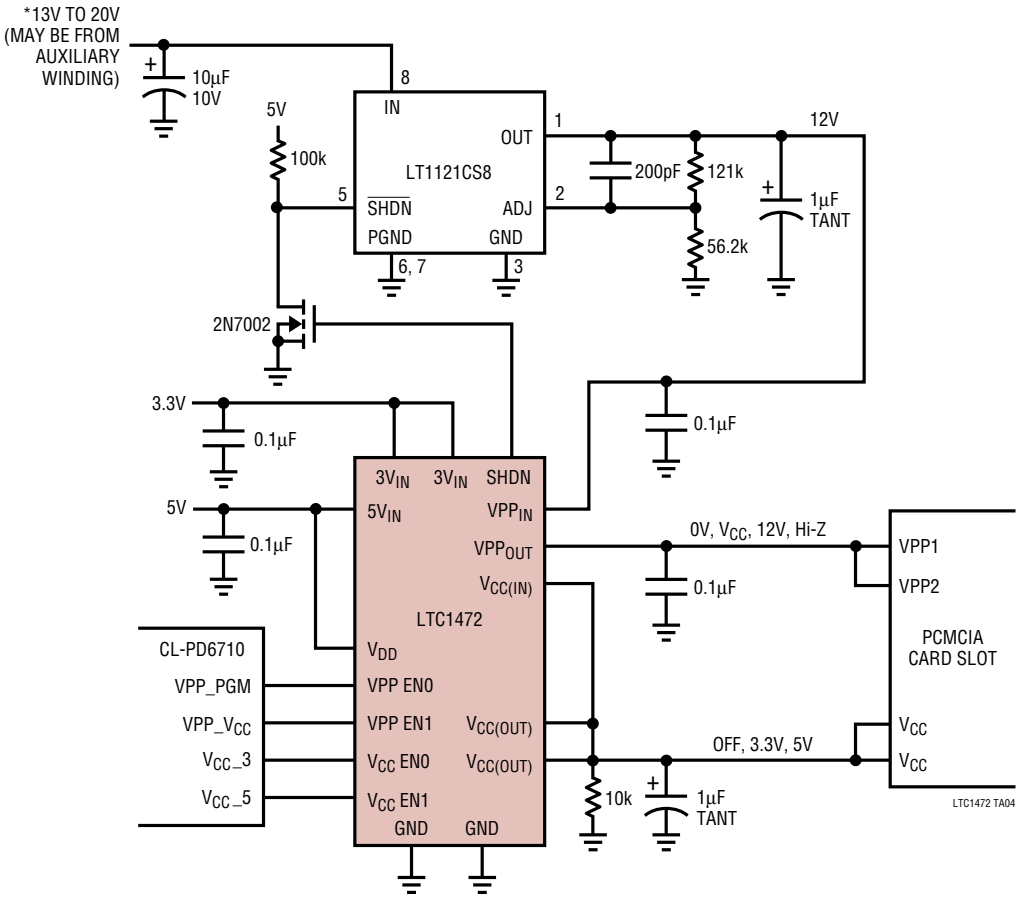
Single Protected PCMCIA Power Management System Using the LT1301 Powered from 3.3V or 5V



*FOR 5V TO 12V CONVERSION USE 10µH, COILCRAFT D01608-103. SEE LT1301 DATA SHEET FOR MORE DETAILED INFORMATION ON INDUCTION AND CAPACITOR SELECTION.

TYPICAL APPLICATIONS

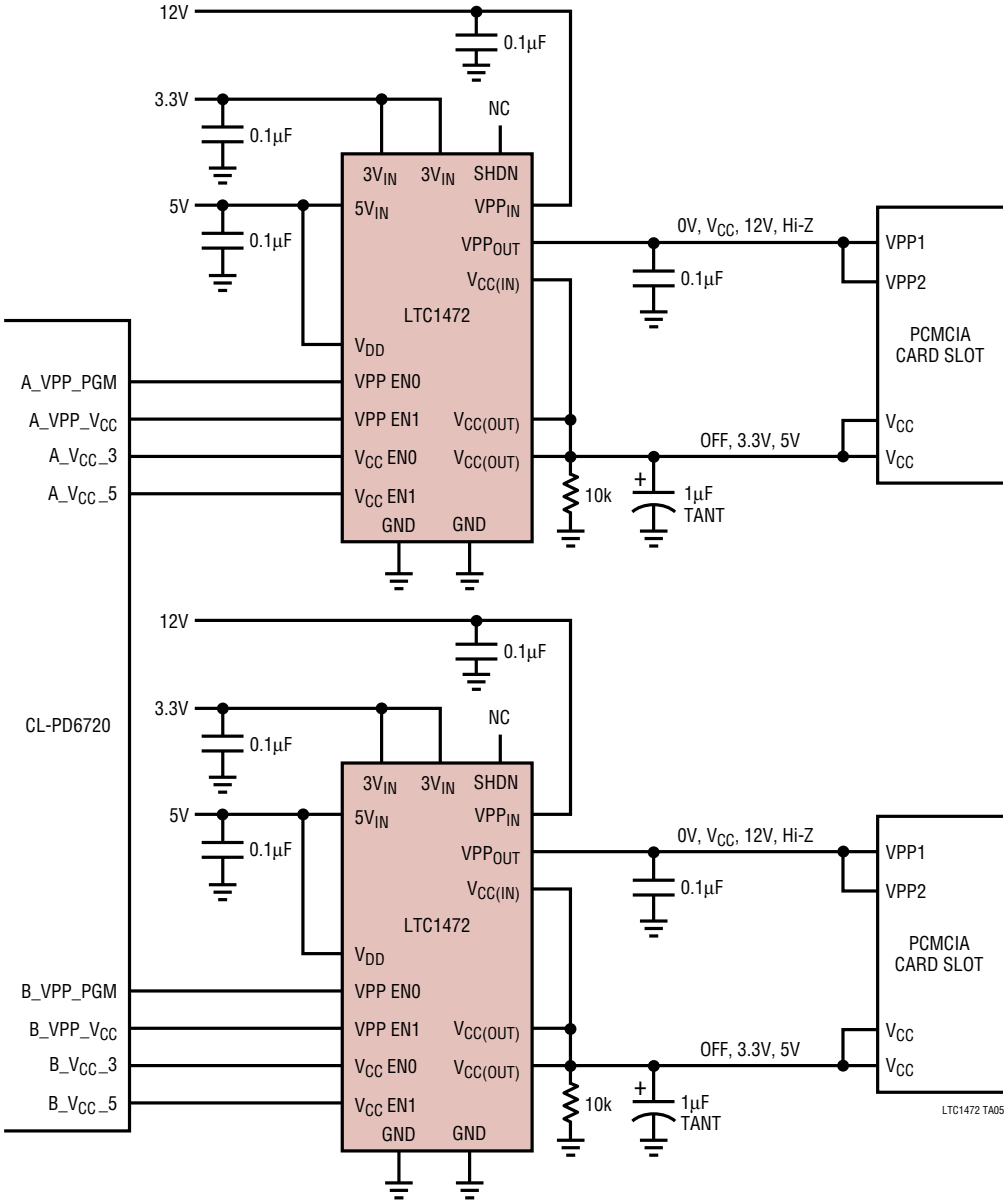
Single Protected PCMCIA Power Management System
Using the LT1121 Powered from an Auxiliary Winding for 12V VPP Power



*SEE THE LTC1142 DATA SHEET FOR AN EXAMPLE OF A 3.3V/5V DUAL REGULATOR WITH AUXILIARY WINDING 15V OUTPUT

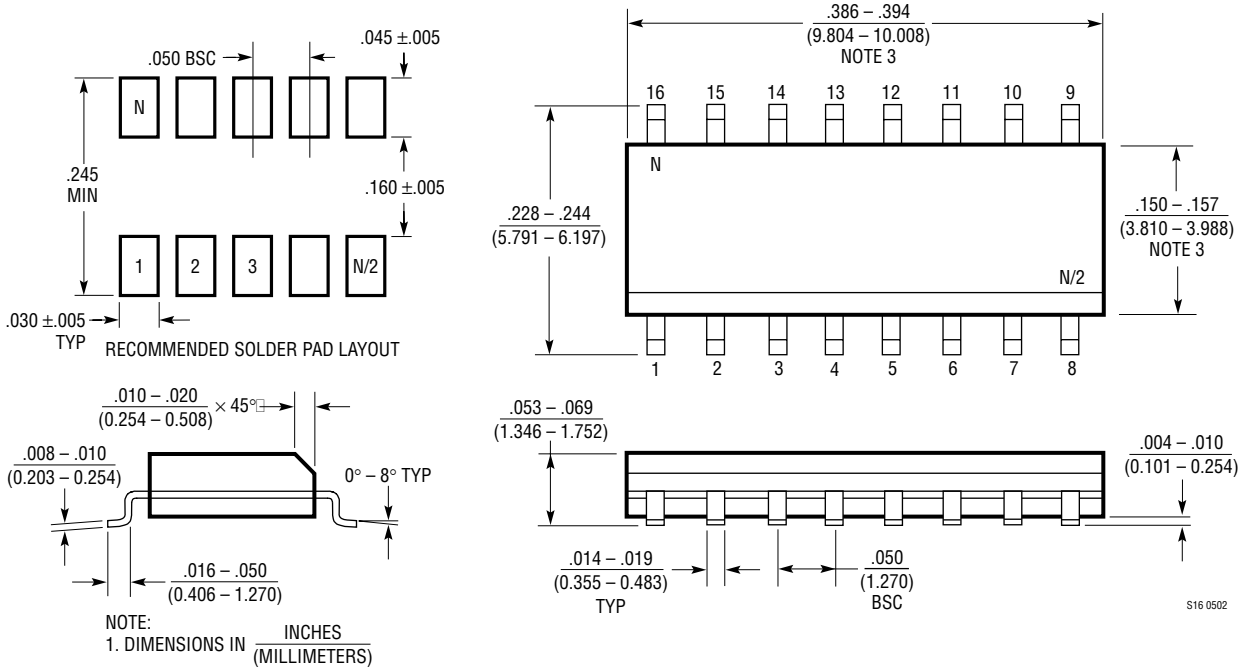
TYPICAL APPLICATIONS

Dual Protected PCMCIA Power Management System
Powered by System 12V Supply



PACKAGE DESCRIPTION

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3405/LTC3405A LTC3405A-1.5 LTC3405A-1.8	300mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN} = 2.7V to 6V, V_{OUT} = 0.8V, I_Q = 20µA I_{SD} = <1µA, ThinSOT Package
LTC3406/LTC3406B	600mA (I_{OUT}) 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.5V to 5.5V, V_{OUT} = 0.6V, I_Q = 20µA I_{SD} = <1µA, ThinSOT Package
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 60µA I_{SD} = <1µA, MS10 Package
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 60µA I_{SD} = <1µA, TSSOP16E Package
LTC3413	3A (I_{OUT}), Sink/Source, 2MHz, Monolithic Synchronous Regulator for DDR/QDR Memory Termination	90% Efficiency, V_{IN} = 2.25V to 5.5V, V_{OUT} = $V_{REF/2}$, I_Q = 280µA I_{SD} = <1µA, TSSOP16E Package
LT3430	60V, 2.75A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN} = 5.5V to 60V, V_{OUT} = 1.20V, I_Q = 2.5mA I_{SD} = 25µA, TSSOP16E Package
LTC3440	600mA (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN} = 2.5V to 5.5V, V_{OUT} = 2.5V, I_Q = 25µA I_{SD} = <1µA, MS Package

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