

LTC1326/LTC1326-2.5

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Terminal Voltage

V_{CC3} , V_{CC5} , V_{CC25} , V_{CCA}	–0.5V to 7V
$\overline{RST}$, $\overline{SRST}$	–0.5V to 7V
$\overline{RST}$	–0.5V to ($V_{CC3} + 0.3V$)
$\overline{PBR}$	–7V to 7V

Operating Temperature Range

LTC1326C/LTC1326C-2.5	0°C to 70°C
LTC1326I/LTC1326I-2.5	–40°C to 85°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 250^{\circ}C/W$		TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$	
ORDER PART NUMBER	MS8 PART NUMBER	ORDER PART NUMBER	S8 PART NUMBER
LTC1326CMS8 LTC1326IMS8	LTBA LTUH	LTC1326CS8 LTC1326IS8	1326 1326I
TOP VIEW MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 250^{\circ}C/W$		TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$	
ORDER PART NUMBER	MS8 PART NUMBER	ORDER PART NUMBER	S8 PART NUMBER
LTC1326CMS8-2.5 LTC1326IMS8-2.5	LTEK LTUJ	LTC1326CS8-2.5 LTC1326IS8-2.5	132625 326I25
Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: http://www.linear.com/leadfree/			

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC3} = 3.3\text{V}$, $V_{CC5} = 5\text{V}$ (for LTC1326), $V_{CC25} = 2.5\text{V}$ (for LTC1326-2.5), $V_{CCA} = V_{CC3}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RT3}	Reset Threshold V_{CC3}	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	3.094	3.118	3.135	V
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	3.052	3.118	3.143	V
V_{RT5}	Reset Threshold V_{CC5} (LTC1326)	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	4.687	4.725	4.750	V
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	4.625	4.725	4.762	V
V_{RT25}	Reset Threshold V_{CC25} (LTC1326-2.5)	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	2.344	2.363	2.375	V
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	2.312	2.363	2.381	V
V_{RTA}	Reset Threshold V_{CCA}	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	0.992	1.000	1.007	V
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.980	1.000	1.007	V
V_{CC}	V_{CC3} Operating Voltage	$\overline{\text{RST}}$ in Correct Logic State	●	1		7	V
I_{VCC3}	V_{CC3} Supply Current	$\overline{\text{PBR}} = V_{CC3}$	●		20	40	μA
I_{VCC5}	V_{CC5} Input Current (LTC1326)	$V_{CC5} = 5\text{V}$	●		4	10	μA
I_{VCC25}	V_{CC25} Input Current (LTC1326-2.5)	$V_{CC25} = 2.5\text{V}$	●		2.8	7	μA
I_{VCCA}	V_{CCA} Input Current	$V_{CCA} = 1\text{V}$	●	-15	0	15	nA
t_{RST}	Reset Pulse Width	$\overline{\text{RST}}$ Low with $10\text{k}\Omega$ Pull-Up to V_{CC3}					
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	140	200	280	ms
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	140	200	300	ms
t_{SRST}	Soft Reset Pulse Width	$\overline{\text{SRST}}$ Low with $10\text{k}\Omega$ Pull-Up to V_{CC3}	●	50	100	200	μs
t_{UV}	V_{CC} Undervoltage Detect to $\overline{\text{RST}}$	V_{CC25} , V_{CC3} or V_{CCA} Less Than Reset Threshold V_{RT} by More Than 1%			13		μs
I_{PBR}	$\overline{\text{PBR}}$ Pull-Up Current	$\overline{\text{PBR}} = 0\text{V}$					
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	3	7	10	μA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	3	7	15	μA
V_{IL}	$\overline{\text{PBR}}$, $\overline{\text{RST}}$ Input Low Voltage		●			0.8	V
V_{IH}	$\overline{\text{PBR}}$, $\overline{\text{RST}}$ Input High Voltage		●	2			V
t_{PW}	$\overline{\text{PBR}}$ Min Pulse Width		●	40			ns
t_{DB}	$\overline{\text{PBR}}$ Debounce	Deassertion of $\overline{\text{PBR}}$ Input to $\overline{\text{SRST}}$ Output ($\overline{\text{PBR}}$ Pulse Width = $1\mu\text{s}$)	●		20	35	ms
t_{PB}	$\overline{\text{PBR}}$ Assertion Time for Transition from Soft to Hard Reset Mode	$\overline{\text{PBR}}$ Held Less Than V_{IL}					
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	1.4	2.0	2.8	s
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	1.4	2.0	3.0	s
V_{OL}	RST Output Voltage Low	$I_{\text{SINK}} = 5\text{mA}$	●		0.15	0.4	V
		$I_{\text{SINK}} = 100\mu\text{A}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●		0.05	0.4	V
			●		0.05	0.4	V
			●		0.05	0.4	V
		$I_{\text{SINK}} = 100\mu\text{A}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●		0.05	0.4	V
			●		0.05	0.4	V
			●		0.05	0.4	V
		$I_{\text{SINK}} = 100\mu\text{A}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●		0.05	0.4	V
			●		0.05	0.4	V
			●		0.05	0.4	V
		$I_{\text{SINK}} = 100\mu\text{A}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●		0.05	0.4	V
	$\overline{\text{SRST}}$ Output Voltage Low	$I_{\text{SINK}} = 2.5\text{mA}$	●		0.15	0.4	V
	RST Output Voltage Low	$I_{\text{SINK}} = 2.5\text{mA}$	●		0.15	0.4	V

LTC1326/LTC1326-2.5

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. LTC1326 Only $V_{CC3} = 3.3\text{V}$, $V_{CC5} = 5\text{V}$, $V_{CCA} = V_{CC3}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH}	$\overline{\text{RST}}$ Output Voltage High (Note 3)	$I_{\text{SOURCE}} = 1\mu\text{A}$	● $V_{CC3} - 1$			V
	$\overline{\text{SRST}}$ Output Voltage High (Note 3)	$I_{\text{SOURCE}} = 1\mu\text{A}$	● $V_{CC3} - 1$			V
	$\overline{\text{RST}}$ Output Voltage High	$I_{\text{SOURCE}} = 600\mu\text{A}$	● $V_{CC3} - 1$			V
t_{PHL}	Prop Delay $\overline{\text{RST}}$ to $\overline{\text{RST}}$ High Input to Low Output	$C_{\text{RST}} = 20\text{pF}$		25		ns
t_{PLH}	Prop Delay $\overline{\text{RST}}$ to $\overline{\text{RST}}$ Low Input to High Output	$C_{\text{RST}} = 20\text{pF}$		45		ns
V_{OVR}	V_{CC5} Reset Override Voltage	Override V_{CC5} Ability to Assert $\overline{\text{RST}}$ (Note 4)		$V_{CC3} \pm 0.025$		V

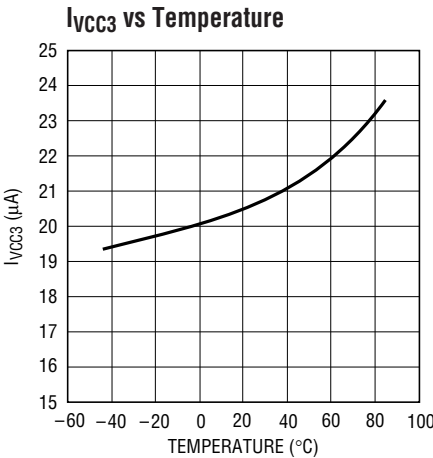
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

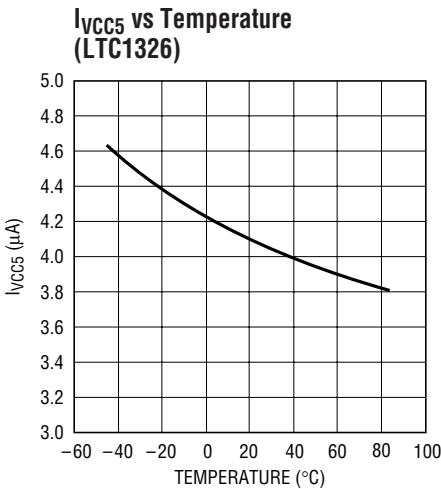
Note 3: The output pins $\overline{\text{SRST}}$ and $\overline{\text{RST}}$ have weak internal pull-ups to V_{CC3} of $6\mu\text{A}$ typ. However, external pull-up resistors may be used when faster rise times are required.

Note 4: The V_{CC5} reset override voltage is valid for an operating range less than approximately 4.15V . Above this point the override is turned off and the V_{CC5} pin functions normally.

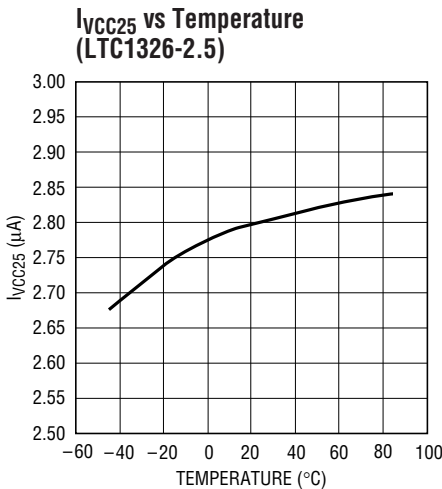
TYPICAL PERFORMANCE CHARACTERISTICS



1326/2.5 G01

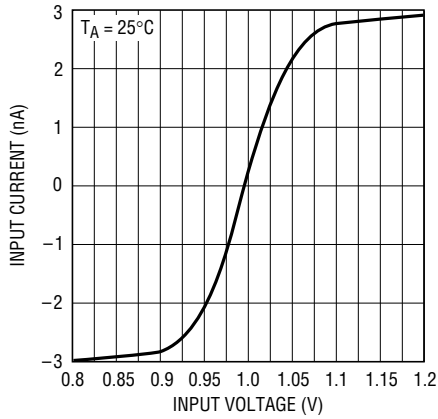


1326/2.5 G02

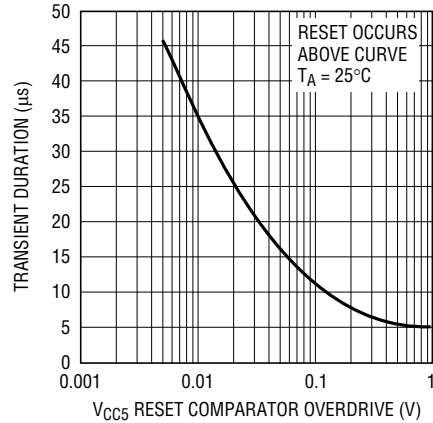


1326/2.5 G03

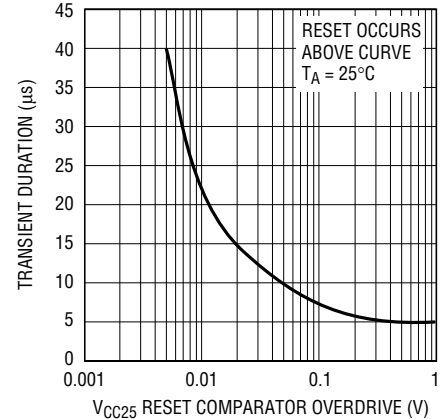
TYPICAL PERFORMANCE CHARACTERISTICS

 V_{CCA} Input Current vs Input Voltage

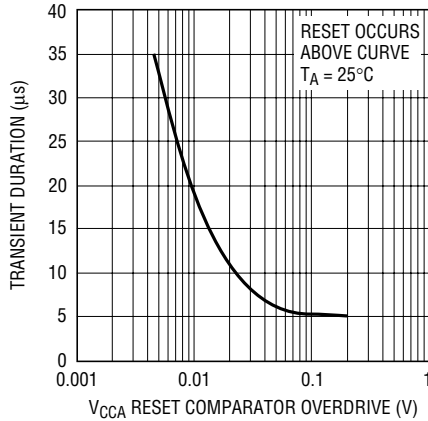
1326/2.5 G04

 V_{CC5} Transient Immunity (LTC1326)

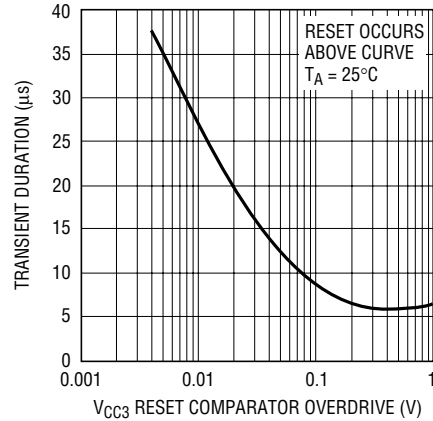
1326/2.5 G05

 V_{CC25} Transient Immunity (LTC1326-2.5)

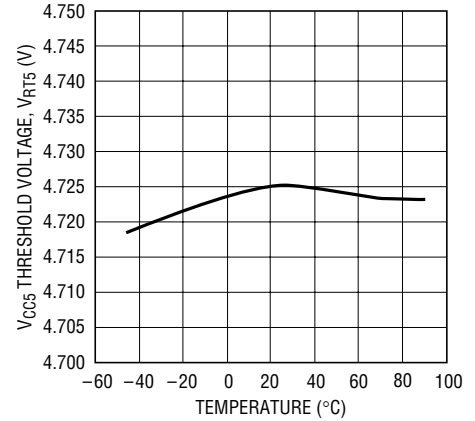
1326/2.5 G06

 V_{CCA} Transient Immunity

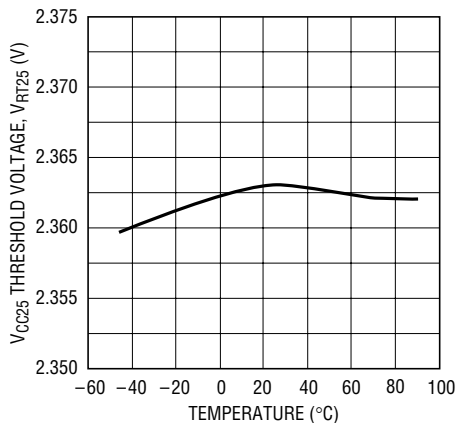
1326/2.5 G07

 V_{CC3} Transient Immunity

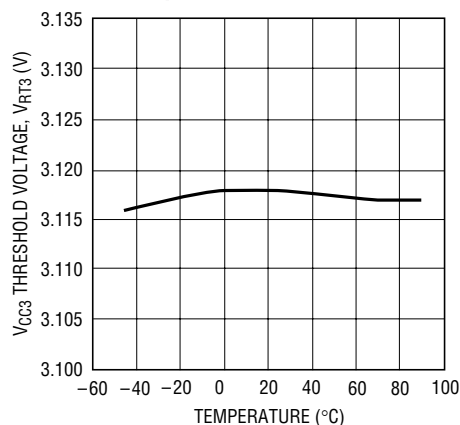
1326/2.5 G08

 V_{CC5} Threshold Voltage vs Temperature (LTC1326)

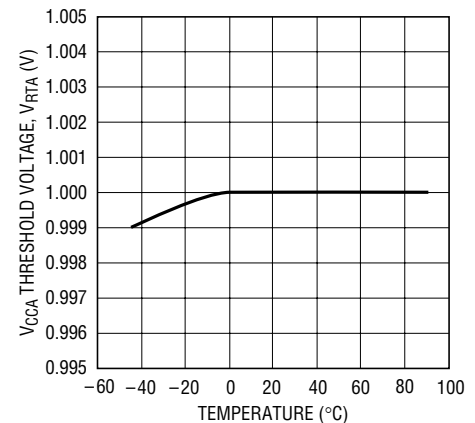
1326/2.5 G09

 V_{CC25} Threshold Voltage vs Temperature (LTC1326-2.5)

1326/2.5 G10

 V_{CC3} Threshold Voltage vs Temperature

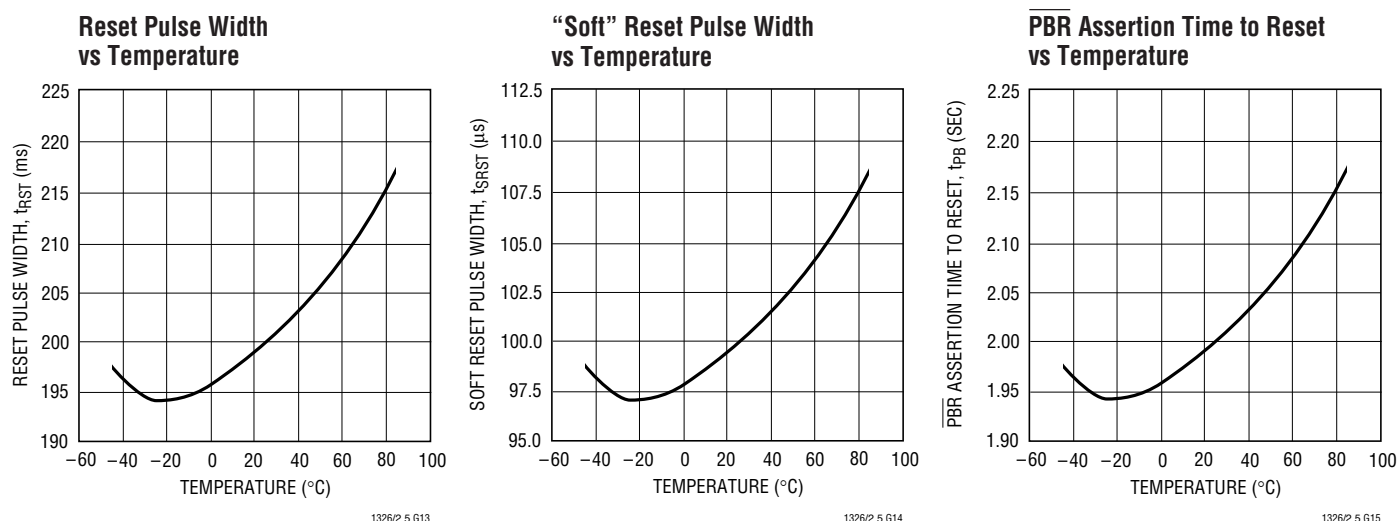
1326/2.5 G11

 V_{CCA} Threshold Voltage vs Temperature

1326/2.5 G12

132625fc

TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

V_{CC3} (Pin 1): 3.3V Sense Input and Power Supply Pin for the IC. Bypass to ground with $\geq 0.1\mu\text{F}$ ceramic capacitor.

V_{CC5} (Pin 2) (LTC1326): 5V Sense Input. Used as gate drive for the $\overline{\text{RST}}$ output FET when the voltage on V_{CC3} is less than the voltage on V_{CC5}. If unused, it can be tied to V_{CC3} (see Dual and Single Supply Monitor Operation in the Applications Information section).

V_{CC25} (Pin 2) (LTC1326-2.5): 2.5V Sense Input. Used as gate drive for $\overline{\text{RST}}$ output FET when the voltage on V_{CC3} is less than the voltage on V_{CC25}. If unused, it can be tied to V_{CC3}.

V_{CCA} (Pin 3): 1V Sense, High Impedance Input. Can be used as a logic input with a 1V threshold. If unused, it can be tied to either V_{CC3} or V_{CC25}.

GND (Pin 4): Ground.

RST (Pin 5): Reset Logic Output. Active high CMOS logic output, drives high to V_{CC3}, buffered complement of $\overline{\text{RST}}$. An external pull-down on the $\overline{\text{RST}}$ pin will drive this pin high.

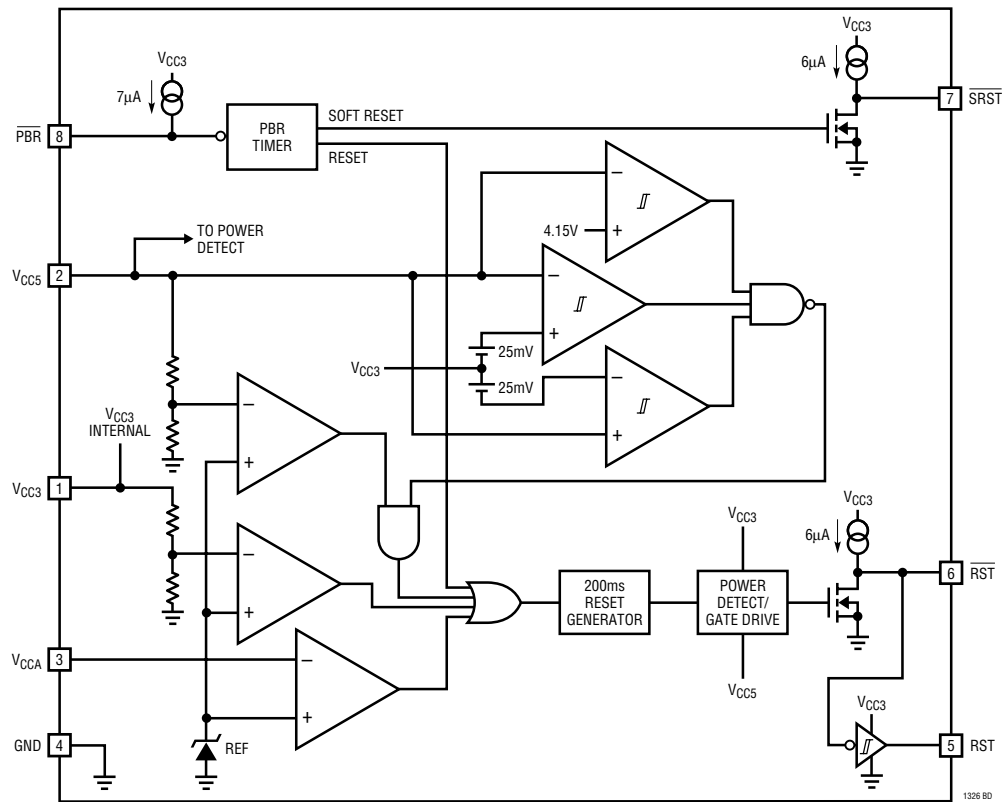
$\overline{\text{RST}}$ (Pin 6): Reset Logic Output. Active low, open-drain logic output with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. Asserted when one or more of the supplies are below trip thresholds and held for 200ms after all supplies become valid. Also asserted after PBR is held low for more than 2 seconds and for an additional 200ms after PBR is released.

SRST (Pin 7): Soft Reset. Active low, open-drain logic output with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. Asserted for 100μs after PBR is held low for less than 2 seconds and released.

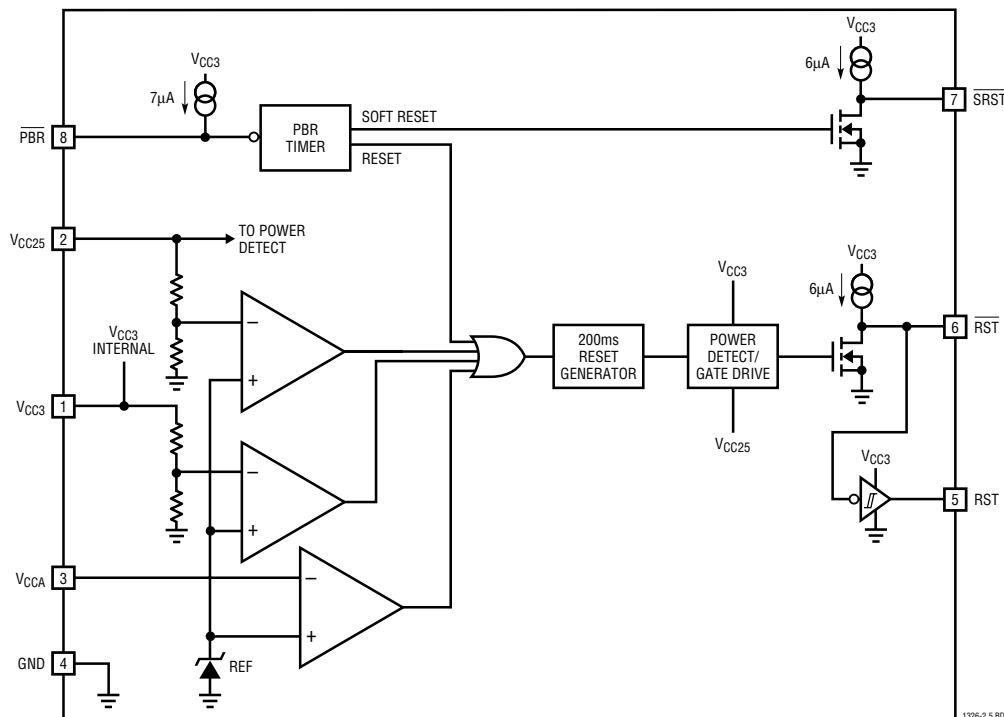
PBR (Pin 8): Push-Button Reset. Active low logic input with weak pull-up to V_{CC3}. Can be pulled up greater than V_{CC3} when interfacing to 5V logic. When asserted for less than 2 seconds, outputs a soft reset 100μs pulse on the SRST pin. When PBR is asserted for greater than 2 seconds, the $\overline{\text{RST}}$ output is forced low and remains low until 200ms after PBR is released.

BLOCK DIAGRAMS

LTC1326

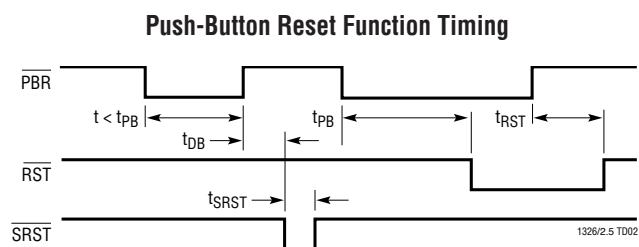
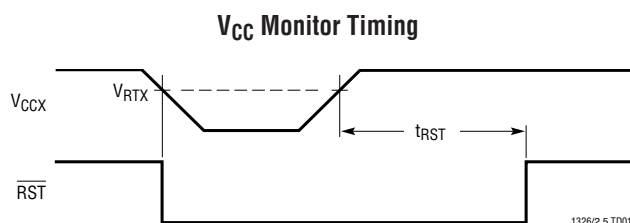


LTC1326-2.5



132625fc

TIMING DIAGRAMS



APPLICATIONS INFORMATION

Operation

The LTC1326/LTC1326-2.5 are micropower, high accuracy triple supply monitoring circuits. The parts have two basic functions: generation of a reset when power supplies are out of range, and generation of reset or a “soft” reset when the $\overline{\text{PBR}}$ pin is pulled low.

Supply Monitoring

All three V_{CC} inputs must be above predetermined thresholds for 200ms before the reset output is released. The parts will assert reset during power-up, power-down and brownout conditions on any one or more of the V_{CC} inputs.

On power-up, either the $V_{\text{CC}5}$ or $V_{\text{CC}3}$ pin on the LTC1326, or the $V_{\text{CC}25}$ or $V_{\text{CC}3}$ pin on the LTC1326-2.5, can power the drive circuits for the $\overline{\text{RST}}$ pin. This ensures that $\overline{\text{RST}}$ will be low when $V_{\text{CC}5}$, $V_{\text{CC}25}$ or $V_{\text{CC}3}$ reaches 1V. As long as any one of the V_{CC} inputs is below its predetermined threshold, $\overline{\text{RST}}$ will stay a logic low. Once all of the V_{CC} inputs rise above their thresholds, an internal timer is started and $\overline{\text{RST}}$ is released after 200ms. The $\overline{\text{RST}}$ pin outputs the inverted state of what is seen on $\overline{\text{RST}}$ pin.

$\overline{\text{RST}}$ is reasserted whenever any one of the V_{CC} inputs drops below its predetermined threshold and remains asserted until 200ms after all of the V_{CC} inputs are above their thresholds.

On power-down, once any of the V_{CC} inputs drop below its threshold, $\overline{\text{RST}}$ is held at a logic low. A logic low of 0.4V is guaranteed until $V_{\text{CC}3}$ and $V_{\text{CC}5}$ on the LTC1326 or $V_{\text{CC}3}$ and $V_{\text{CC}25}$ on the LTC1326-2.5 drop below 1V.

The three internal precision voltage comparators have response times that are typically 13 μ s. This slow response time helps prevent mistriggering due to transients on each of the V_{CC} inputs. The part's ability to suppress transients can be improved by bypassing each of the V_{CC} inputs with a 0.1 μ F capacitor to ground.

Push-Button Reset

The parts provide a push-button reset input pin. The $\overline{\text{PBR}}$ input has an internal pull-up current source to $V_{\text{CC}3}$. If the $\overline{\text{PBR}}$ pin is not used it can be left floating.

When the $\overline{\text{PBR}}$ is pulled low for less than t_{PB} (≈ 2 sec), a narrow (100 μ s typ) soft reset pulse is generated on the $\overline{\text{SRST}}$ output pin after the button is released. The push-button circuitry contains an internal debounce counter which delays the output of the soft reset pulse by typically 20ms. This pin can be OR-tied to the $\overline{\text{RST}}$ pin and issue what is called a “soft” reset. The $\overline{\text{SRST}}$ thereby resets the microprocessor without interrupting the DRAM refresh cycle. In this manner DRAM information remains undisturbed. Alternatively, $\overline{\text{SRST}}$ may be monitored by the processor to initiate a software-controlled reset.

When the $\overline{\text{PBR}}$ pin is held low for longer than t_{PB} (≈ 2 sec), a standard reset is generated on the $\overline{\text{RST}}$ and $\overline{\text{RST}}$ pins. Once the 2 second period has elapsed, a reset signal is produced by the push-button logic, thereby clearing the reset counter. Once the button is released, the reset counter begins counting the reset period (200ms nominal). Consequently, the reset outputs remain asserted for approximately 200ms after the button is released.

APPLICATIONS INFORMATION

During a supply induced reset condition, the ability of the PBR pin to force a soft reset condition on the SRST pin is disabled. In other words $\overline{\text{SRST}}$ will remain high. If the PBR pin is held low, both during and after a supply induced reset (low $\overline{\text{RST}}$), the $\overline{\text{RST}}$ pin will remain low until 200ms after the PBR goes high.

Power Detect/Gate Drive

The LTC1326/LTC1326-2.5 for the most part are powered internally from the V_{CC3} pin. The exception is at the gate drive of the output FET on the $\overline{\text{RST}}$ pin. On the input to this FET is power detection circuitry used to detect and drive the gate from either the 3.3V input pin (V_{CC3}) or the 5V input pin (V_{CC5}) on the LTC1326 or the 2.5V input pin (V_{CC25}) on the LTC1326-2.5. The gate drive is derived from the pin with the highest potential. This ensures the part pulls the $\overline{\text{RST}}$ pin low as soon as either input pin is $\geq 1\text{V}$.

Dual and Single Supply Monitor Operation

The V_{CC3} , V_{CC5} and V_{CCA} inputs may be individually disabled by the following override techniques which allow the LTC1326 or LTC1326-2.5 to be used as a dual or single supply monitor.

LTC1326 Override Functions

The V_{CCA} pin, if unused, can be tied to either V_{CC3} or V_{CC5} . This is an obvious solution since the trip points for V_{CC3} and V_{CC5} will always be greater than the trip point for V_{CCA} .

The V_{CC5} input trip point is disabled if its voltage is equal to the voltage on $V_{\text{CC3}} \pm 25\text{mV}$ and the voltage on V_{CC5} is less than 4.15V. In this manner, the part will behave as a 3.3V monitor and the V_{CC5} reset will be disabled.

The V_{CC5} trip point is reenabled when the voltage on V_{CC5} is equal to the voltage on $V_{\text{CC3}} \pm 25\text{mV}$ and the two inputs are greater than approximately 4.15V. In this manner, the LTC1326 can function as a 5V monitor with the 3.3V monitor disabled.

When monitoring either 3.3V or 5V with V_{CC3} strapped to V_{CC5} (see Figure 1), the LTC1326 determines which is the

appropriate range. The LTC1326 handles this situation as shown in Figure 2. Above 1V and below V_{RT3} , $\overline{\text{RST}}$ is held low. From V_{RT3} to approximately 4.15V, the LTC1326 assumes 3.3V supply monitoring and $\overline{\text{RST}}$ is deasserted. Above approximately 4.15V, the LTC1326 operates as a 5V monitor. In most systems, the 5V supply will pass through the 3.1V to 4.15V region in <200ms during power-up, and the $\overline{\text{RST}}$ output will behave as desired. Table 1 summarizes the state of $\overline{\text{RST}}$ and $\overline{\text{RST}}$ at various operating voltages with $V_{\text{CC3}} = V_{\text{CC5}}$.

Table 1. Override Truth Table ($V_{\text{CC3}} = V_{\text{CC5}}$)

INPUTS ($V_{\text{CC3}} = V_{\text{CC5}} = V_{\text{CC}}$)	$\overline{\text{RST}}$	$\overline{\text{RST}}$
$0\text{V} \leq V_{\text{CC}} \leq 1\text{V}$	—	—
$1\text{V} \leq V_{\text{CC}} \leq V_{\text{RT3}}$	0	1
$V_{\text{RT3}} \leq V_{\text{CC}} \leq 4.15\text{V}$	1	0
$4.15\text{V} \leq V_{\text{CC}} \leq V_{\text{RT5}}$	0	1
$V_{\text{RT5}} \leq V_{\text{CC}}$	1	0

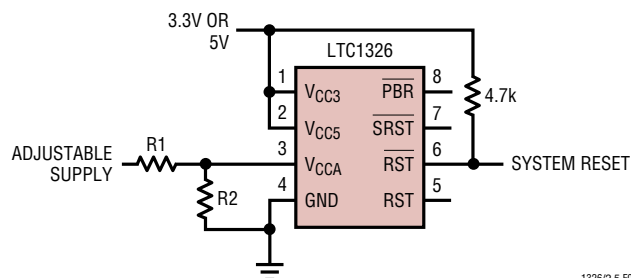


Figure 1

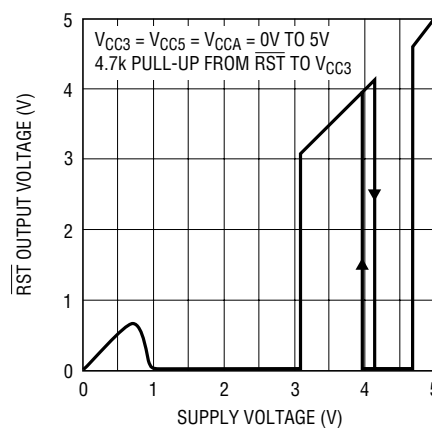


Figure 2. $\overline{\text{RST}}$ Voltage vs Supply Voltage

APPLICATIONS INFORMATION

Figure 3 contains a simple circuit for 5V systems that can't risk the $\overline{\text{RST}}$ output going high in the 3.1V to 4.15V range (possibly due to very slow rise time on the 5V supply). Diode D1 powers the LTC1326 while dropping $\approx 0.6\text{V}$ from the V_{CC5} pin to the V_{CC3} pin. This prevents the part's internal override circuit from being activated. Without the override circuit active, the $\overline{\text{RST}}$ pin stays low until V_{CC5} reaches $V_{\text{RT5}} \equiv 4.725\text{V}$ (See Figure 4).

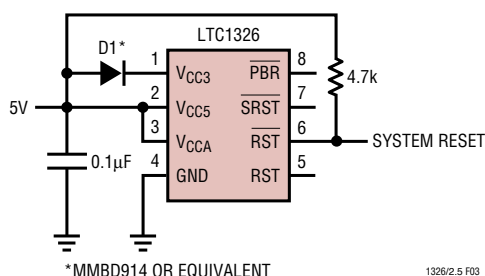


Figure 3. LTC1326 Monitoring a Single 5V Supply. D1 Used to Avoid $\overline{\text{RST}}$ High Near 3.3V to 4V (See Figure 2).

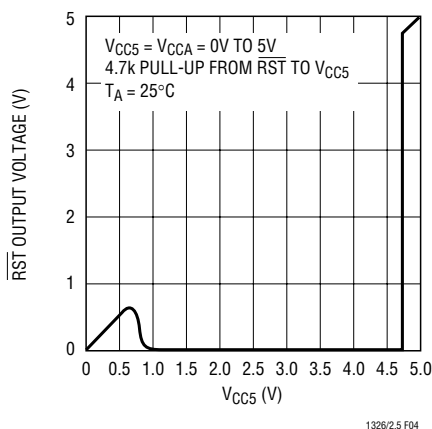


Figure 4. $\overline{\text{RST}}$ Output Voltage Characteristics of the Circuit in Figure 3

LTC1326-2.5 Override Functions

The V_{CCA} pin, if unused, can be tied to either V_{CC3} or V_{CC25} . This is an obvious solution since the trip points for V_{CC3} and V_{CC25} will always be greater than the trip point for V_{CCA} . Likewise, the V_{CC25} , if unused, can be tied to V_{CC3} . V_{CC3} must always be used. Tying V_{CC3} to V_{CC25} and operating off of a 2.5V supply will result in the continuous assertion of $\overline{\text{RST}}$.

Extending ESD Tolerance on the $\overline{\text{PBR}}$ Input Pin

The $\overline{\text{PBR}}$ pin is susceptible to ESD since it may be brought out to a front panel in normal applications. The ESD tolerance of this pin can be increased by adding a resistor in series with the $\overline{\text{PBR}}$ pin. A 10k resistor can increase the ESD tolerance of the $\overline{\text{PBR}}$ pin to approximately 10kV. The $\overline{\text{PBR}}$'s internal pull-up current of 7 μA typical means there is only 70mV (150mV max) dropped across the resistor. See Figure 5.

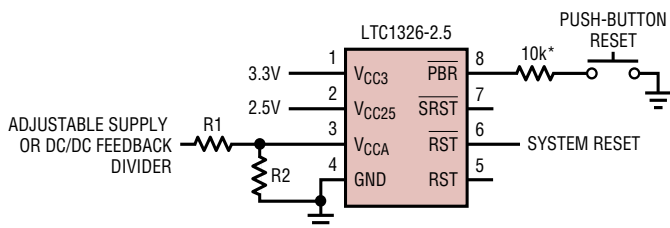
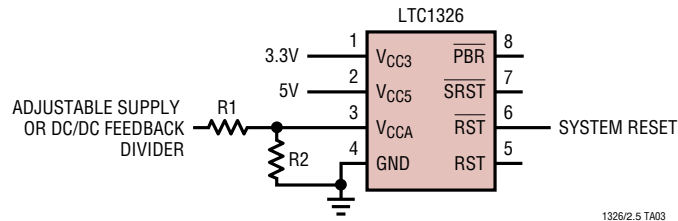


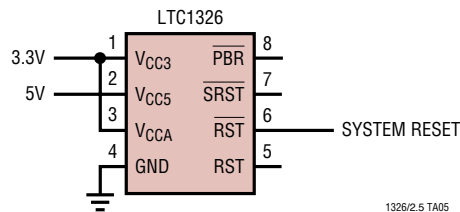
Figure 5. Triple Supply Monitor (3.3V, 2.5V and Adjustable) with Extended ESD Tolerance

TYPICAL APPLICATIONS

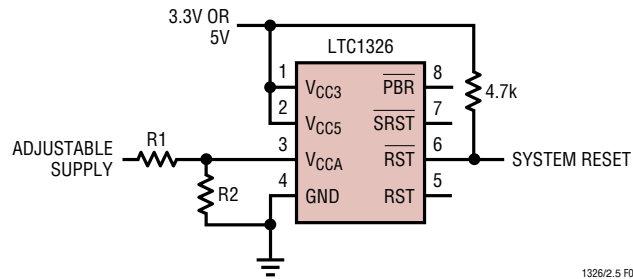
Triple Supply Monitor (3.3V, 5V and Adjustable)



Dual Supply Monitor (3.3V and 5V, Defeat VCCA Input)



Dual Supply Monitor (3.3V or 5V Plus Adj)



REFER TO LTC1326 OVERRIDE FUNCTIONS IN THE APPLICATIONS INFORMATION SECTION.

Dual Supply Monitor (3.3V Plus Adj)

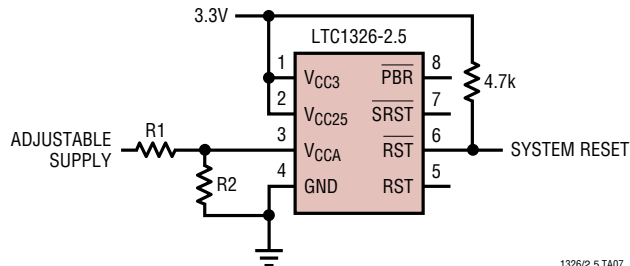


Figure 1 shows the typical application circuit for the LTC1326/2.5. The internal structure of the LTC1326/2.5 is shown on the left, with pins 5, 6, 7, and 8. Pin 8 (PBR) is connected to a pushbutton. Pin 7 (SRST) is connected to a 3.3V supply through a 4.7k resistor and to a reset source. Pin 6 (RST) is connected to a 3.3V supply through a 4.7k resistor and to a reset source. Pin 5 (RST) is connected to a reset source. The internal circuit includes two 6μA current sources, two Schmitt triggers, and a Schmitt trigger with a VCC3 input. The reset sources are labeled "OTHER OPEN DRAIN RESET SOURCES OR-TIED TO RESET".

LTC1326-2.5

Pin Configuration:

- Pin 1: 3.3V
- Pin 2: 2.5V
- Pin 3: 2.5V
- Pin 4: GND
- Pin 5: RST
- Pin 6: RST
- Pin 7: SRST
- Pin 8: PBR

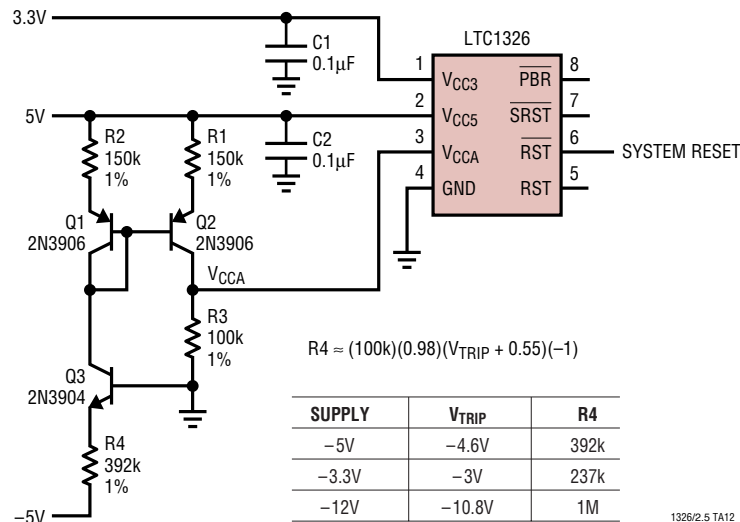
Timing Diagram:

- PBR (Active Low) pulse width: 20ms
- SRST (Active Low) pulse width: 20ms
- RST (Active Low) pulse width: 20ms
- Delay between PBR and SRST: $40\text{ns} \leq t_p \leq 10\mu\text{s}$

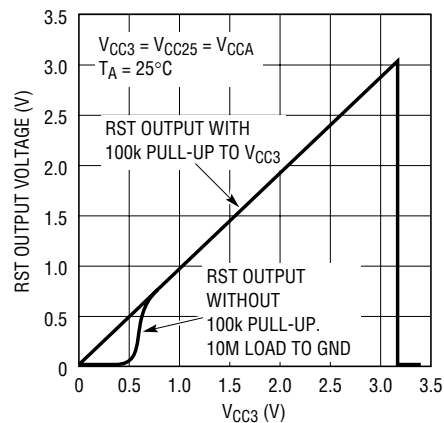
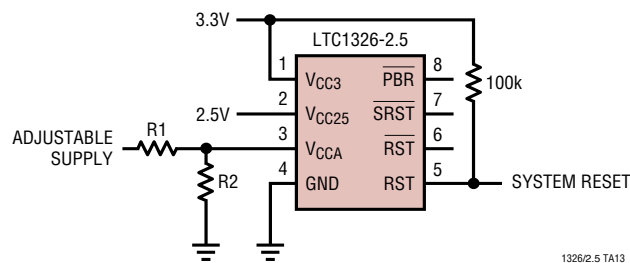
1326/2.5 TA11

TYPICAL APPLICATIONS

Monitoring a Negative Supply



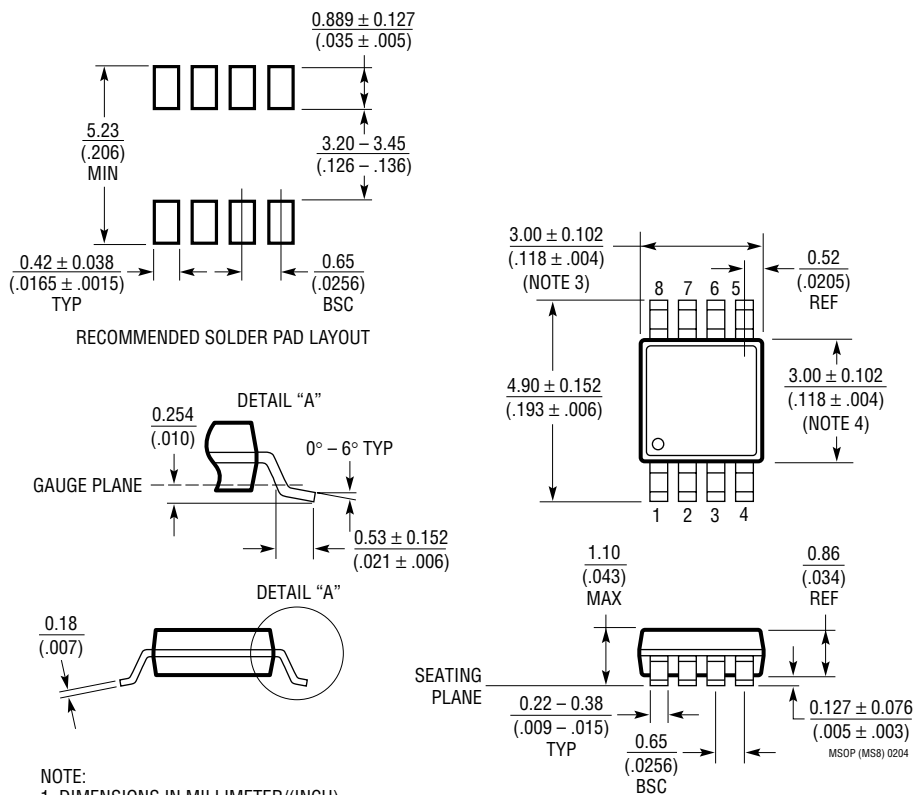
Reset Valid for VCC3 Down to 0V



1326/2.5 TA13a

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
 (Reference LTC DWG # 05-08-1660)

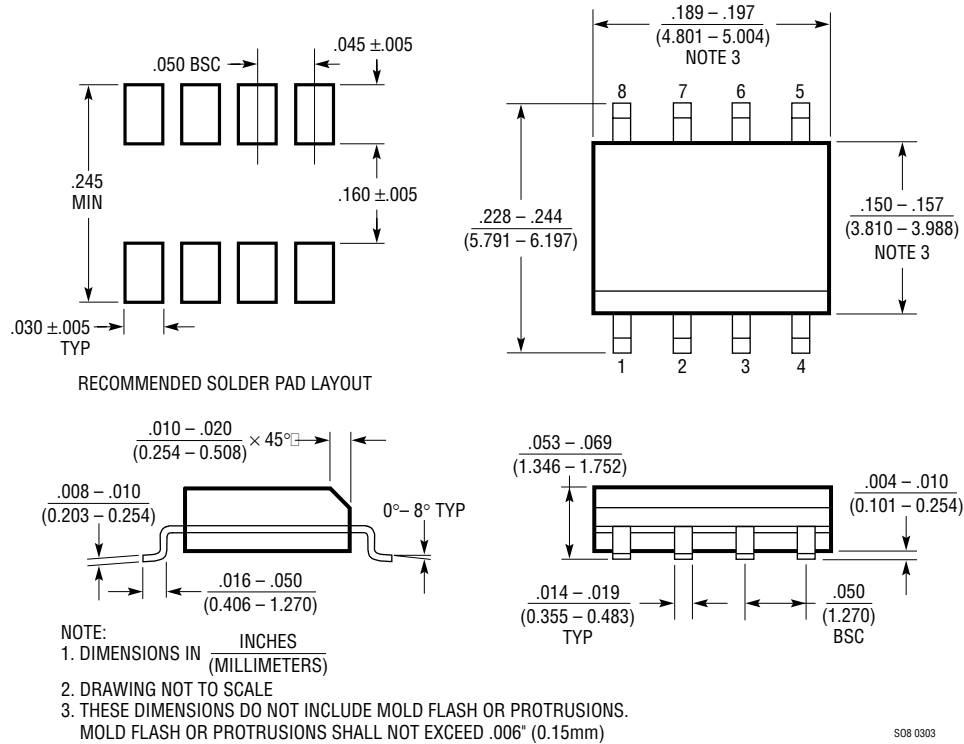


NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



S08 0303

