

LTC1257

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} to GND	-0.5V to 16.5V	Maximum Junction Temperature	
TTL Input Voltage	-0.5V to $V_{CC} + 0.5V$	Plastic Package.....	-65°C to 125°C
V_{OUT}	-0.5V to $V_{CC} + 0.5V$	Storage Temperature Range	-65°C to 150°C
REF	-0.5V to $V_{CC} + 0.5V$	Lead Temperature (Soldering, 10 sec).....	300°C
Operating Temperature Range			
LTC1257C	0°C to 70°C		
LTC1257I.....	-40°C to 85°C		

PIN CONFIGURATION

TOP VIEW N8 PACKAGE 8-LEAD PDIP $T_{JMAX} = 125^{\circ}C, \theta_{JA} = 100^{\circ}C/W$	TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 125^{\circ}C, \theta_{JA} = 150^{\circ}C/W$
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ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1257CN8#PBF	LTC1257CN8#TRPBF	LTC1257CN8	8-Lead PDIP	0°C to 70°C
LTC1257IN8#PBF	LTC1257IN8#TRPBF	LTC1257IN8	8-Lead PDIP	-40°C to 85°C
LTC1257CS8#PBF	LTC1257CS8#TRPBF	1257	8-Lead Plastic SO	0°C to 70°C
LTC1257IS8#PBF	LTC1257IS8#TRPBF	1257I	8-Lead Plastic SO	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = T_{MIN}$ to T_{MAX} . $V_{CC} = 4.75V$ to $15.75V$, internal or external reference ($2.475V \leq V_{REF} \leq V_{CC} - 2.7V$), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DAC						
	Resolution		●	12		Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 4)	●		±0.5	LSB
INL	Integral Nonlinearity	LTC1257C (Note 4)	●		±3.5	LSB
		LTC1257I (Note 4)	●		±4.0	LSB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = T_{MIN}$ to T_{MAX} . $V_{CC} = 4.75V$ to $15.75V$, internal or external reference ($2.475V \leq V_{REF} \leq V_{CC} - 2.7V$), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OFF	Offset Error	When Using Internal Reference, LTC1257C	●		±8	LSB
		When Using Internal Reference, LTC1257I	●		±10	LSB
		When Using External Reference, LTC1257C	●		±4	mV
		When Using External Reference, LTC1257I	●		±5	mV
OFF _{TC}	Offset Error Tempco	When Using Internal Reference (Note 2)	●	±0.02	±0.066	LSB/°C
		When Using External Reference (Note 2)	●	±15	±30	μV/°C
	Gain Error		●	0.5	±2	LSB
	Gain Error Tempco	(Note 2)	●	±0.01	±0.02	LSB/°C

Reference

	Reference Output Voltage	$I_{REF} = 0$, LTC1257C	●	2.028	2.048	2.068	V
		$I_{REF} = 0$, LTC1257I	●	2.018		2.078	V
	Reference Output Tempco	$I_{REF} = 0$	●		±0.06		LSB/°C
	Reference Line Regulation	$I_{REF} = 0$, LTC1257C	●			±0.4	LSB/V
		$I_{REF} = 0$, LTC1257I	●			±0.7	LSB/V
	Reference Load Regulation	$0\mu A \leq I_{REF} \leq 100\mu A$	●			±1	LSB
	Reference Input Range	$V_{CC} > V_{REF} + 2.7V$	●	2.475		12	V
	Reference Input Resistance		●	8	14	18	kΩ
	Reference Input Capacitance	(Note 2)			15		pF
	Short-Circuit Current	V_{REF} Shorted to GND	●			90	mA

Power Supply

V_{CC}	Positive Supply Voltage	For Specified Performance	●	4.75		15.75	V
I_{CC}	Supply Current	$4.75V \leq V_{CC} \leq 5.25V$	●		350	600	μA
		$4.75V \leq V_{CC} \leq 15.75V$	●		800	1500	μA

Op Amp DC Performance

	Short-Circuit Current Low	V_{OUT} Shorted to GND	●			60	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●			60	mA
	Output Impedance to GND	Input Code = 0	●		250	500	Ω

AC Performance

	Voltage Output Slew Rate	5kΩ in Parallel with 100pF	●	1.0			V/μs
	Voltage Output Settling Time	To ±1/2LSB, 5kΩ in Parallel with 100pF, $V_{CC} = 4.75V$			6		μs
	Digital Feedthrough	(Notes 2, 3)			50		nV/s

Digital I/O

V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
V_{OH}	Digital Output High Voltage	$I_{OUT} = -1mA$, D_{OUT} Only	●	$V_{CC} - 1$			V
V_{OL}	Digital Output Low Voltage	$I_{OUT} = 1mA$, D_{OUT} Only	●	0.4			V
I_{LEAK}	Digital Input Leakage	$V_{IN} = GND$ to V_{CC}	●			±10	μA
C_{IN}	Digital Input Capacitance	(Note 2)	●			10	pF

Switching (Note 2)

t_1	D_{IN} Valid to CLK Setup		●	100			ns
t_2	D_{IN} Valid to CLK Hold		●	25			ns
t_3	CLK High Time		●	350			ns
t_4	CLK Low Time		●	350			ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = T_{MIN}$ to T_{MAX} . $V_{CC} = 4.75V$ to $15.75V$, internal or external reference ($2.475V \leq V_{REF} \leq V_{CC} - 2.7V$), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_5	LOAD Pulse Width	●	150			ns
t_6	LSB CLK to $\overline{LOAD}$	●	0			ns
t_7	LOAD High to CLK	●	0			ns
t_8	D_{OUT} Output Delay	$C_{LOAD} = 15pF$ ●	35		150	ns
f_{CLK}	Maximum Clock Frequency				1.4	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

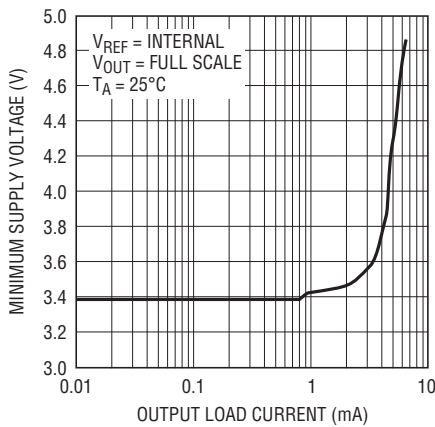
Note 2: Guaranteed by design; not subject to test.

Note 3: DAC switched from all 1s to all 0s, and all 0s to all 1s code.

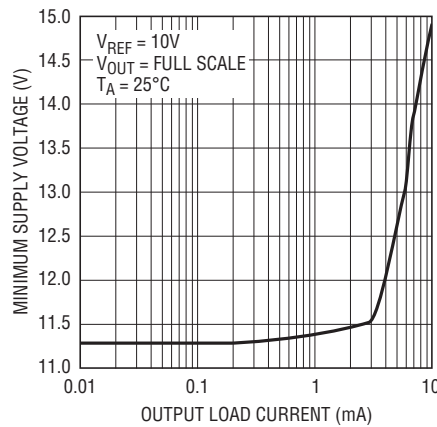
Note 4: Guaranteed with internal V_{REF} or with external V_{REF} range of 2.475V to 12V. Tested at 10V.

TYPICAL PERFORMANCE CHARACTERISTICS

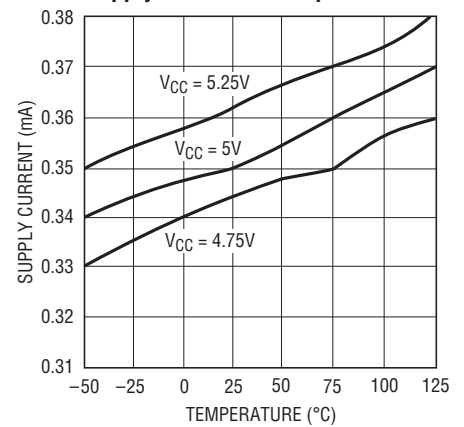
Minimum Supply Voltage
vs Load Current #1



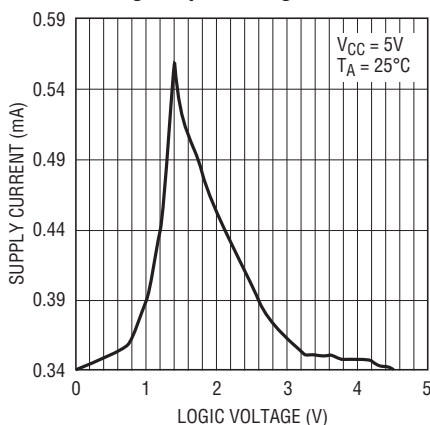
Minimum Supply Voltage
vs Load Current #2



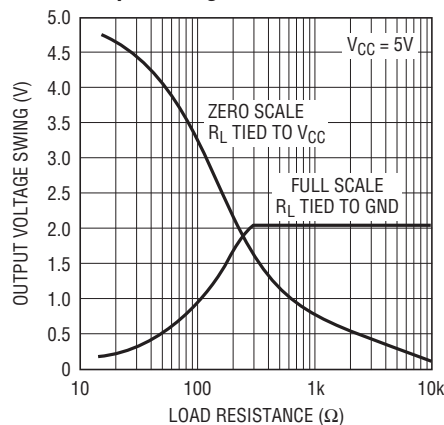
Supply Current vs Temperature



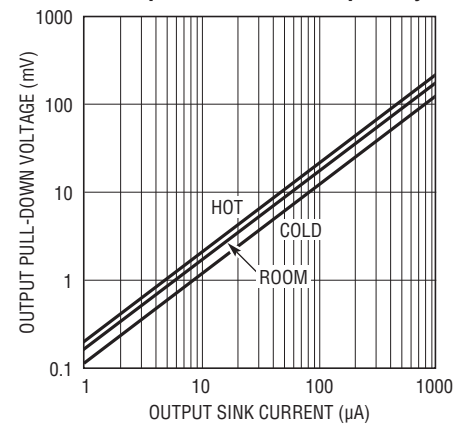
Supply Current
vs Logic Input Voltage



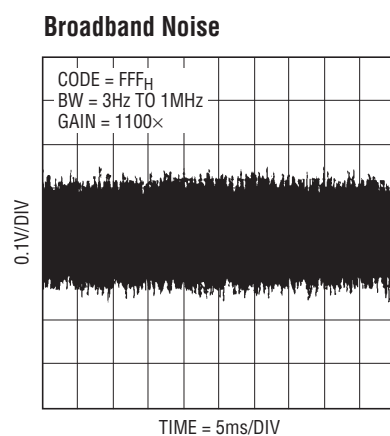
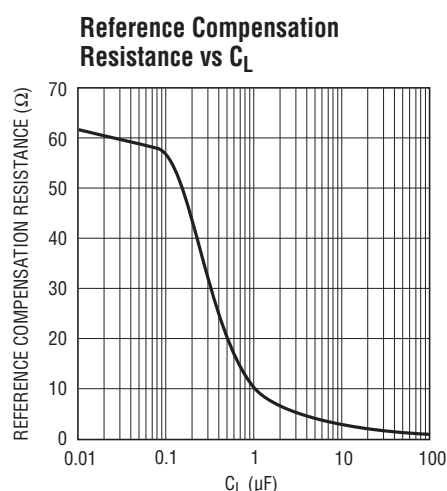
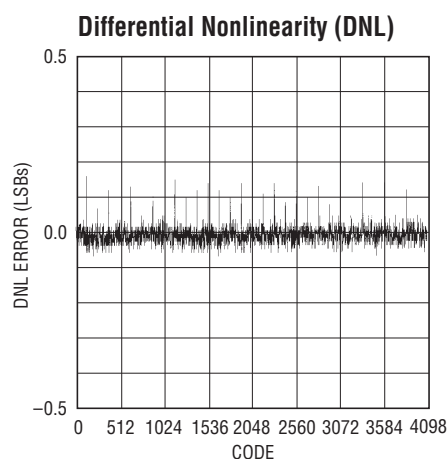
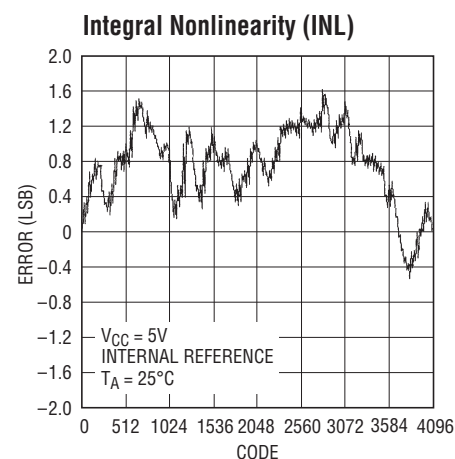
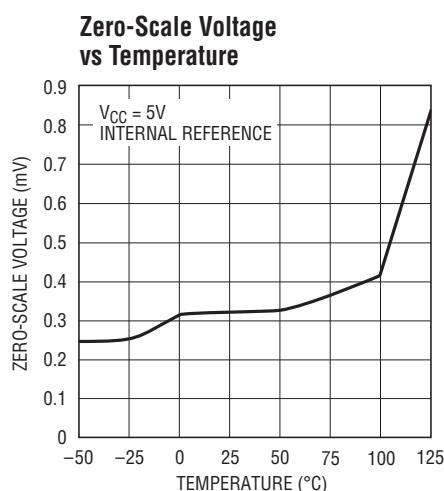
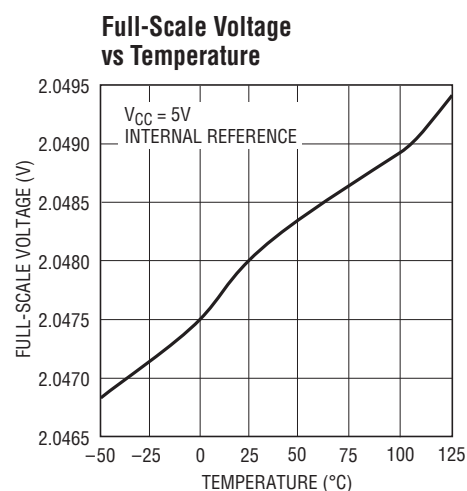
Output Swing vs Load Resistance



Pull-Down Voltage
vs Output Sink Current Capability



TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

CLK (Pin 1): The TTL level input for the serial interface clock.

D_{IN} (Pin 2): The TTL level input for the serial interface data. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock.

LOAD (Pin 3): The TTL level input for the serial interface load control. Data is loaded from the shift register into the DAC register, thus updating the DAC output when $\overline{LOAD}$ is pulled low. The DAC register is transparent as long as $\overline{LOAD}$ is held low.

D_{OUT} (Pin 4): The output of the shift register which becomes valid on the rising edge of the serial clock. The D_{OUT} pin is driven from GND to V_{CC} by an internal CMOS inverter. Multiple LTC1257s may be cascaded by connecting the D_{OUT} pin to the D_{IN} pin of the next chip.

GND (Pin 5): Ground.

REF (Pin 6): The output of the 2.048V reference and the input to the DAC resistor ladder. An external reference with voltage from 2.475V to $V_{CC} - 2.7V$ may be used to override the internal reference.

PIN FUNCTIONS

V_{OUT} (Pin 7): The buffered DAC output is capable of sourcing 2mA over temperature while pulling within 2.7V of V_{CC}. The output will pull to ground through an internal 250Ω equivalent resistance.

V_{CC} (Pin 8): The positive supply input. $4.75V \leq V_{CC} \leq 15.75V$. Requires a bypass capacitor to ground.

DEFINITIONS

LSB: The least significant bit or the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS}) / 2^n - 1$$

n = The number of digital input bits

V_{OS} = The zero code error or offset of the DAC

V_{FS} = The full-scale output voltage of the DAC measured when all bits are set to 1

Resolution: The resolution is the number of DAC output states (2^n) that divide the full-scale range. The resolution does not imply linearity.

INL: End-point integral nonlinearity is the maximum deviation from a straight line passing through the end-points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below ground, the linearity is measured between full-scale and the first code that guarantees a positive output. The INL error at a given input code is calculated as follows:

$$INL = (V_{OUT} - V_{IDEAL}) / LSB$$

$$V_{IDEAL} = (Code)(LSB) + V_{OS}$$

V_{OUT} = The output voltage of the DAC measured at the given input code

DNL: Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB) / LSB$$

ΔV_{OUT} = The measured voltage difference between two adjacent codes

Offset Error: The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below ground. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

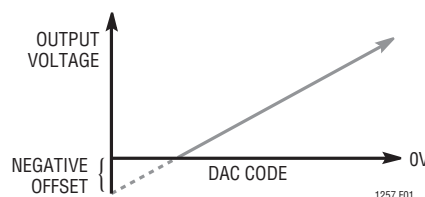


Figure 1. Effect of Negative Offset

The offset of the part is measured at the first code that produces an output voltage 0.5LSB greater than the previous code:

$$V_{OS} = V_{OUT} - [(Code)(V_{FS}) / (2^n - 1)]$$

Full-Scale Error: Full-scale error is the difference between the ideal and measured DAC output voltages with all bits set to one (Code = 4095). The full-scale error includes the offset error and is calculated as follows:

$$FSE = (V_{OUT} - V_{IDEAL}) / LSB$$

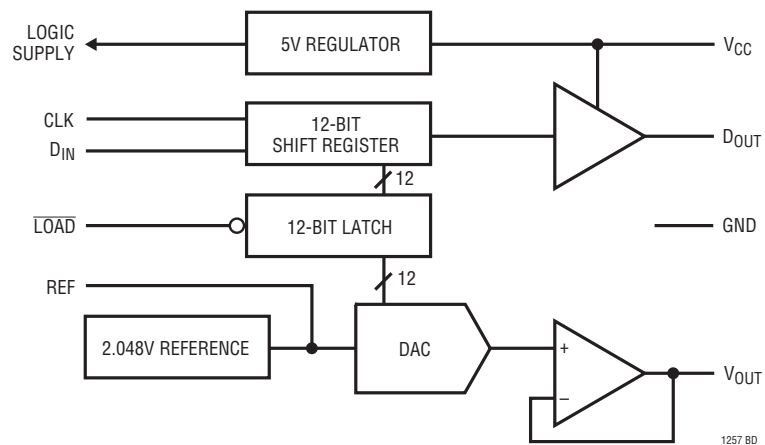
$$V_{IDEAL} = (V_{REF})(1 - 2^{-n}) - V_{OS}$$

V_{REF} = The reference voltage, either internal or external

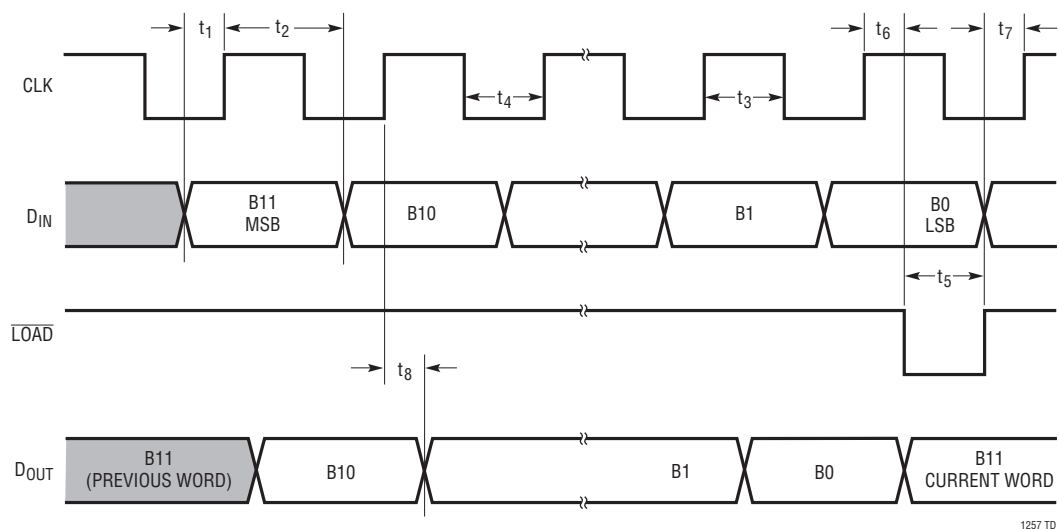
Gain Error: Gain error is the difference between the ideal and measured slope of the DAC transfer characteristic. Gain error is equal to full-scale error minus offset error.

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(sec).

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

Serial Interface

The data on the D_{IN} input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first and the LSB last. The DAC register loads the data from the shift register when $\overline{LOAD}$ is pulled low, and remains transparent until $\overline{LOAD}$ is pulled high and the data is latched.

An internal 5V regulator provides the supply for the digital logic. By limiting the internal digital signal swings to 5V, digital noise is reduced. The buffered output of the 12-bit shift register is available on the D_{OUT} pin which will swing from GND to V_{CC} .

Multiple LTC1257s may be daisy chained together by connecting the D_{OUT} pin to the D_{IN} pin of the next chip, while the clock and load signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the $\overline{LOAD}$ signal is pulled low to update all of them simultaneously. The maximum clocking rate is 1.4MHz.

Reference

The LTC1257 includes an internal 2.048V reference, making 1LSB equal to 500 μ V. The internal reference output is turned off when the pin is forced above the reference voltage, allowing an external reference to be connected to the reference pin. The external reference must be greater than 2.475V and less than $V_{CC} - 2.7V$, and be capable of driving the 10k minimum DAC resistor ladder.

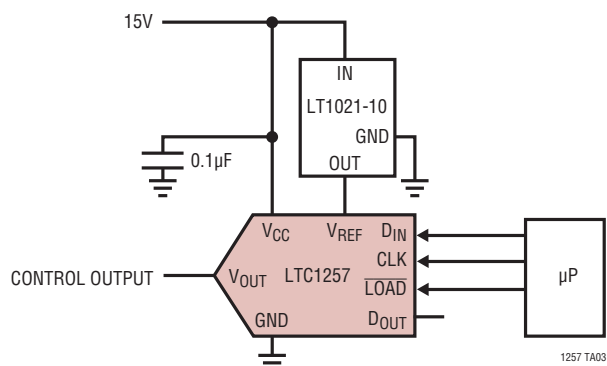
If the reference output is driving a large capacitive load, a series resistor must be added to insure stability. For any capacitive load greater than 1 μ F, a 10 Ω series resistor will suffice.

Voltage Output

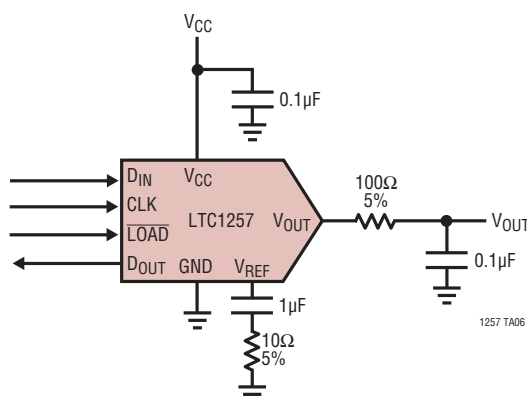
The LTC1257 voltage output is able to pull within 2.7V of V_{CC} while sourcing 2mA. A internal NMOS transistor with a 200 Ω equivalent impedance pulls the output to ground. The output is protected against short circuits and is able to drive up to a 500pF capacitive load without oscillation. If digital noise on the output causes a problem, a simple 100 Ω , 0.1 μ F RC circuit can be used to filter the noise.

TYPICAL APPLICATIONS

DAC with External Reference



Filtering V_{REF} and V_{OUT}



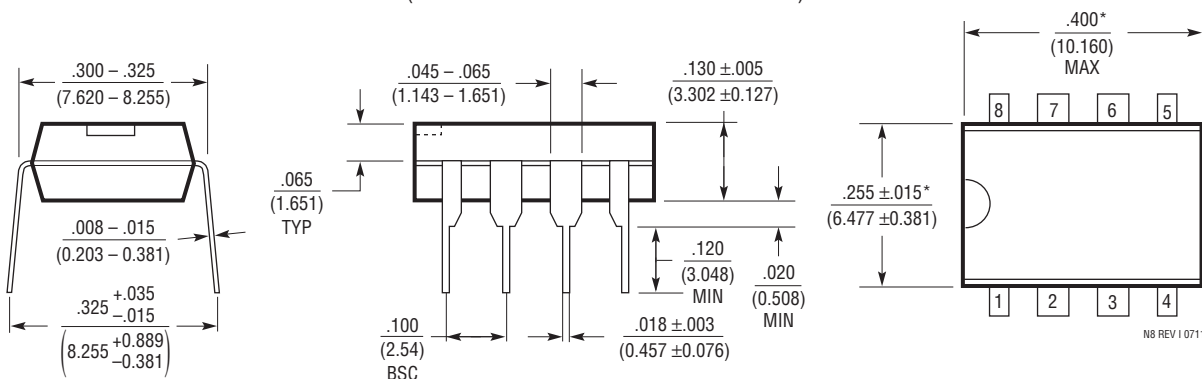
The circuit diagram illustrates a multi-channel differential amplifier. At the top, a 5V supply is connected to the V_{CC} pin of the LTC1296 multiplexer and the V_{CC} pin of the first LTC1257 op-amp. A 22 μF capacitor is connected between the 5V supply and ground. The LTC1296 multiplexer has 8 ANALOG INPUT CHANNELS (CH0 to CH7) and a COM pin. Its V_{CC} pin is connected to the 5V supply, and its $\overline{CS}$ pin is connected to the μP . The LTC1296's D_{OUT} , CLK , and D_{IN} pins are connected to the μP . The LTC1296's REF^+ pin is connected to ground, and its SSO pin is connected to the V_{REF} pin of the first LTC1257 op-amp. The first LTC1257 op-amp has its V_{CC} pin connected to the 5V supply, its GND pin connected to ground, and its V_{REF} pin connected to the SSO pin of the LTC1296. The D_{IN} , CLK , $LOAD$, and D_{OUT} pins of the first LTC1257 are connected to the μP . The output of the first LTC1257 (V_{OUT}) is connected to the non-inverting input of the second LTC1257 op-amp. The second LTC1257 op-amp has its V_{CC} pin connected to the 5V supply, its GND pin connected to ground, and its V_{REF} pin connected to the SSO pin of the LTC1296. The output of the second LTC1257 (V_{OUT}) is connected to the inverting input of the first LTC1257 op-amp. A 100 Ω resistor is connected between the V_{OUT} pin of the first LTC1257 and ground. A 0.1 μF capacitor is connected between the V_{OUT} pin of the first LTC1257 and ground. A 50k resistor is connected between the 5V supply and the non-inverting input of the first LTC1257. A 50k resistor is connected between the non-inverting input of the first LTC1257 and the inverting input of the first LTC1257. A 100 Ω resistor is connected between the non-inverting input of the first LTC1257 and ground. A 0.1 μF capacitor is connected between the non-inverting input of the first LTC1257 and ground. A 74HC04 inverter is connected between the 5V supply and ground. The output of the 74HC04 is connected to the D_{IN} pin of the first LTC1257 op-amp. The μP is connected to the $\overline{CS}$, D_{OUT} , CLK , D_{IN} , $LOAD$, and D_{OUT} pins of the LTC1296 and the D_{IN} , CLK , $LOAD$, and D_{OUT} pins of the LTC1257 op-amps.

The circuit diagram illustrates a precision 12-bit DAC system. It features an LT1025A precision current source, an LTC1050 precision op-amp, an LTC1297 12-bit DAC, and an LTC1257 12-bit DAC. The LT1025A provides a precise current to the LTC1050, which is configured as a voltage-to-current converter. The LTC1297 DAC is used for digital-to-analog conversion, and the LTC1257 DAC is used for analog-to-digital conversion. The circuit is powered by a 5V supply and includes various passive components like resistors and capacitors for stability and precision.

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

N Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510 Rev I)

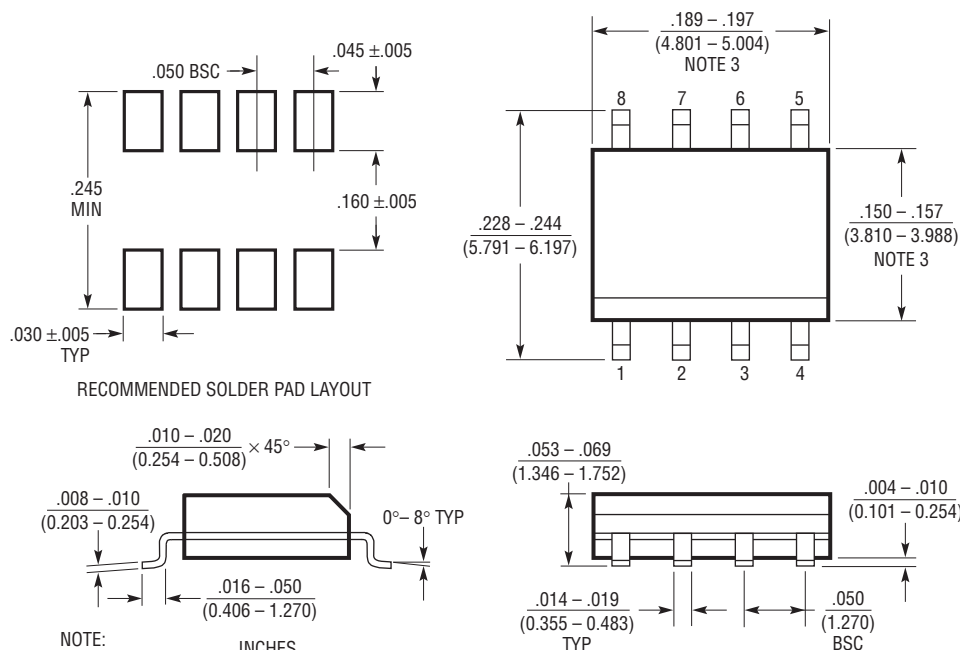


NOTE:

1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610 Rev G)



NOTE:

1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

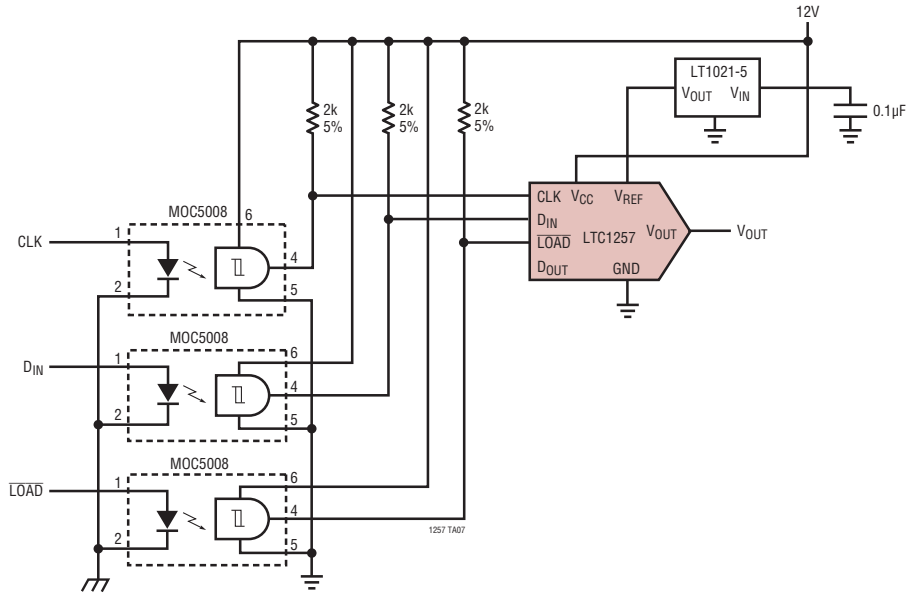
S08 REV G 0212

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	12/12	Removed MAX Voltage Output Settling Time value in Electrical Characteristics section	3

TYPICAL APPLICATION

Driving LTC1257 with Opto-Isolators



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
12 Bit		
LTC1446/LTC1446L	Dual 12-Bit V_{OUT} DACs in SO-8 Package	LTC1446: $V_{CC} = 4.5V$ to $5.5V$, $V_{OUT} = 0V$ to $4.095V$ LTC1446L: $V_{CC} = 2.7V$ to $5.5V$, $V_{OUT} = 0V$ to $2.5V$
LTC1448	Dual 12-Bit V_{OUT} DAC in SO-8 Package, $V_{CC} = 2.7V$ to $5.5V$	Output Swings from GND to REF, REF Input Can Be Tied to V_{CC}
LTC1450/LTC1450L	Single 12-Bit V_{OUT} DACs with Parallel Interface	LTC1450: $V_{CC} = 4.5V$ to $5.5V$, $V_{OUT} = 0V$ to $4.095V$ LTC1450L: $V_{CC} = 2.7V$ to $5.5V$, $V_{OUT} = 0V$ to $2.5V$
LTC1451	Single Rail-to-Rail 12-Bit V_{OUT} DAC, Full Scale: $4.095V$, $V_{CC} = 4.5V$ to $5.5V$, Internal $2.048V$ Reference Brought Out to Pin	Low Power, Complete V_{OUT} DAC in SO-8 Package
LTC1452	Single Rail-to-Rail 12-Bit V_{OUT} Multiplying DAC, $V_{CC} = 2.7V$ to $5.5V$	Low Power, Multiplying V_{OUT} DAC with Rail-to-Rail Buffer Amplifier in SO-8 Package
LTC1453	Single Rail-to-Rail 12-Bit V_{OUT} DAC, Full Scale: $2.5V$, $V_{CC} = 2.7V$ to $5.5V$	$3V$, Low Power, Complete V_{OUT} DAC in SO-8 Package
LTC1454/LTC1454L	Dual 12-Bit V_{OUT} DACs in SO-16 Package with Added Functionality	LTC1454: $V_{CC} = 4.5V$ to $5.5V$, $V_{OUT} = 0V$ to $4.095V$ LTC1454L: $V_{CC} = 2.7V$ to $5.5V$, $V_{OUT} = 0V$ to $2.5V$
LTC1456	Single Rail-to-Rail Output 12-Bit DAC with Clear Pin, Full Scale: $4.095V$, $V_{CC} = 4.5V$ to $5.5V$	Low Power, Complete V_{OUT} DAC in SO-8 Package with Clear Pin
LTC1458/LTC1458L	Quad 12 Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: $V_{CC} = 4.5V$ to $5.5V$, $V_{OUT} = 0V$ to $4.095V$ LTC1458L: $V_{CC} = 2.7V$ to $5.5V$, $V_{OUT} = 0V$ to $2.5V$
LTC1659	Single Rail-to-Rail 12-Bit V_{OUT} DAC in MSOP-8 Package, $V_{CC} = 2.7V$ to $5.5V$	Output Swings from GND to REF, REF Input Can Be Tied to V_{CC}
14 Bit		
LTC1658	14-Bit Rail-to-Rail Micropower DAC in MSOP, $V_{CC} = 2.7V$ to $5.5V$	Output Swings from GND to REF, REF Input Can Be Tied to V_{CC}
LTC1654	Dual 14-Bit V_{OUT} DAC	Programmable Speed/Power, SO-8 Footprint
16 Bit		
LTC1655(L)	Single 16-Bit V_{OUT} DAC with Serial Interface in SO-8	$V_{CC} = 5V$ ($3V$), Low Power, Deglitched, $V_{OUT} = 0V$ to $4.096V$ ($0V$ to $2.5V$)

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