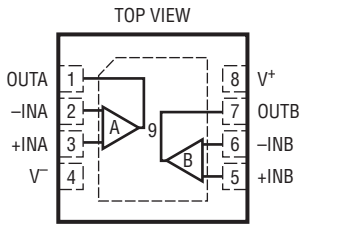
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage (within Supplies) 36V
Input Voltage (DGND, EN, +IN, –IN)
(Relative to V^-) 36V
Input Current (+IN, –IN, DGND, EN) ..... ±10mA
Output Short-Circuit Duration ..... Indefinite

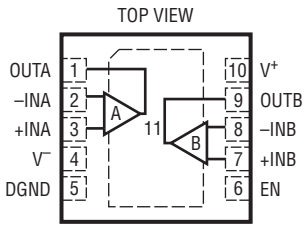
Operating and Specified Temperature Range
I-Grade ..... –40°C to 85°C
H-Grade ..... –40°C to 125°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



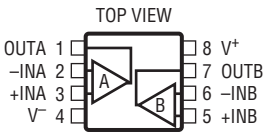
DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

θ_{JA} = 43°C/W, θ_{JC} = 5.5°C/W
EXPOSED PAD (PIN 9) IS CONNECTED TO V^- (PIN 4)
(PCB CONNECTION OPTIONAL)



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

θ_{JA} = 43°C/W, θ_{JC} = 5.5°C/W
EXPOSED PAD (PIN 11) IS CONNECTED TO V^- (PIN 4)
(PCB CONNECTION OPTIONAL)



MS8 PACKAGE
8-LEAD PLASTIC MSOP

θ_{JA} = 163°C/W, θ_{JC} = 40°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT6023IDD#PBF	LT6023IDD#TRPBF	LGRS	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT6023HDD#PBF	LT6023HDD#TRPBF	LGRS	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT6023IDD-1#PBF	LT6023IDD-1#TRPBF	LGRV	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT6023HDD-1#PBF	LT6023HDD-1#TRPBF	LGRV	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT6023IMS8#PBF	LT6023IMS8#TRPBF	LTGRT	8-Lead Plastic MSOP	–40°C to 85°C
LT6023HMS8#PBF	LT6023HMS8#TRPBF	LTGRT	8-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = Mid-Supply, V_{DGND} = 0V, V_{EN} = 5V. DGND and EN specifications only apply to the LT6023-1.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	DD Packages			20	70	µV
			●			160	µV
		MS8 Package			5	30	µV
			●			160	µV
$\frac{\Delta V_{OSI}}{\Delta Temp}$	Input Offset Voltage Drift (Note 2)	DD Packages	●	–3.5	±0.9	3.5	µV/°C
		MS8 Package	●	–2.9	±0.5	2.9	µV/°C
$\frac{\Delta V_{OSI}}{\Delta Time}$	Long Term Input Offset Voltage Stability				±0.2		µV/Mo
I_B	Input Bias Current			–3	±0.1	3	nA
		T_A = –40° to 85°C	●	–3		3	nA
		T_A = –40° to 125°C	●	–10		10	nA
I_{OS}	Input Offset Current			–1	±0.1	1	nA
		T_A = –40° to 85°C	●	–1		1	nA
		T_A = –40° to 125°C	●	–2		2	nA
	Input Noise Voltage	0.1Hz to 10Hz			3		μV_{P-P}
e_n	Input Noise Voltage Density	f = 1Hz			132		$nV/\sqrt{Hz}$
		f = 1kHz			132		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1kHz			12.1		$fA/\sqrt{Hz}$
C_{IN}	Input Capacitance	Common Mode			1.5		pF
		Differential Mode			2.5		pF
R_{IN}	Input Resistance	Common Mode			140		GΩ
		Differential Mode			330		MΩ
V_{ICM}	Common Mode Input Range		●	V^- + 1.2		V^+ – 1.4	V
CMRR	Common Mode Rejection Ratio	V_{CM} = –13.8V to 13.6V		120	136		dB
			●	116			dB
PSRR	Supply Rejection Ratio	V_S = 3V to 30V		120	140		dB
			●	110			dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 10kΩ, V_{OUT} = ±14V		110	114		dB
			●	100			dB
		R_L = 100kΩ, V_{OUT} = ±14.5V		126	134		dB
			●	116			dB
V_{OL}	Output Swing Low ($V_{OUT} - V^-$)	R_L = 10kΩ			180	300	mV
		T_A = –40° to 85°C	●			380	mV
		T_A = –40° to 125°C	●			430	mV
V_{OH}	Output Swing High ($V^+ - V_{OUT}$)	R_L = 10kΩ			115	140	mV
		T_A = –40° to 85°C	●			165	mV
		T_A = –40° to 125°C	●			190	mV
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, Sourcing		3	5.25		mA
		T_A = –40° to 85°C	●	2.5			mA
		T_A = –40° to 125°C	●	2			mA
		V_{OUT} = 0V, Sinking		6.5	15		mA
		T_A = –40° to 85°C	●	4.5			mA
		T_A = –40° to 125°C	●	4			mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = Mid-Supply, V_{DGND} = 0V, V_{EN} = 5V. DGND and EN specifications only apply to the LT6023-1.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SR	Slew Rate	A_{VCL} = 1, 10V Step		0.85	1.4		V/µs
		T_A = –40° to 85°C	●	0.7			V/µs
		T_A = –40° to 125°C	●	0.6			V/µs
		A_{VCL} = 1, 5V Step		0.3	0.65		V/µs
		T_A = –40° to 85°C	●	0.25			V/µs
		T_A = –40° to 125°C	●	0.2			V/µs
GBW	Gain-Bandwidth Product	f = 1kHz	●	29	40		kHz
	Minimum Supply Voltage	Guaranteed by PSRR	●	3			V
I_S	Supply Current per Amplifier				18	20	µA
		T_A = –40° to 85°C	●			28	µA
		T_A = –40° to 125°C	●			40	µA
	Supply Current in Shutdown	V_{EN} = 0.8V			0.8	3	µA
		T_A = –40° to 85°C	●			3.2	µA
		T_A = –40° to 125°C	●			3.6	µA
t_s	Settling Time (A_V = 1)	0.1% 5V Output Step			40		µs
		0.01% 5V Output Step			60		µs
		0.0015% 5V Output Step			124		µs
		0.0015% 10V Output Step			132		µs
t_{ON}	Enable Time	A_V = 1			480		µs
V_{DGND}	DGND Pin Voltage Range		●	V^-		V^+ – 3	V
I_{DGND}	DGND Pin Current		●			–200	nA
I_{EN}	EN Pin Current		●			–200	nA
V_{ENL}	EN Pin Input Low Voltage	Relative to DGND	●			0.8	V
V_{ENH}	EN Pin Input High Voltage	Relative to DGND	●	1.7			V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C, V_S = 3V, V_{CM} = V_{OUT} = Mid-Supply, V_{DGND} = 0V, V_{EN} = 3V. DGND and EN pin specifications only apply to the LT6023-1.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	DD Packages	 ●		20	100 190	µV µV
		MS8 Package	 ●		5	45 175	µV µV
$\frac{\Delta V_{OSI}}{\Delta Temp}$	Input Offset Voltage Drift (Note 2)	DD Packages	●	–3.5	±0.9	3.5	µV/°C
		MS8 Package	●	–2.9	±0.5	2.9	µV/°C
$\frac{\Delta V_{OSI}}{\Delta Time}$	Long Term Input Offset Voltage Stability				±0.2		µV/Mo
I_B	Input Bias Current				±1		nA
I_{OS}	Input Offset Current				±0.1		nA
	Input Noise Voltage	0.1Hz to 10Hz			3		μV_{P-P}
e_n	Input Noise Voltage Density	f = 1Hz f = 1kHz			132 132		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 1kHz			12.1		$fA/\sqrt{Hz}$
C_{IN}	Input Capacitance	Common Mode Differential Mode			1.5 2.5		pF pF
R_{IN}	Input Resistance	Common Mode Differential Mode			140 400		GΩ MΩ
V_{ICM}	Common Mode Input Range		●	V^- + 1.2		V^+ – 1.4	V
CMRR	Common Mode Rejection Ratio	V_{CM} = 1.2V to 1.6V			125		dB
PSRR	Supply Rejection Ratio	V_S = 3V to 30V	 ●	120 110	140		dB dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 10kΩ, V_{OUT} = 0.5V to 2.5V	 ●	98 95	108		dB dB
		R_L = 100kΩ, V_{OUT} = 0.5V to 2.5V			136		dB
V_{OL}	Output Swing Low (V_{OUT} – V^-)	R_L = 10kΩ T_A = –40° to 85°C T_A = –40° to 125°C	 ● ●		60	100 150 170	mV mV mV
V_{OH}	Output Swing High (V^+ – V_{OUT})	R_L = 10kΩ T_A = –40° to 85°C T_A = –40° to 125°C	 ● ●		60	80 90 100	mV mV mV
I_{SC}	Short-Circuit Current	V_{OUT} = 1.5V, Sourcing T_A = –40° to 85°C T_A = –40° to 125°C	 ● ●	2.5 2.25 2	3.5		mA mA mA
		V_{OUT} = 1.5V, Sinking T_A = –40° to 85°C T_A = –40° to 125°C	 ● ●	3.5 2 2	5		mA mA mA
SR	Slew Rate (Note 3)	A_{VCL} = –1, 2V Step			0.05		V/µs
GBW	Gain-Bandwidth Product	f = 1kHz			40		kHz
	Minimum Supply Voltage	Guaranteed by PSRR	●	3			V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C, V_S = 3V, V_{CM} = V_{OUT} = Mid-Supply, V_{DGND} = 0V, V_{EN} = 3V. DGND and EN pin specifications only apply to the LT6023-1.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Supply Current per Amplifier				15	20	µA
		T_A = –40° to 85°C	●			25	µA
		T_A = –40° to 125°C	●			35	µA
	Supply Current in Shutdown	V_{EN} = 0.8V			0.2	1.1	µA
		T_A = –40° to 85°C	●			1.5	µA
		T_A = –40° to 125°C	●			3	µA
t_s	Settling Time (A_V = –1)	0.1% 2.4V Output Step			85		µs
		0.01% 2.4V Output Step			100		µs
		0.0015% 2.4V Output Step			250		µs
t_{ON}	Enable Time	A_V = 1			580		µs
V_{DGND}	DGND Pin Voltage Range		●	V^-		V^+ – 3	V
I_{DGND}	DGND Pin Current				–75		nA
I_{EN}	EN Pin Current				–75		nA
V_{ENL}	EN Pin Input Low Voltage	Relative to DGND	●			0.8	V
V_{ENH}	EN Pin Input High Voltage	Relative to DGND	●	1.7			V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

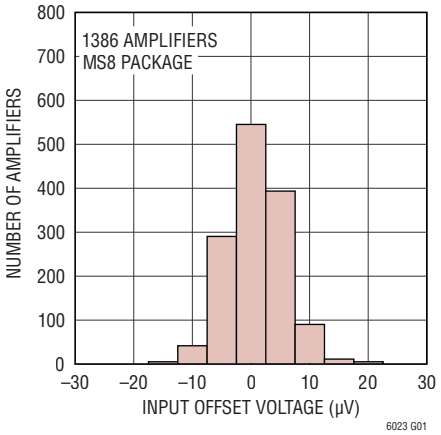
Note 2: Guaranteed by design.

Note 3: The slew rate of the LT6023 increases with the size of the input step. At lower supplies, the input step size is limited by the input common mode range. This trend can be seen in the Typical Performance Characteristics.

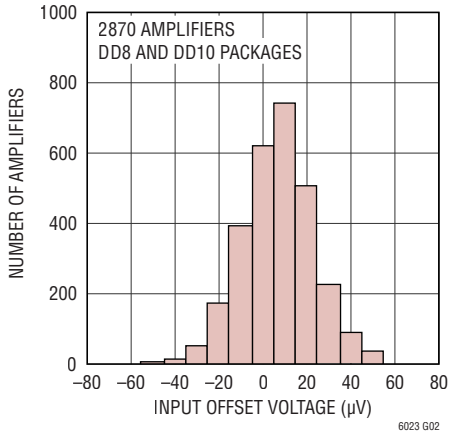
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, R_L = 100kΩ, unless otherwise specified.

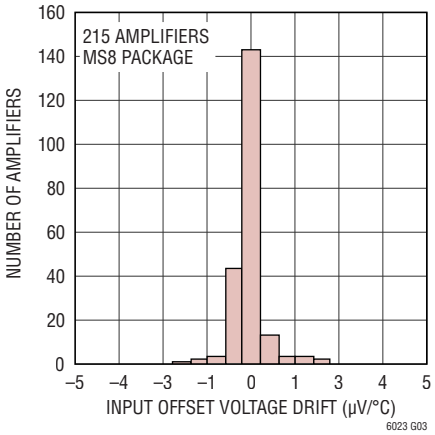
Typical Distribution of Input Offset Voltage



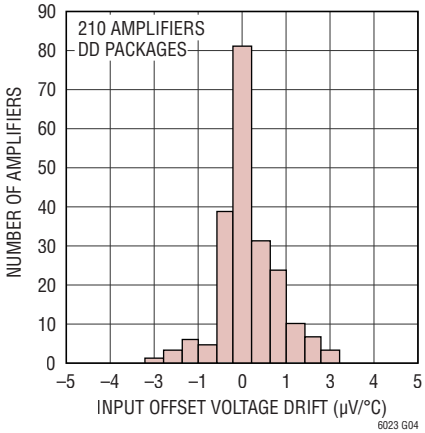
Typical Distribution of Input Offset Voltage



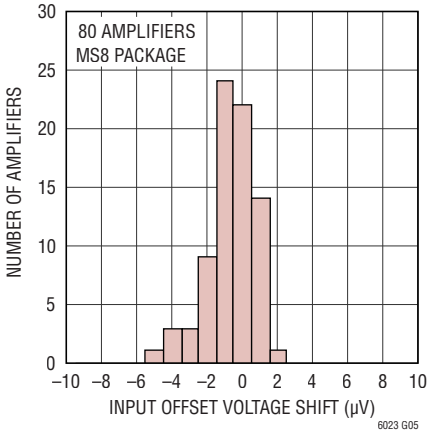
Typical Distribution of Input Offset Voltage Drift



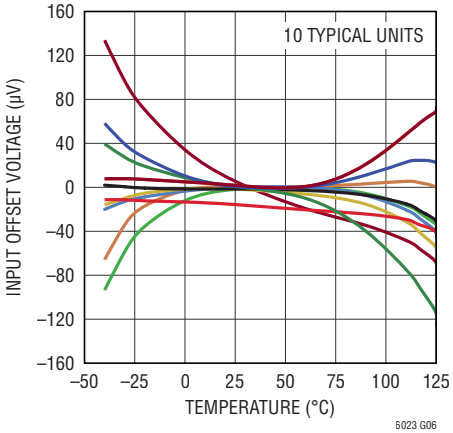
Typical Distribution of Input Offset Voltage Drift



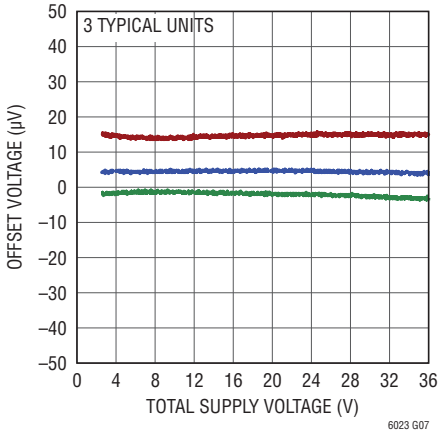
Offset Voltage Shift vs Lead Free IR Reflow



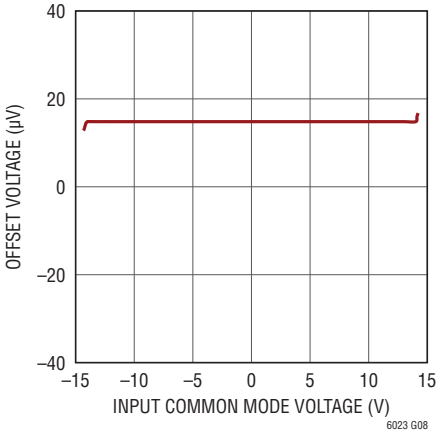
Typical Input Offset Voltage vs Temperature



Offset Voltage vs Supply Voltage



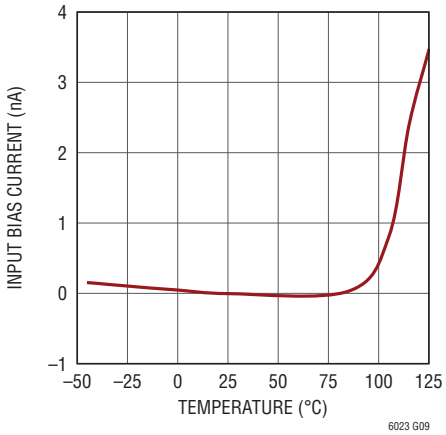
Offset Voltage vs Input Common Mode Voltage



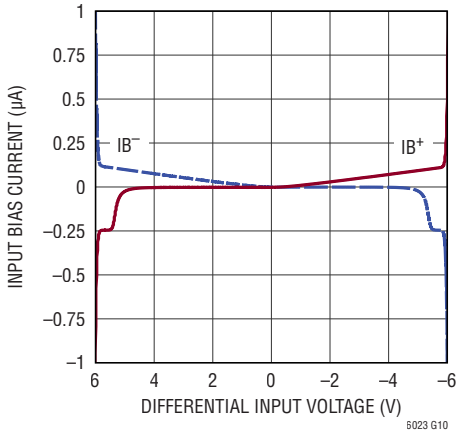
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, R_L = 100kΩ, unless otherwise specified.

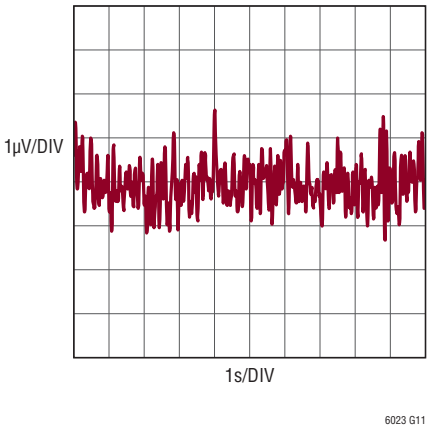
Input Bias Current vs Temperature



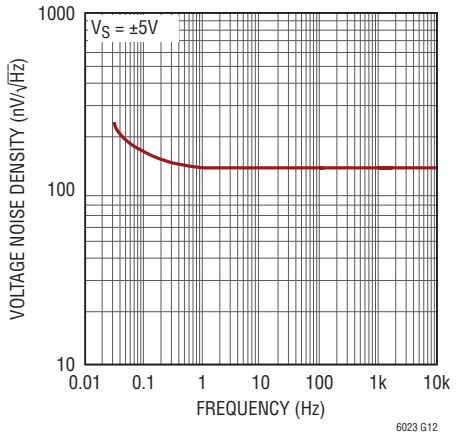
Input Bias Current vs Differential Input Voltage



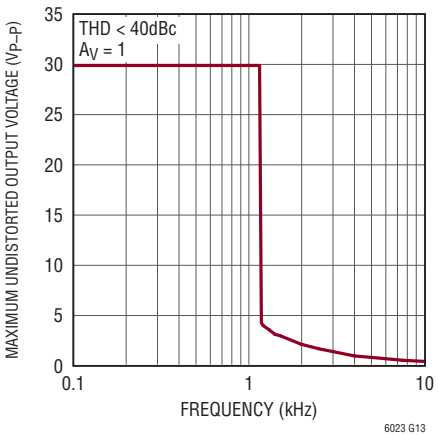
0.1Hz to 10Hz Voltage Noise



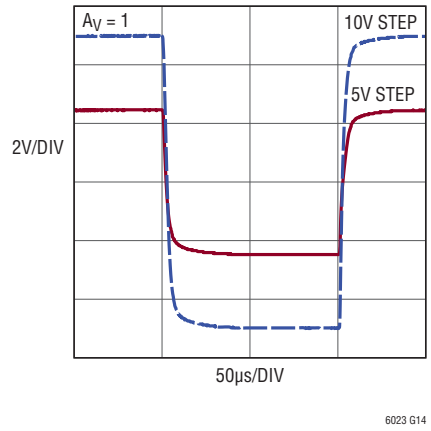
Voltage Noise Density vs Frequency



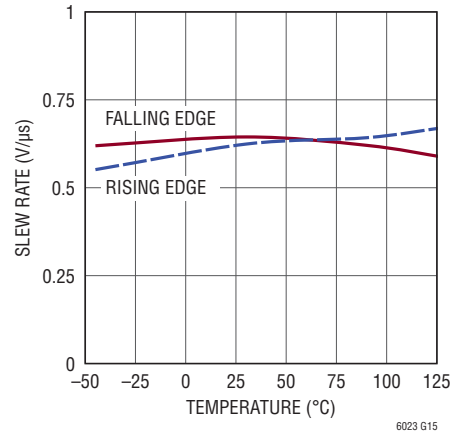
Maximum Undistorted Output Amplitude vs Frequency



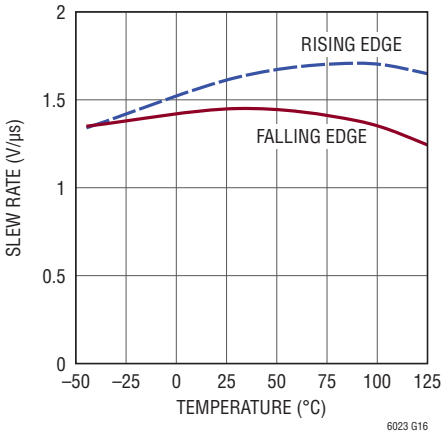
Large-Signal Transient Response (5V Step)



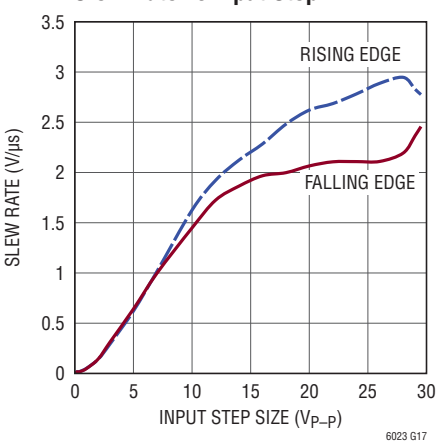
Slew Rate vs Temperature (5V Step)



Slew Rate vs Temperature (10V Step)



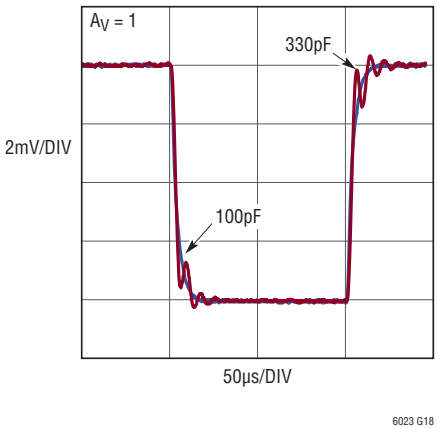
Slew Rate vs Input Step



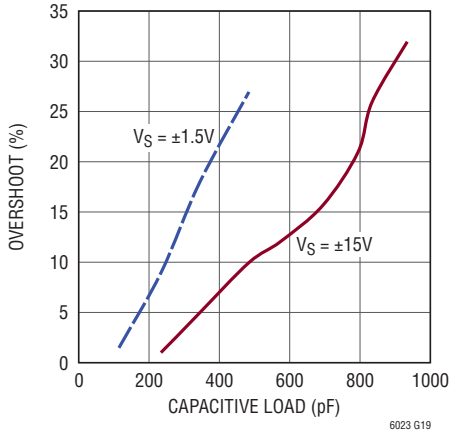
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, R_L = 100kΩ unless otherwise specified.

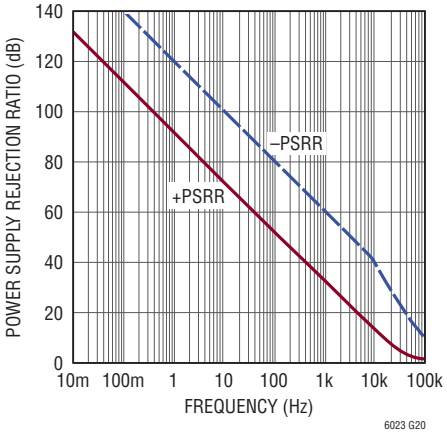
Small-Signal Transient Response



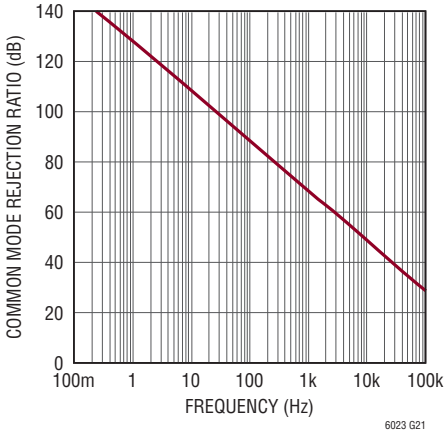
Overshoot vs Capacitive Load



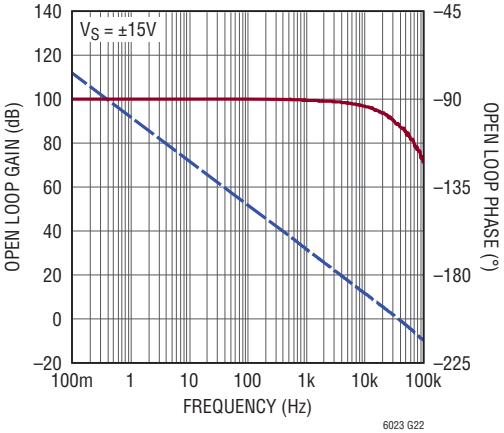
PSRR vs Frequency



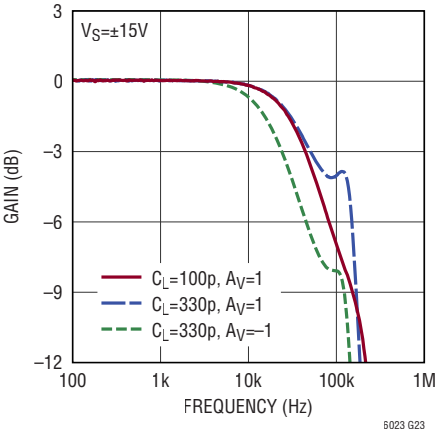
CMRR vs Frequency



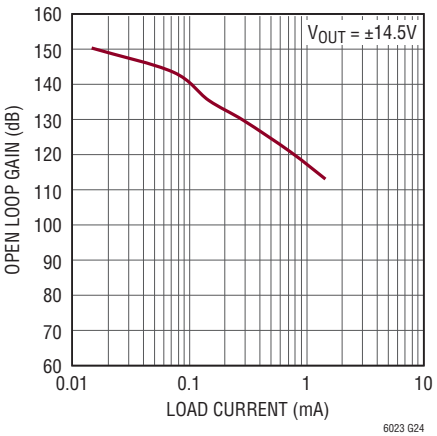
Open-Loop Gain and Phase vs Frequency



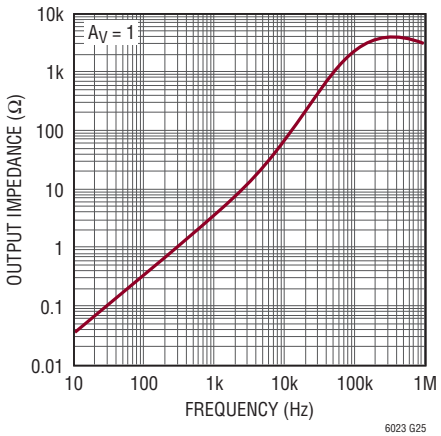
Gain vs Frequency



Open Loop Gain vs Load



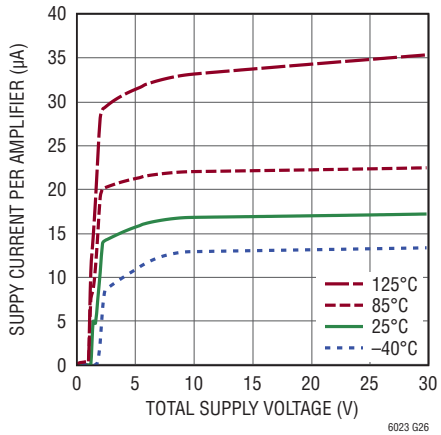
Output Impedance vs Frequency



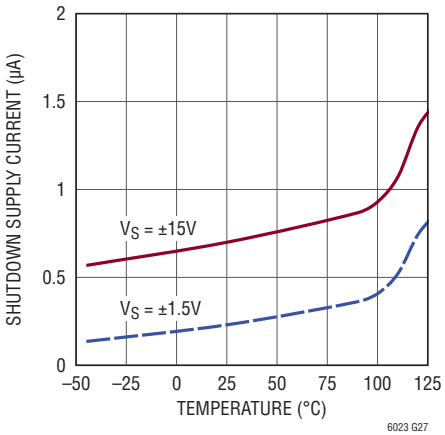
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, R_L = 100kΩ unless otherwise specified.

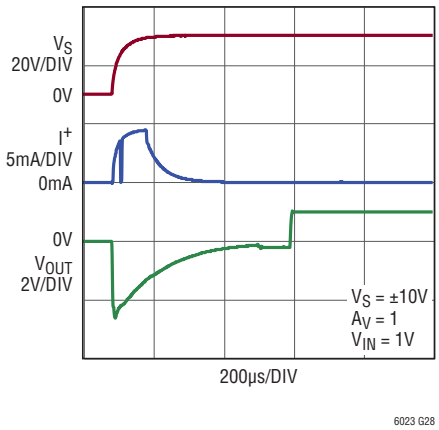
Supply Current vs Supply Voltage



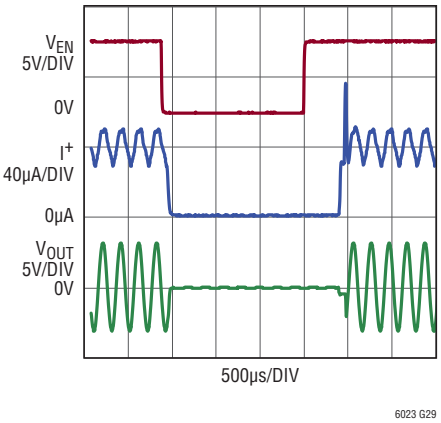
Shutdown Supply Current vs Temperature



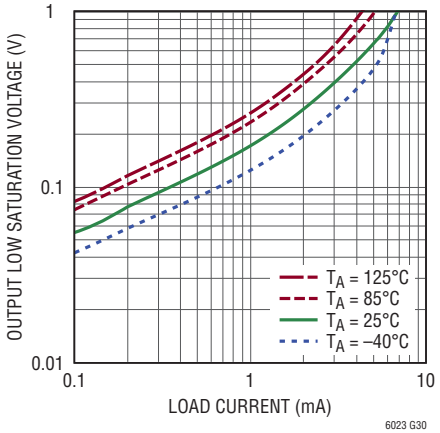
Start-Up Response



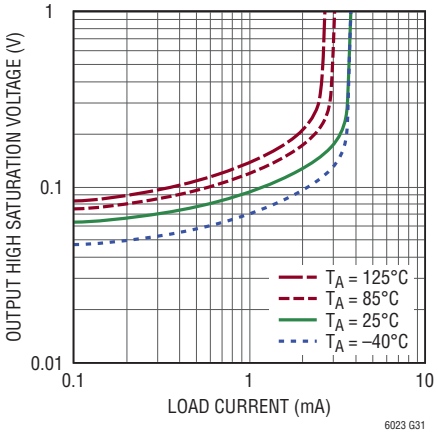
Enable/Disable Response



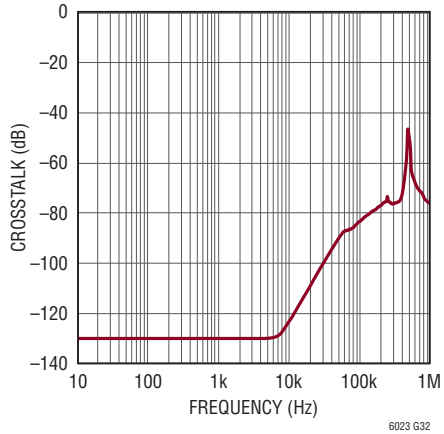
Output Saturation Voltage vs Sink Current (Output Low)



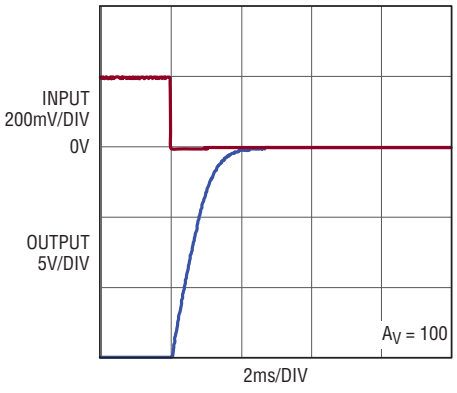
Output Saturation Voltage vs Source Current (Output High)



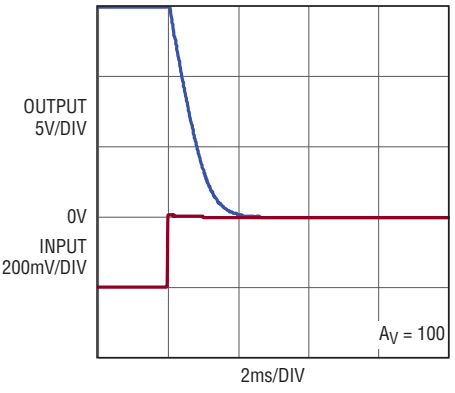
Crosstalk vs Frequency



Positive Output Overdrive Recovery



Negative Output Overdrive Recovery



PIN FUNCTIONS

OUT: Amplifier Output.

–IN: Inverting Input of the Amplifier.

+IN: Noninverting Input of the Amplifier.

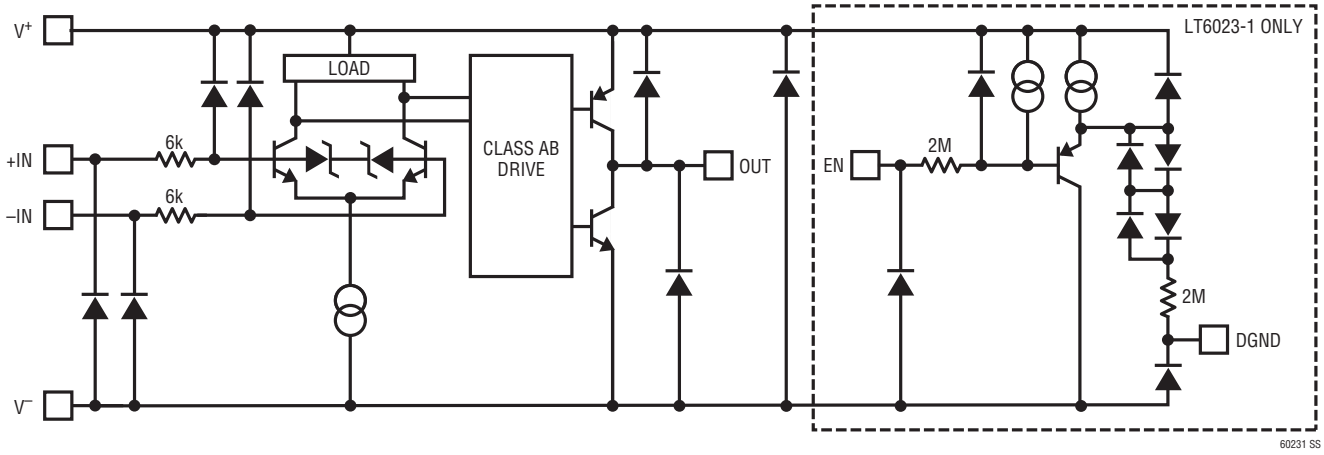
V^-: Negative Power Supply. A bypass capacitor should be used between supply pins and ground. Additional bypass capacitance may be used between the power supply pins.

DGND (LT6023-1 Only): Reference for EN Pin. It is normally tied to ground. DGND must be in the range from V^- to V^+ –3V. If grounded, V^+ must be ≥ 3V. The EN pin threshold is specified with respect to the DGND pin. DGND cannot be floated.

EN (LT6023-1 Only): Enable Input. This pin must be connected high, normally to V^+, for the amplifiers to be functional. EN is active high with the threshold approximately two diodes above DGND. EN cannot be floated. The shutdown threshold voltage is specified with respect to the voltage on the DGND pin.

V^+: Positive Power Supply. A bypass capacitor should be used between supply pins and ground. Additional bypass capacitance may be used between the power supply pins.

SIMPLIFIED SCHEMATIC



APPLICATIONS INFORMATION

Preserving Low Power Operation

The proprietary circuitry used in the LT6023 provides an excellent combination of low power, low offset and enhanced slew rate. Normally an amplifier with higher supply current would be required to achieve this combination of slew rate and precision. Special care must be taken to ensure that the low power operation is preserved.

The choice of feedback resistor values impacts several op-amp parameters as noted in the feedback components section. It should also be noted that the output of the amplifier must drive this network. For example, in a gain of two with a total feedback resistance of 10kΩ and an output voltage of 14V, the amplifier's output will need to supply 1.4mA of current. This current will ultimately come from a supply.

The supply current of the LT6023 increases with large differential input voltages. Normally, this does not impact the low power nature of the LT6023 because the amplifier is forcing the two inputs to be at the same potential. Conditions which cause differential input voltage to appear should be avoided in order to preserve the low power dissipation of the LT6023. This includes but is not limited to: operation as a comparator, excessive loading on the output and overdriving the input.

Enhanced Slew Rate

The LT6023 uses a proprietary input stage which provides an enhanced slew rate without sacrificing input precision specs such as input offset voltage, common mode rejection and noise. The unique input stage of the LT6023 allows the output to quickly slew to its final value when large signal input steps are applied. This enhanced slew characteristic allows the LT6023 to quickly settle the output to 0.0015% independent of input step size as shown in Figure 1. Typical micropower amplifiers cannot process large amplitude signals with this speed. As shown in the Typical Performance curves, when the LT6023 is configured in unity gain and a 10V step is applied to the input the output will slew at 1.4V/µs. In this same configuration, a 5V input step will slew the output at 0.65V/µs. Furthermore, a 0.7V input step will lower the slew rate to 0.02V/µs. Note that for these smaller inputs the LT6023 slew rate approaches the slew rate more common in traditional micropower amplifiers.

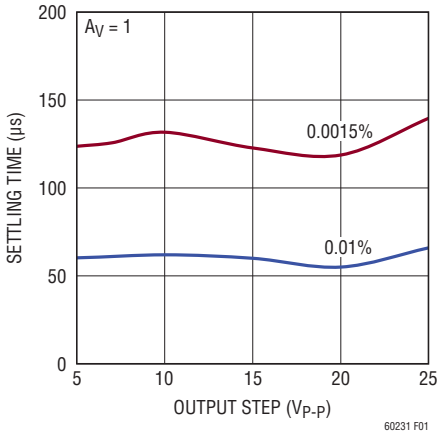


Figure 1. Settling Time Is Essentially Flat

Input Bias Current

The design of the input stage of the LT6023 is more sophisticated than that shown in the Simplified Schematic. It uses both NPN and PNP input differential amplifiers to sense the input differential voltage. As a result the specified input bias current may flow in or out of the input pins.

Multiplexer Applications/High Dynamic Input Impedance

The LT6023 has features which make it desirable for multiplexer applications, such as the application featured on the front page of this data sheet. When the channels of the multiplexer are cycled, the output of the multiplexer can produce large voltage transitions. Normally, bipolar amplifiers have back-to-back diodes between the inputs, which will turn on when the input transient voltage exceeds 0.7V, causing a large transient current to be conducted from the amplifier output stage back into the input driving circuitry. The driving circuitry then needs to absorb this current and settle before the amplifier can settle. The LT6023 uses 5.5V Zener diodes to protect its inputs which dramatically increases its input impedance with input steps as large as 5V.

APPLICATIONS INFORMATION

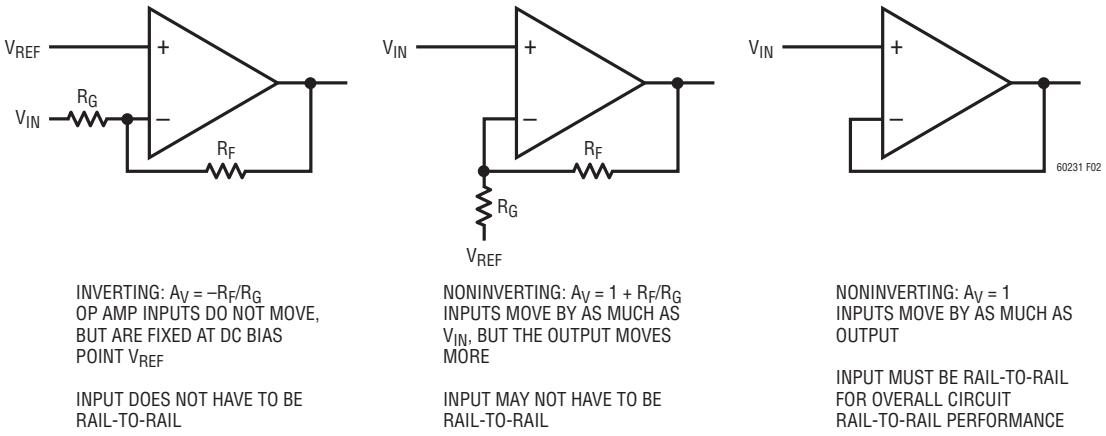


Figure 2. Some Op Amp Configurations Do Not Require Rail-to-Rail Inputs to Achieve Rail-to-Rail Outputs

Achieving Rail-to-Rail Operation without Rail-to-Rail Inputs

The LT6023 output is able to swing close to each power supply rail, but the input stage is limited to operating between V^- + 1.2V and V^+ – 1.4V. For many inverting applications and noninverting gain applications, this is largely inconsequential. Figure 2 shows the basic op amp configurations, what happens to the op amp inputs and whether or not the op amp must have rail-to-rail inputs.

The circuit of Figure 3 shows an extreme example of the inverting case. The input voltage at the 100k resistor can swing ±13.5V and the LT6023 will output an inverted, divided-by-ten version of the input voltage. The output accuracy is limited by the resistors shown to 0.2%. Output referred, this error becomes 2.7mV. The 30µV input offset voltage contribution, plus the additional error due to input bias current times the ~10k effective source impedance, contribute only negligibly to error.

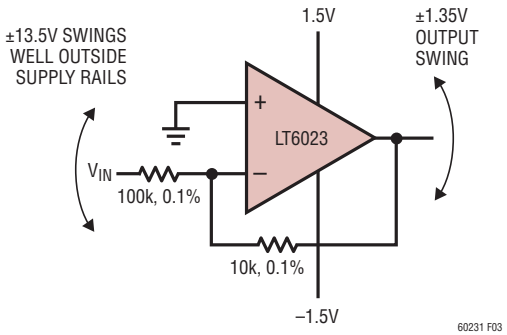


Figure 3. Extreme Inverting Case: Circuit Operates Properly with Input Voltage Swing Well Outside Op Amp Supply Rails

Phase Inversion

The LT6023 input stage is limited to operating between V^- + 1.2V and V^+ – 1.4V. Exceeding this common mode range will cause the open loop gain to drop significantly. For a unity gain amplifier, the output roughly tracks the input well beyond the specified input voltage range as shown in Figure 4.

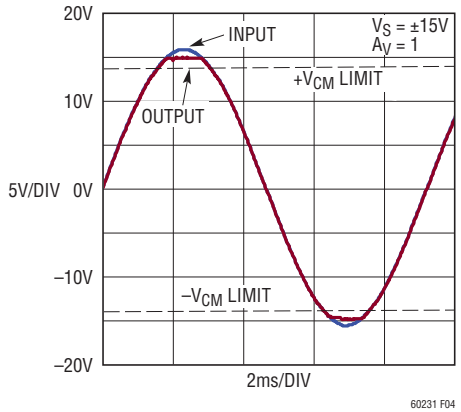


Figure 4. No Phase Inversion

APPLICATIONS INFORMATION

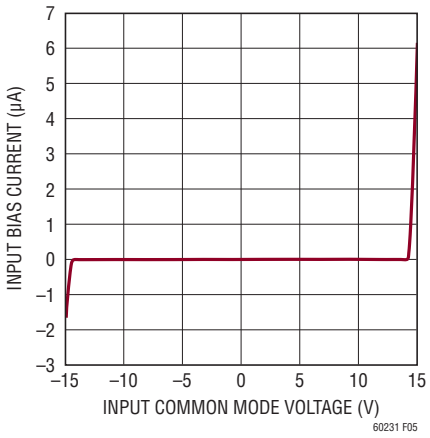


Figure 5. Increased Ib Beyond VICM

However the open loop gain is significantly reduced. While the output roughly tracks the input, the reduction in open loop gain degrades the accuracy of the LT6023 in this region. Exceeding the input common mode range also causes a significant increase in input bias current as shown in Figure 5. The output of the LT6023 is guaranteed over the specified temperature range not to phase invert as long as the input voltage does not exceed the supply voltage.

Preserving Input Precision

Preserving the input accuracy of the LT6023 requires that the application circuit and PC board layout do not introduce errors comparable to or greater than the offset of the amplifiers. Temperature differentials across the input connections can generate thermocouple voltages of tens of microvolts so the connections of the input leads should be short, close together and away from heat dissipating components. Air currents across the board can also generate temperature differentials.

As is the case with all amplifiers, a change in load current changes the finite open loop gain. Increased load current reduces the open loop gain as seen in the Typical Performance Characteristics section. This results in a change in input offset voltage. Under large signal conditions with load currents of ±1mA the effective change in input error is just tens of microvolts. In precision applications it is important to consider amplifier loading when selecting feedback resistor values as well as the loads on the device.

Feedback Components

Care must be taken to ensure that the phase shift formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example, in a gain of +2 configuration, with 1M feedback resistors and a poorly designed circuit board layout with parasitic capacitance of 10pF (amplifier + PC board) at the amplifier's inverting input will cause the amplifier to have poor phase margin due to a pole formed at 32kHz. An additional capacitor of 10pF across the feedback resistor as shown in Figure 6 will eliminate any ringing or oscillation.

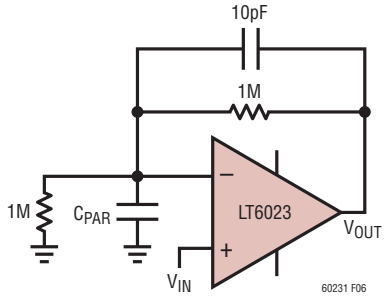


Figure 6. Stability with Parasitic Input Capacitance

Capacitive Loads

The LT6023 can drive capacitive loads up to 100pF in unity gain. The capacitive load driving capability increases as the amplifier is used in higher gain configurations. A small series resistance between the output and the load will further increase the amount of capacitance that the amplifier can drive.

APPLICATIONS INFORMATION

Shutdown Operation (LT6023-1)

The LT6023-1 shutdown function has been designed to be easily controlled from single supply logic or microcontollers. To enable the LT6023-1 when V_{DGND} = 0V the enable pin must be driven above 1.7V. Conversely, to enter the low power shutdown mode the enable pin must be driven below 0.8V. In a ±15V dual supply application where V_{DGND} = –15V, the enable pin must be driven above ~ –13.3V to enable the LT6023-1. If the enable pin is driven below –14.2V the LT6023-1 enters the low power shutdown mode. Note that to enable the LT6023-1 the enable pin voltage can range from –13.3V to 15V whereas to disable the LT6023-1 the enable pin can range from –15V to –14.2V. Figure 7 shows examples of enable pin control. While in shutdown, the outputs of the LT6023-1 are high impedance.

The LT6023-1 is typically capable of coming out of shutdown within 480µs. This is useful in power sensitive applications where duty cycled operation is employed such as wireless mesh networks. In these applications the system is in low power mode the majority of the time, but then needs to wake up quickly and settle for an acquisition before being powered back down to save power.

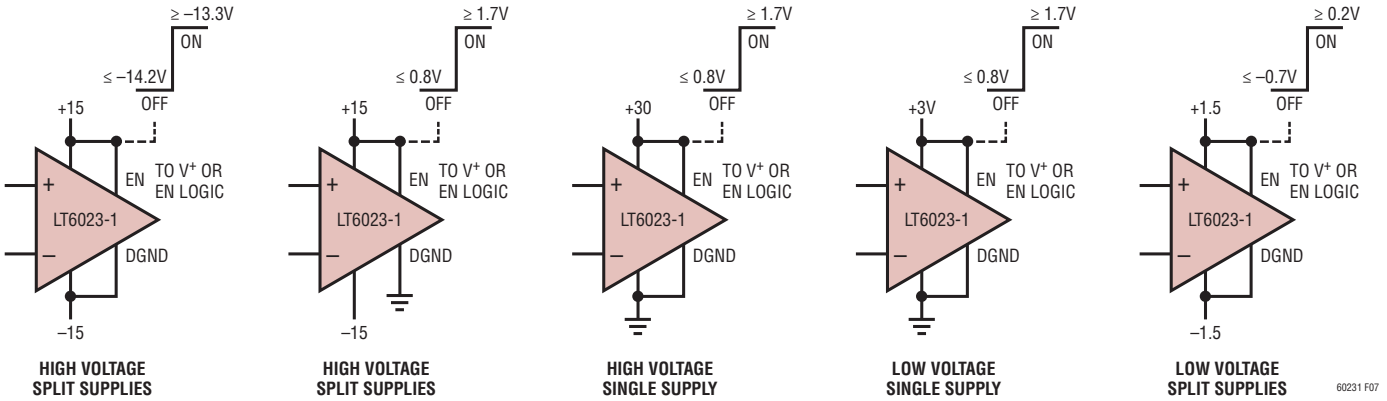
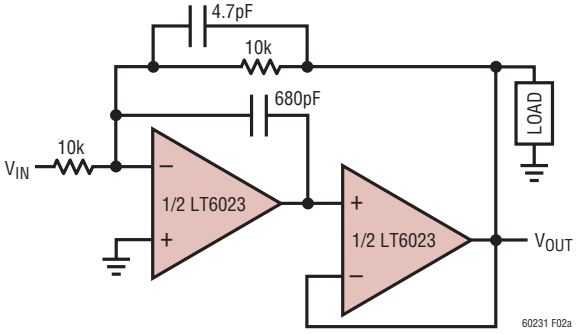


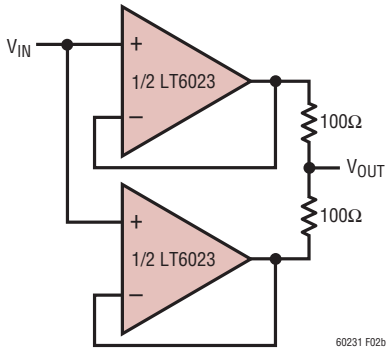
Figure 7. LT6023-1 Enable Pin Control Examples

TYPICAL APPLICATIONS

High Open-Loop Gain Composite Amplifier

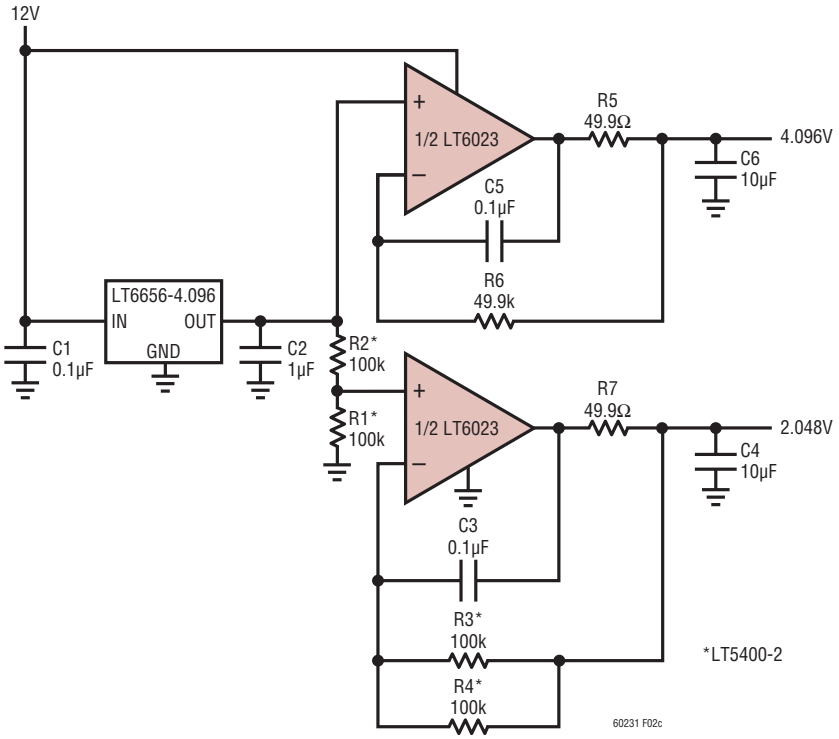


Parallel Amplifiers Achieves 93nV/√Hz Noise, Doubles Output Drive and Lowers Offset



TYPICAL APPLICATIONS

Micropower Reference Divider/Buffer



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
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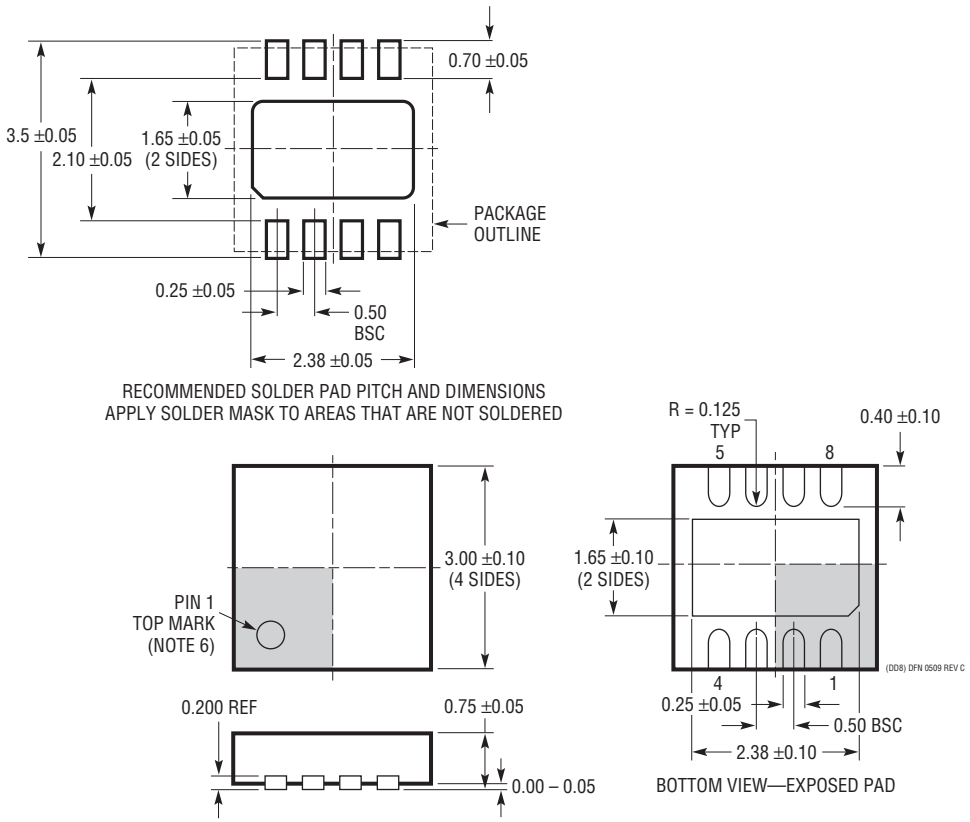
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
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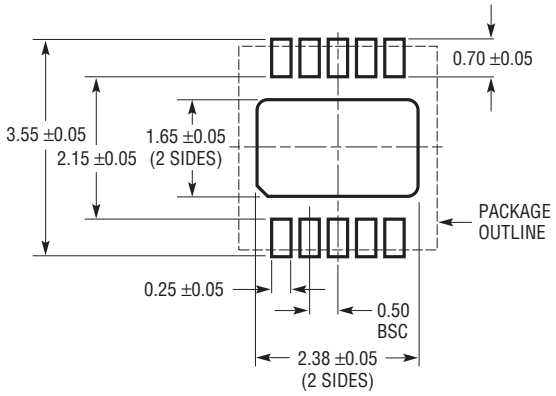
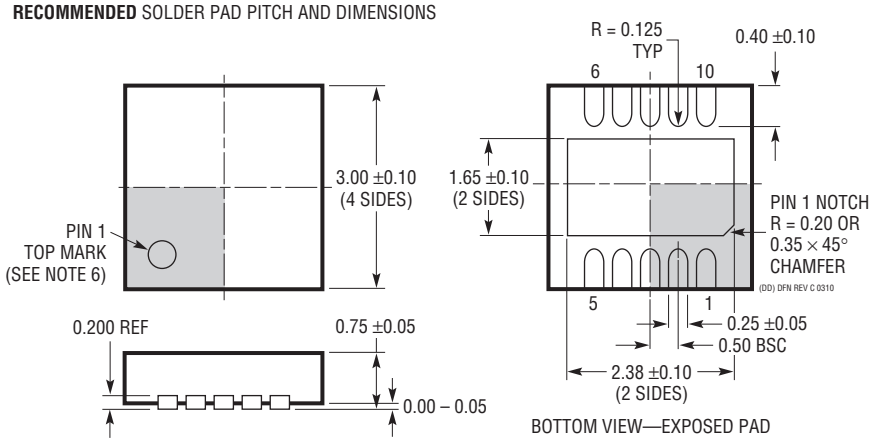
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



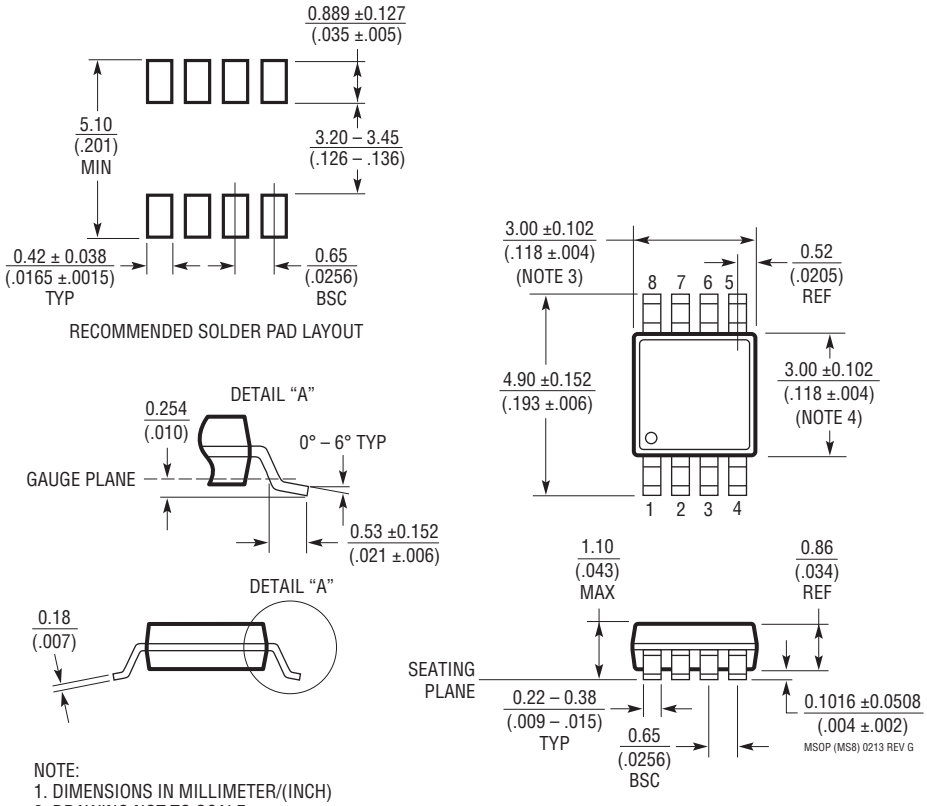
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)



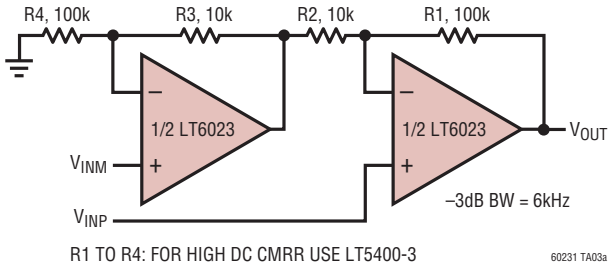
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

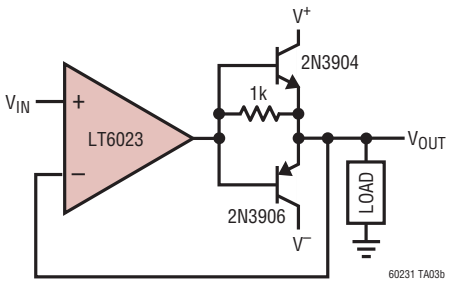
REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/15	Updated typical slew rate to be consistent throughout the data sheet	1, 4
		Corrected negative supply voltage on front page circuit	1
		Corrected Input Bias Current vs. Differential Input Voltage graph	8

TYPICAL APPLICATION

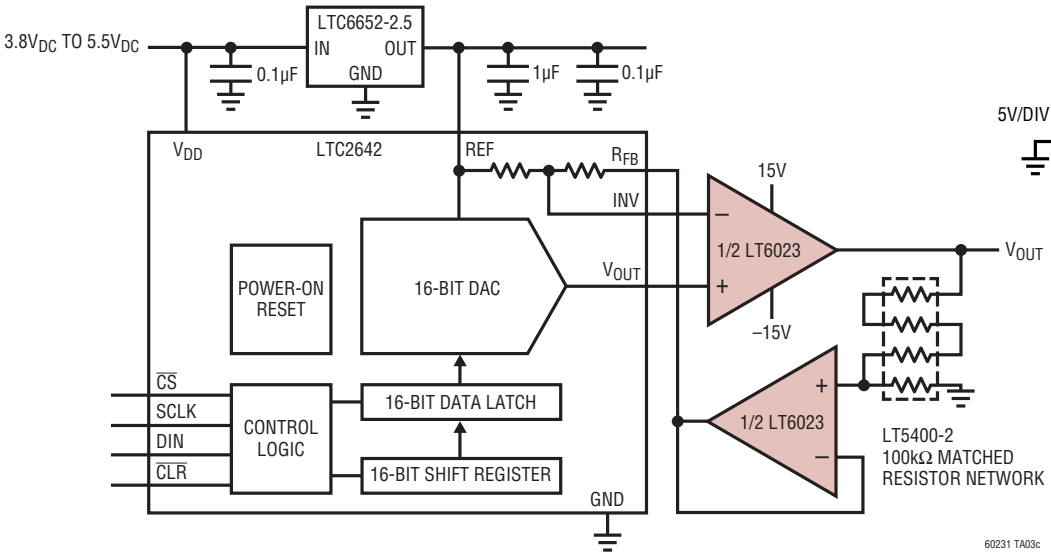
Gain of 11 Instrumentation Amplifier



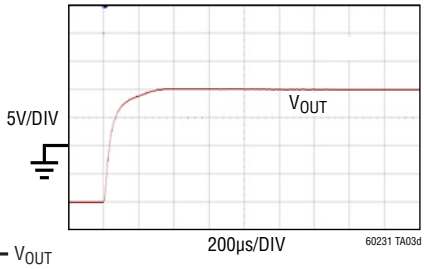
Improved Load Drive Capability



16-Bit DAC with ±10V Output Swing



20V Output Step Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT6004	2kHz, 1µA RRIO Op Amp	V_{OS}: 500µV, GBW: 2kHz, SR: 0.8V/ms, e_n: 325nV/√Hz, I_S: 1µA
LT1490A	200kHz, 50µA RRIO Op Amp	V_{OS}: 500µV, GBW: 200kHz, SR: 0.06V/µs, e_n: 50nV/√Hz, I_S: 50µA
LTC6256	6.5MHz, 65µA RRIO Op Amp	V_{OS}: 350µV, GBW: 6.5MHz, SR: 1.8V/µs, e_n: 20nV/√Hz, I_S: 65µA
LT6020	400kHz, 100µA, 5V/µs Op Amp	V_{OS}: 30µV, GBW: 400kHz, SR: 5V/µs, e_n: 46nV/√Hz, I_S: 100µA
LTC2055	500kHz, 150µA Zero-Drift Op Amp	V_{OS}: 3µV, GBW: 500kHz, SR: 0.5V/µs, I_S: 150µA
LT1783	1.2MHz, 230µA Over-The-Top RRIO Op Amp	V_{OS}: 600µV, GBW: 1.2MHz, SR: 0.4V/µs, e_n: 20nV/√Hz, I_S: 230µA
LT1352	3MHz. 200V/µs Op Amp	V_{OS}: 600µV, GBW: 3MHz, SR: 200V/µs, e_n: 14nV/√Hz, I_S: 330µA
LT1492	5MHz, 3V/µs Op Amp	V_{OS}: 180µV, GBW: 5MHz, SR: 3V/µs, e_n: 16.5nV/√Hz, I_S: 550µA
LTC5800	SmartMesh® Wireless Sensor Network I_C	Wireless Mesh Networks
LT5400	Quad Matched Resistor Network	0.01% Matching