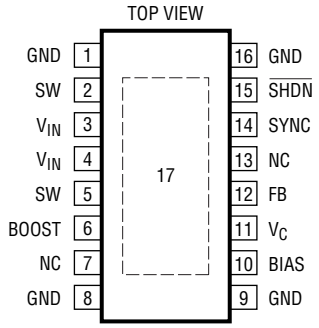
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage (V_{IN}) 60V
BOOST Pin Above SW (Note 11)..... 35V
BOOST Pin Voltage 68V
SYNC Voltage..... 7V
$\overline{SHDN}$ Voltage 6V
BIAS Pin Voltage 30V
FB Pin Voltage/Current 3.5V/2mA
Operating Junction Temperature Range
LT3430EFE (Notes 8, 10) .....–40°C to 125°C
LT3430IFE (Notes 8, 10) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER PART NUMBER	FE PART MARKING
LT3430EFE LT3430IFE LT3430EFE-1 LT3430IFE-1	3430EFE 3430IFE 3430EFE-1 3430IFE-1

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 15V, V_C = 1.5V, $\overline{SHDN}$ = 1V, BOOST = Open Circuit, SW = Open Circuit, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage (V_{REF})	V_{OL} + 0.2 ≤ V_C ≤ V_{OH} – 0.2 5.5V ≤ V_{IN} ≤ 60V	 ●	1.204 1.195	1.219	1.234 1.243	V
FB Input Bias Current		●		–0.2	–1.5	µA
Error Amp Voltage Gain	(Note 2)		200	400		V/V
Error Amp g_m	dI (V_C) = ±10µA	 ●	1650 1000	2200	3300 4200	µMho µMho
V_C to Switch g_m				3.4		A/V
EA Source Current	FB = 1V	●	125	225	450	µA
EA Sink Current	FB = 1.4V	●	100	225	500	µA
V_C Switching Threshold	Duty Cycle = 0			0.9		V
V_C High Clamp	$\overline{SHDN}$ = 1V			2.1		V
Switch Current Limit	V_C Open, Boost = V_{IN} + 5V, FB = 1V –40°C ≤ T_J ≤ 25°C T_J = 125°C (Note 9)		 3 2.5	 5 4	 6.5 5.5	 A A
Switch On Resistance	I_{SW} = 2.5A, Boost = V_{IN} + 5V (Note 7)			0.1	0.14 0.18	Ω Ω
Maximum Switch Duty Cycle (LT3430)	FB = 1V	 ●	93 90	96		% %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 15V, V_C = 1.5V, $\overline{SHDN}$ = 1V, BOOST = Open Circuit, SW = Open Circuit, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Switch Duty Cycle (LT3430-1)		 ●	96 94	98		% %
Switch Frequency (LT3430)	V_C Set to Give DC = 50%	 ●	184 172	200 200	216 228	kHz kHz
Switch Frequency (LT3430-1)		 ●	88 85	100 100	115 120	kHz kHz
f_{SW} Line Regulation	5.5V ≤ V_{IN} ≤ 60V	●		0.05	0.15	%/V
f_{SW} Shifting Threshold	Df = 10kHz			0.8		V
Minimum Input Voltage	(Note 3)	●		4.6	5.5	V
Minimum Boost Voltage	(Note 4) I_{SW} ≤ 2.5A	●		1.8	3	V
Boost Current (Note 5)	Boost = V_{IN} + 5V, I_{SW} = 0.75A Boost = V_{IN} + 5V, I_{SW} = 2.5A	● ●		25 75	50 120	mA mA
Input Supply Current (I_{VIN})	(Note 6) V_{BIAS} = 5V			1.5	2.2	mA
Bias Supply Current (I_{BIAS})	(Note 6) V_{BIAS} = 5V			3.1	4.2	mA
Shutdown Supply Current	$\overline{SHDN}$ = 0V, V_{IN} ≤ 60V, SW = 0V, V_C Open	 ●		30	100 200	µA µA
Lockout Threshold	V_C Open	●	2.3	2.42	2.53	V
Shutdown Threshold	V_C Open, Shutting Down V_C Open, Starting Up	● ●	0.15 0.25	0.37 0.42	0.58 0.60	V V
Minimum SYNC Amplitude				1.5		V
SYNC Frequency Range (LT3430)			228		700	kHz
SYNC Frequency Range (LT3430-1)			125		250	kHz
SYNC Input Resistance				20		kΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Gain is measured with a V_C swing equal to 200mV above the low clamp level to 200mV below the upper clamp level.

Note 3: Minimum input voltage is not measured directly, but is guaranteed by other tests. It is defined as the voltage where internal bias lines are still regulated so that the reference voltage and oscillator remain constant. Actual minimum input voltage to maintain a regulated output will depend upon output voltage and load current. See Applications Information.

Note 4: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the internal power switch.

Note 5: Boost current is the current flowing into the BOOST pin with the pin held 5V above input voltage. It flows only during switch on time.

Note 6: Input supply current is the quiescent current drawn by the input pin when the BIAS pin is held at 5V with switching disabled. Bias supply current is the current drawn by the BIAS pin when the BIAS pin is held at 5V. Total input referred supply current is calculated by summing input supply current (I_{VIN}) with a fraction of bias supply current (I_{BIAS}):

$$I_{TOTAL} = I_{VIN} + (I_{BIAS})(V_{OUT}/V_{IN})$$

With V_{IN} = 15V, V_{OUT} = 5V, I_{VIN} = 1.4mA, I_{BIAS} = 2.9mA, I_{TOTAL} = 2.4mA.

Note 7: Switch on resistance is calculated by dividing V_{IN} to SW voltage by the forced current (3A). See Typical Performance Characteristics for the graph of switch voltage at other currents.

Note 8: The LT3430EFE/LT3430EFE-1 are guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3430IFE/LT3430IFE-1 are guaranteed over the full –40°C to 125°C operating junction temperature range.

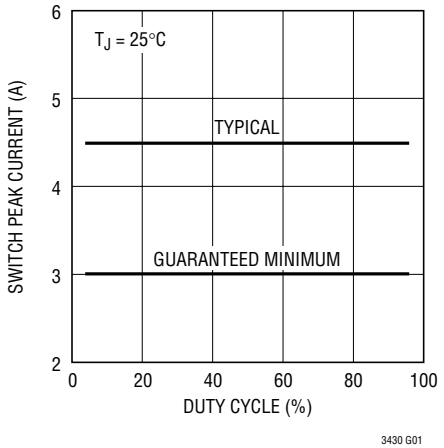
Note 9: See Peak Switch Current Limit vs Junction Temperature graph in the Typical Performance Characteristics section.

Note 10: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 11: The maximum operational Boost-SW voltage is limited by thermal and load current constraints. See 'Boost Pin' and 'Thermal Calculations' in the Applications Information section.

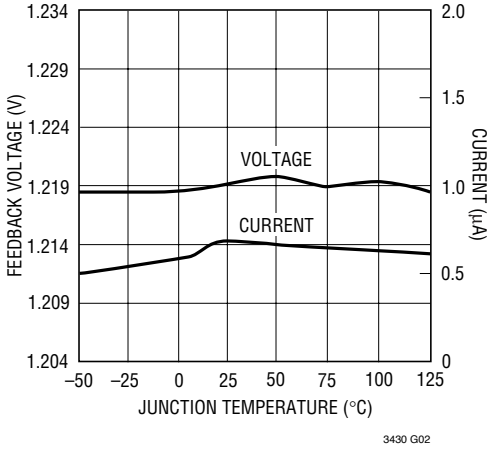
TYPICAL PERFORMANCE CHARACTERISTICS

Switch Peak Current Limit



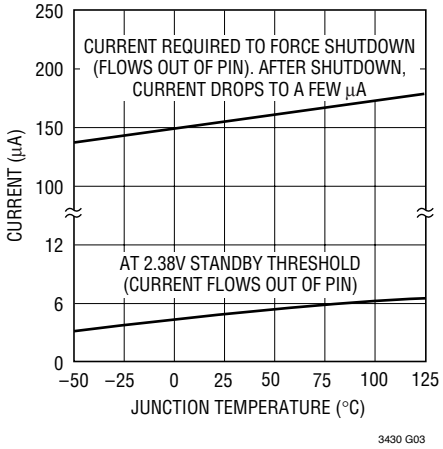
3430 G01

FB Pin Voltage and Current



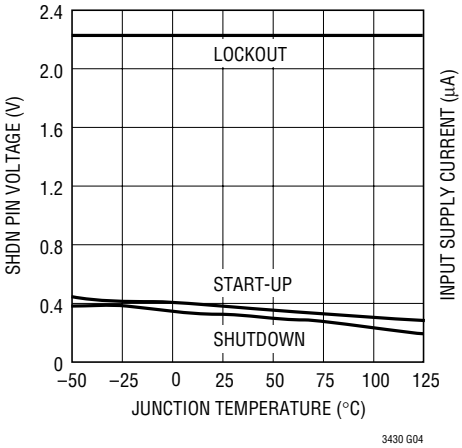
3430 G02

$\overline{SHDN}$ Pin Bias Current



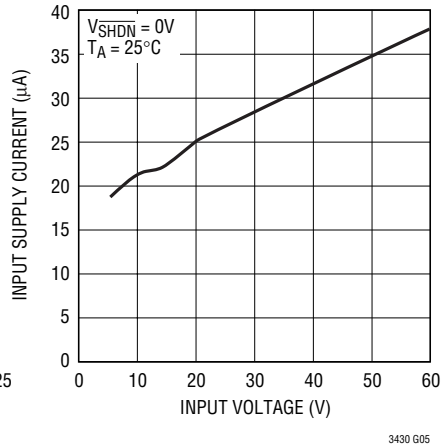
3430 G03

Lockout and Shutdown Threshold



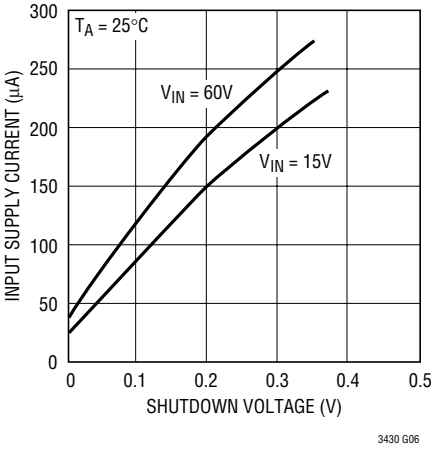
3430 G04

Shutdown Supply Current



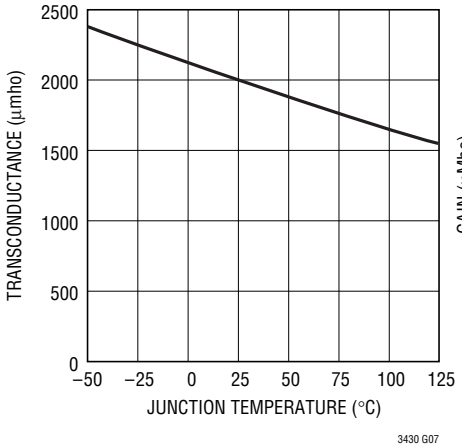
3430 G05

Shutdown Supply Current



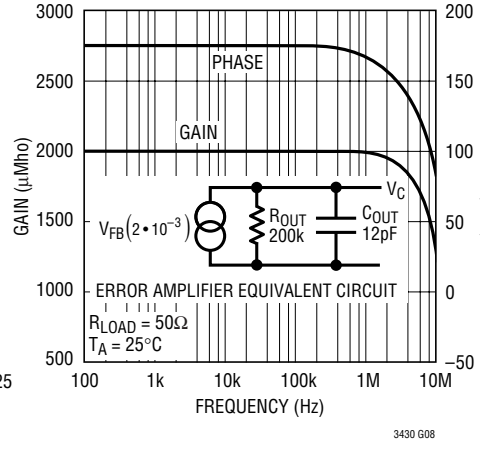
3430 G06

Error Amplifier Transconductance



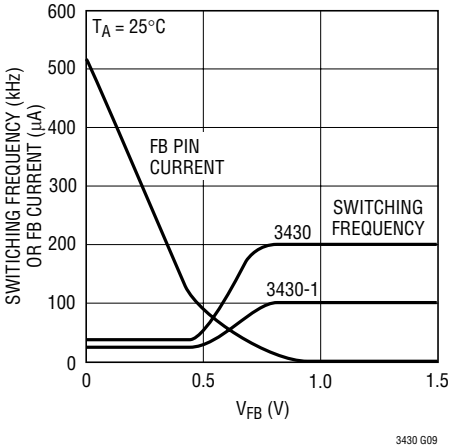
3430 G07

Error Amplifier Transconductance



3430 G08

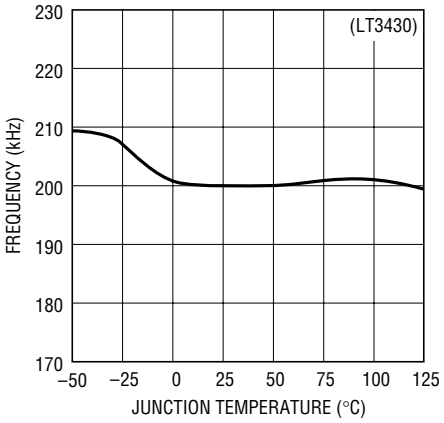
Frequency Foldback



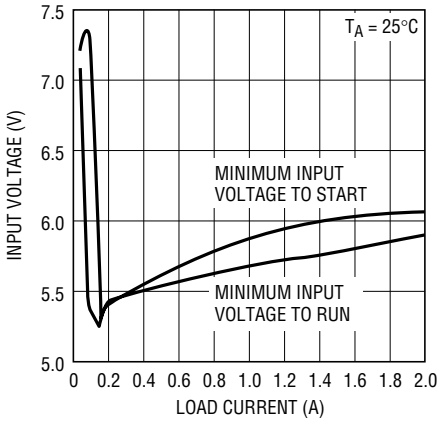
3430 G09

TYPICAL PERFORMANCE CHARACTERISTICS

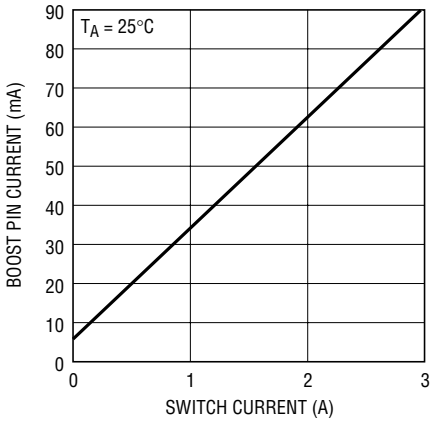
Switching Frequency



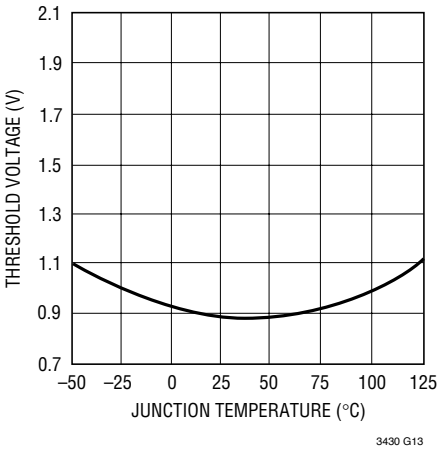
Minimum Input Voltage with 5V Output



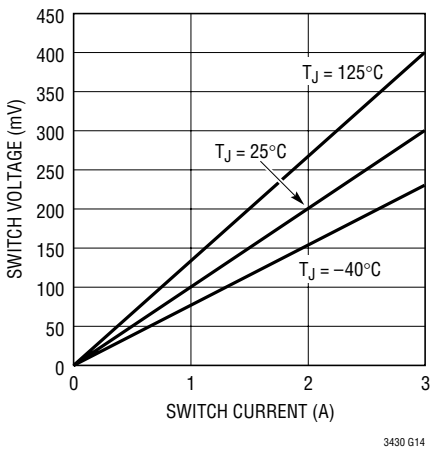
BOOST Pin Current



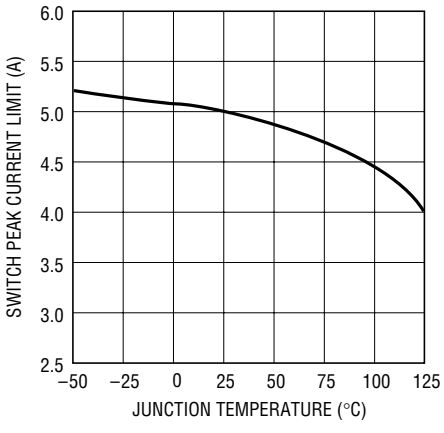
V_C Pin Shutdown Threshold



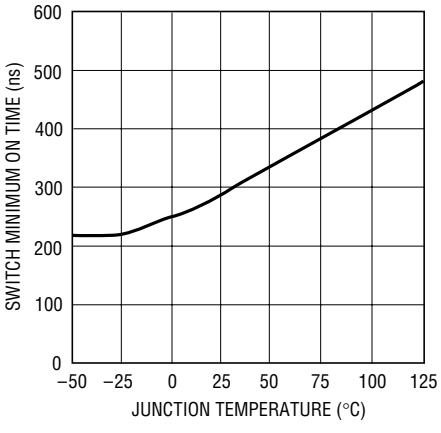
Switch Voltage Drop



Switch Peak Current Limit



Switch Minimum ON Time vs Temperature



PIN FUNCTIONS

GND (Pins 1, 8, 9, 16, 17): The GND pin connections act as the reference for the regulated output, so load regulation will suffer if the "ground" end of the load is not at the same voltage as the GND pins of the IC. This condition will occur when load current or other currents flow through metal paths between the GND pins and the load ground. Keep the paths between the GND pins and the load ground short and use a ground plane when possible. The FE package has an exposed pad that is fused to the GND pins. The pad (Pin 17) should be soldered to the copper ground plane under the device to reduce thermal resistance. (See Applications Information—Layout Considerations.)

SW (Pins 2, 5): The switch pin is the emitter of the on-chip power NPN switch. This pin is driven up to the input pin voltage during switch on time. Inductor current drives the switch pin voltage negative during switch off time. Negative voltage is clamped with the external catch diode. Maximum negative switch voltage allowed is –0.8V.

V_{IN} (Pins 3, 4): This is the collector of the on-chip power NPN switch. V_{IN} powers the internal control circuitry when a voltage on the BIAS pin is not present. High dI/dt edges occur on this pin during switch turn on and off. Keep the path short from the V_{IN} pin through the input bypass capacitor, through the catch diode back to SW. All trace inductance in this path creates voltage spikes at switch off, adding to the V_{CE} voltage across the internal NPN.

BOOST (Pin 6): The BOOST pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch. Without this added voltage, the typical switch voltage loss would be about 1.5V. The additional BOOST voltage allows the switch to saturate and voltage loss approximates that of a 0.1Ω FET structure.

NC (Pins 7, 13): No Connection.

BIAS (Pin 10): The BIAS pin is used to improve efficiency when operating at higher input voltages and light load current. Connecting this pin to the regulated output voltage forces most of the internal circuitry to draw its operating current from the output voltage rather than the input supply. This architecture increases efficiency especially when the input voltage is much higher than the output. Minimum output voltage setting for this mode of operation is 3V.

V_C (Pin 11): The V_C pin is the output of the error amplifier and the input of the peak switch current comparator. It is normally used for frequency compensation, but can also serve as a current clamp or control loop override. V_C sits at about 0.9V for light loads and 2.1V at maximum load. It can be driven to ground to shut off the regulator, but if driven high, current must be limited to 4mA.

FB (Pin 12): The feedback pin is used to set the output voltage using an external voltage divider that generates 1.22V at the pin for the desired output voltage. Three additional functions are performed by the FB pin. When the pin voltage drops below 0.6V, switch current limit is reduced and the external SYNC function is disabled. Below 0.8V, switching frequency is also reduced. See Feedback Pin Functions in Applications Information for details.

SYNC (Pin 14): The SYNC pin is used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 10% and 90% duty cycle. The synchronizing range is 125kHz to 250kHz for the LT3430-1 and 228kHz to 700kHz for the LT3430. See Synchronizing in Applications Information for details.

$\overline{\text{SHDN}}$ (Pin 15): The $\overline{\text{SHDN}}$ pin is used to turn off the regulator and to reduce input drain current to a few microamperes. This pin has two thresholds: one at 2.38V to disable switching and a second at 0.4V to force complete micropower shutdown. The 2.38V threshold functions as an accurate undervoltage lockout (UVLO); sometimes used to prevent the regulator from delivering power until the input voltage has reached a predetermined level.

If the $\overline{\text{SHDN}}$ pin functions are not required, the pin can either be left open (to allow an internal bias current to lift the pin to a default high state) or be forced high to a level not to exceed 6V.

BLOCK DIAGRAM

The LT3430/LT3430-1 are constant frequency, current mode buck converters. This means that there is an internal clock and two feedback loops that control the duty cycle of the power switch. In addition to the normal error amplifier, there is a current sense amplifier that monitors switch current on a cycle-by-cycle basis. A switch cycle starts with an oscillator pulse which sets the R_S flip-flop to turn the switch on. When switch current reaches a level set by the inverting input of the comparator, the flip-flop is reset and the switch turns off. Output voltage control is obtained by using the output of the error amplifier to set the switch current trip point. This technique means that the error amplifier commands current to be delivered to the output rather than voltage. A voltage fed system will have low phase shift up to the resonant frequency of the inductor and output capacitor, then an abrupt 180° shift will occur. The current fed system will have 90° phase shift at a much lower frequency, but will not have the additional 90° shift until well beyond the LC resonant frequency. This makes it much easier to frequency compensate the feedback loop and also gives much quicker transient response.

Most of the circuitry of the LT3430/LT3430-1 operates from an internal 2.9V bias line. The bias regulator normally draws power from the regulator input pin, but if the BIAS pin is connected to an external voltage equal to or higher than 3V, bias power will be drawn from the external source (typically the regulated output voltage). This will improve efficiency if the BIAS pin voltage is lower than regulator input voltage.

High switch efficiency is attained by using the BOOST pin to provide a voltage to the switch driver which is higher than the input voltage, allowing switch to be saturated. This boosted voltage is generated with an external capacitor and diode. Two comparators are connected to the shutdown pin. One has a 2.38V threshold for undervoltage lockout and the second has a 0.4V threshold for complete shutdown.

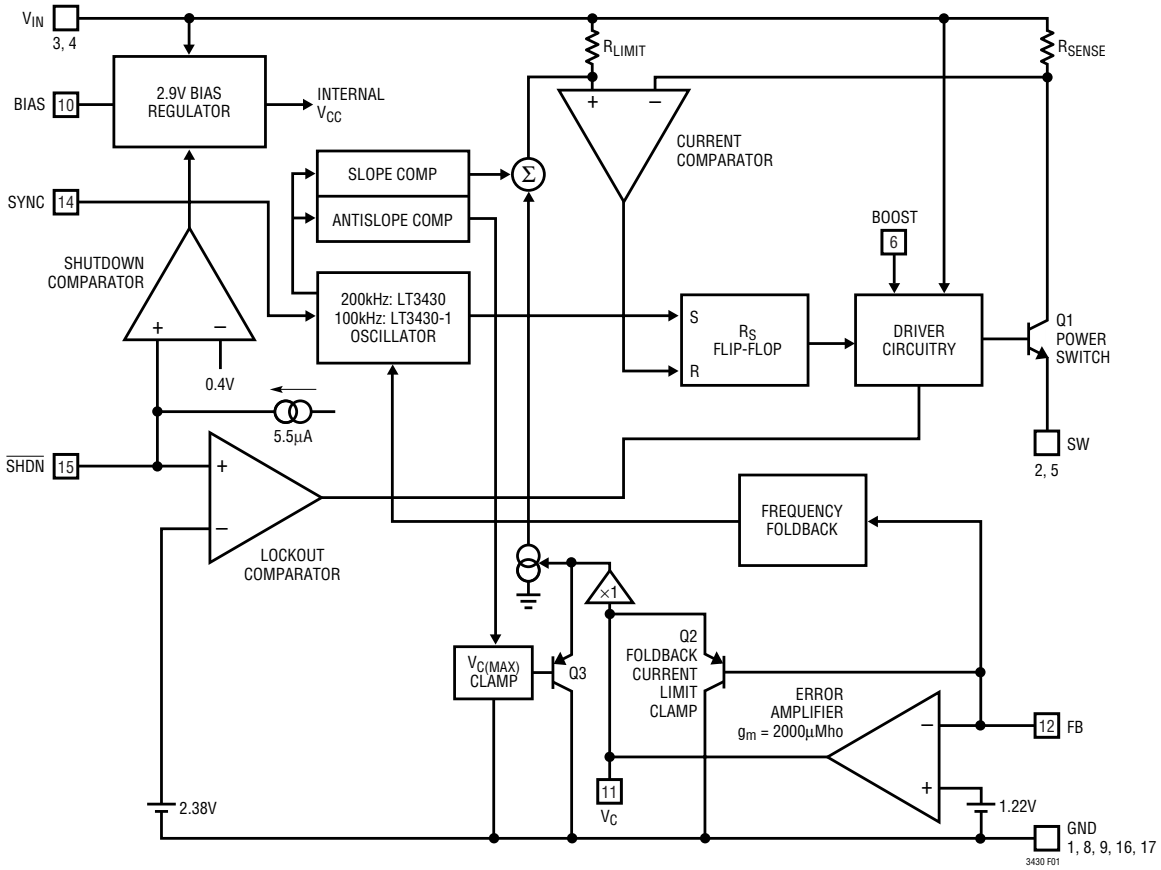


Figure 1. LT3430/LT3430-1 Block Diagram

APPLICATIONS INFORMATION

FEEDBACK PIN FUNCTIONS

The feedback (FB) pin on the LT3430/LT3430-1 is used to set output voltage and provide several overload protection features. The first part of this section deals with selecting resistors to set output voltage and the second part talks about foldback frequency and current limiting created by the FB pin. Please read both parts before committing to a final design.

The suggested value for the LT3430 output divider resistor (see Figure 2) from FB to ground (R2) is 5k or less, and a formula for R1 is shown below. For the LT3430-1, choose the resistors so that the Thevinin resistance of the divider at the feedback pin is 7.5kΩ. The output voltage error caused by ignoring the input bias current on the FB pin is less than 0.25% with R2 = 5k. A table of standard 1% values is shown in Table 1 for common output voltages. Please read the following if divider resistors are increased above the suggested values.

$$R1 = \frac{R2(V_{OUT} - 1.22)}{1.22}$$

Table 1. *LT3430, **LT3430-1

OUTPUT VOLTAGE (V)	R2 (kΩ)	R1 (NEAREST 1%) (kΩ)	% ERROR AT OUTPUT DUE TO DISCREET 1% RESISTOR STEPS
3*	4.99	7.32	+0.32
3.3*	4.99	8.45	–0.43
5*	4.99	15.4	–0.30
12*	4.12	46.4	–0.27
3**	12.7	18.7	+0.54
3.3**	12.1	20.5	–0.40
5**	10	30.9	–0.20
12**	8.25	73.2	+0.37

More Than Just Voltage Feedback

The feedback pin is used for more than just output voltage sensing. It also reduces switching frequency and current limit when output voltage is very low (see the Frequency Foldback graph in Typical Performance Characteristics). This is done to control power dissipation in both the IC and in the external diode and inductor during short-circuit conditions. A shorted output requires the switching regulator to operate at very low duty cycles, and the average current through the diode and inductor is equal to the short-circuit current limit of the switch (typically 4A for the LT3430/LT3430-1, folding back to less than 2A). Minimum switch on time limitations would prevent the switcher from attaining a sufficiently low duty cycle if switching frequency were maintained at 200kHz (100kHz LT3430-1), so frequency is reduced by about 5:1 (3:1 LT3430-1) when the feedback pin voltage drops below 0.8V (see Frequency Foldback graph). This does not affect operation with normal load conditions; one simply sees a gear shift in switching frequency during start-up as the output voltage rises.

In addition to lower switching frequency, the LT3430/LT3430-1 also operate at lower switch current limit when the feedback pin voltage drops below 0.6V. Q2 in Figure 2 performs this function by clamping the V_C pin to a voltage less than its normal 2.1V upper clamp level. This *foldback current limit* greatly reduces power dissipation in the IC, diode and inductor during short-circuit conditions. External synchronization is also disabled to prevent interference with foldback operation. Again, it is nearly transparent to the user under normal load conditions. The only loads that may be affected are current source loads which maintain full load current with output voltage less than 50% of final value. In these rare situations the feedback pin can be clamped above 0.6V with an external diode to defeat foldback current limit. *Caution:* clamping the feedback pin means that frequency shifting will also be defeated, so a combination of high input voltage and dead shorted output may cause the LT3430/LT3430-1 to lose control of current limit.

The internal circuitry which forces reduced switching frequency also causes current to flow out of the feedback pin when output voltage is low. The equivalent circuitry is shown in Figure 2. Q1 is completely off during normal operation. If the FB pin falls below 0.8V, Q1 begins to conduct current and LT3430 reduces frequency at the rate of approximately 1.4kHz/μA. To ensure adequate frequency foldback (under worst-case short-circuit conditions), the external divider Thevinin resistance (R_{THEV}) must be low enough to pull 115μA out of the FB pin with 0.44V on the pin ($R_{THEV} \leq 3.8k$)(LT3430-1 $R_{THEV} \approx 7.5k$). *The net result is that reductions in frequency and current limit are affected by output voltage divider impedance. Cau-*

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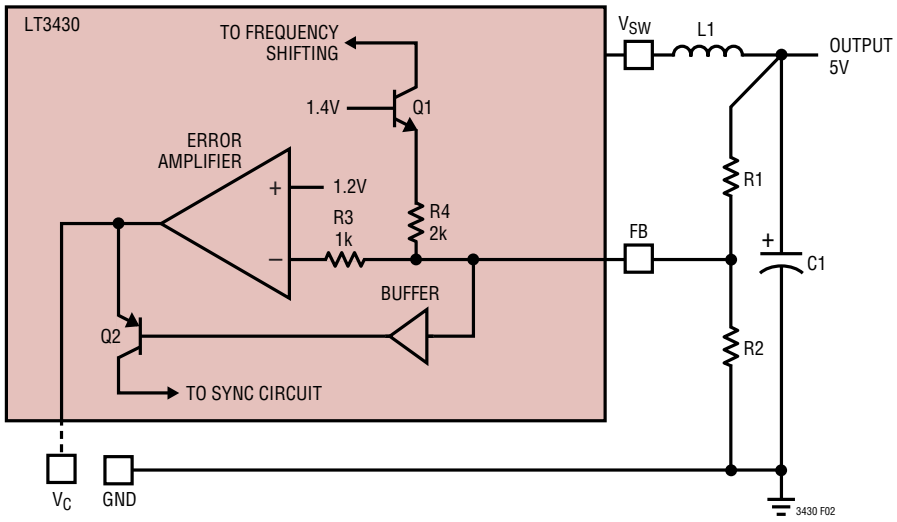

Figure 2. Frequency and Current Limit Foldback

tion should be used if resistors are increased beyond the suggested values and short-circuit conditions occur with high input voltage. High frequency pickup will increase and the protection accorded by frequency and current foldback will decrease.

Choosing the Inductor

For most applications, the output inductor will fall into the range of 5µH to 47µH (10µH to 100µH for LT3430-1). Lower values are chosen to reduce physical size of the inductor. Higher values allow more output current because they reduce peak current seen by the LT3430/LT3430-1 switch, which has a 3A limit. Higher values also reduce output ripple voltage.

When choosing an inductor you will need to consider output ripple voltage, maximum load current, peak inductor current and fault current in the inductor. In addition, other factors such as core and copper losses, allowable component height, EMI, saturation and cost should also be considered. The following procedure is suggested as a way of handling these somewhat complicated and conflicting requirements.

Output Ripple Voltage

Figure 3 shows a comparison of output ripple voltage for the LT3430/LT3430-1 using either a tantalum or ceramic output capacitor. It can be seen from Figure 3 that output ripple voltage can be significantly reduced by using the

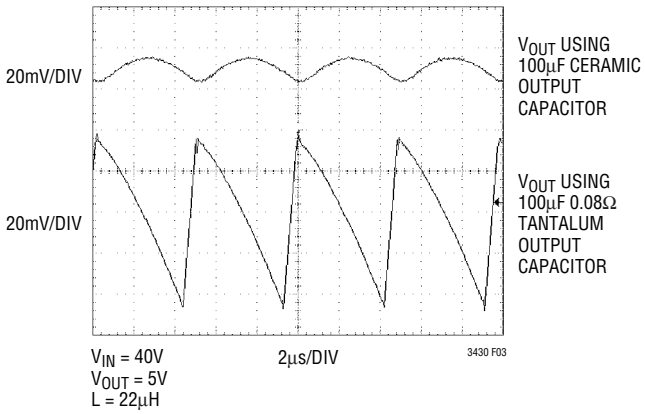

Figure 3. LT3430 Output Ripple Voltage Waveforms. Ceramic vs Tantalum Output Capacitors

ceramic output capacitor; the significant decrease in output ripple voltage is due to the very low ESR of ceramic capacitors.

Output ripple voltage is determined by ripple current (I_{LP-P}) through the inductor and the high frequency impedance of the output capacitor. At high frequencies, the impedance of the tantalum capacitor is dominated by its effective series resistance (ESR).

Tantalum Output Capacitor

The typical method for reducing output ripple voltage when using a tantalum output capacitor is to increase the inductor value (to reduce the ripple current in the inductor). The following equations will help in choosing the required

APPLICATIONS INFORMATION

inductor value to achieve a desirable output ripple voltage level. If output ripple voltage is of less importance, the subsequent suggestions in Peak Inductor and Fault Current and EMI will additionally help in the selection of the inductor value.

Peak-to-peak output ripple voltage is the sum of a triwave (created by peak-to-peak ripple current (I_{LP-P}) times ESR) and a square wave (created by parasitic inductance (ESL) and ripple current slew rate). Capacitive reactance is assumed to be small compared to ESR or ESL.

$$V_{RIPPLE} = (I_{LP-P})(ESR) + (ESL)\frac{dI}{dt}$$

where:

ESR = equivalent series resistance of the output capacitor

ESL = equivalent series inductance of the output capacitor

dI/dt = slew rate of inductor ripple current = V_{IN}/L

Peak-to-peak ripple current (I_{LP-P}) through the inductor and into the output capacitor is typically chosen to be between 20% and 40% of the maximum load current. It is approximated by:

$$I_{LP-P} = \frac{(V_{OUT})(V_{IN} - V_{OUT})}{(V_{IN})(f)(L)}$$

Example: with V_{IN} = 40V, V_{OUT} = 5V, L = 22µH, ESR = 0.080Ω and ESL = 10nH, output ripple voltage can be approximated as follows:

$$I_{P-P} = \frac{(5)(40-5)}{(40)(22 \bullet 10^{-6})(200 \bullet 10^{3})} = 0.99A$$

$$\frac{dI}{dt} = \frac{40}{22 \bullet 10^{-6}} = 10^{6} \bullet 1.8$$

$$V_{RIPPLE} = (0.99A)(0.08) + (10 \bullet 10^{-9})(10^{6})(1.8)$$

$$= 0.079 + 0.018 = 97mV_{P-P}$$

To reduce output ripple voltage further requires an increase in the inductor value with the trade-off being a physically larger inductor with the possibility of increased component height and cost.

Ceramic Output Capacitor

An alternative way to further reduce output ripple voltage is to reduce the ESR of the output capacitor by using a ceramic capacitor. Although this reduction of ESR removes a useful zero in the overall loop response, this zero can be replaced by inserting a resistor (R_C) in series with the V_C pin and the compensation capacitor C_C. (See Ceramic Capacitors in Applications Information.)

Peak Inductor Current and Fault Current

To ensure that the inductor will not saturate, the peak inductor current should be calculated knowing the maximum load current. An appropriate inductor should then be chosen. In addition, a decision should be made whether or not the inductor must withstand continuous fault conditions.

If maximum load current is 1A, for instance, a 1A inductor may not survive a continuous 4A overload condition. Dead shorts will actually be more gentle on the inductor because the LT3430/LT3430-1 have frequency and current limit foldback.

Table 2

VENDOR/ PART NO.	VALUE (µH)	I_{DC} (Amps)	DCR (Ohms)	HEIGHT (mm)
Sumida				
CDRH104R-150	15	3.6	0.050	4
CDRH104R-220	22	2.9	0.073	4
CDRH104R-330	33	2.3	0.093	4
CDRH124-220	22	2.9	0.066	4.5
CDRH124-330	33	2.7	0.097	4.5
CDRH127-330	33	3.0	0.065	8
CDRH127-470	47	2.5	0.100	8
CEI122-220	22	2.3	0.085	8
Coiltronics				
UP3B-330	33	3	0.069	6.8
UP3B-470	47	2.4	0.108	6.8
UP4B-680	68	4.3	0.120	7.9
Coilcraft				
DO3316P-153	15	3	0.046	5.2
DO5022p-683	68	3.5	0.130	7.1

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Peak switch and inductor current can be significantly higher than output current, especially with smaller inductors and lighter loads, so don't omit this step. Powdered iron cores are forgiving because they saturate softly, whereas ferrite cores saturate abruptly. Other core materials fall somewhere in between. The following formula assumes continuous mode of operation, but errs only slightly on the high side for discontinuous mode, so it can be used for all conditions.

$$I_{PEAK} = I_{OUT} + \frac{I_{LP-P}}{2} = I_{OUT} + \frac{(V_{OUT})(V_{IN} - V_{OUT})}{(2)(V_{IN})(f)(L)}$$

EMI

Decide if the design can tolerate an "open" core geometry like a rod or barrel, which have high magnetic field radiation, or whether it needs a closed core like a toroid to prevent EMI problems. This is a tough decision because the rods or barrels are temptingly cheap and small and there are no helpful guidelines to calculate when the magnetic field radiation will be a problem.

Additional Considerations

After making an initial choice, consider additional factors such as core losses and second sourcing, etc. Use the experts in Linear Technology's Applications department if you feel uncertain about the final choice. They have experience with a wide range of inductor types and can tell you about the latest developments in low profile, surface mounting, etc.

Maximum Output Load Current

Maximum load current for a buck converter is limited by the maximum switch current rating (I_P). The current rating for the LT3430/LT3430-1 is 3A. Unlike most current mode converters, the LT3430/LT3430-1 maximum switch current limit does not fall off at high duty cycles. Most current mode converters suffer a drop off of peak switch current for duty cycles above 50%. This is due to the effects of slope compensation required to prevent subharmonic oscillations in current mode converters. (For detailed analysis, see Application Note 19.)

The LT3430/LT3430-1 are able to maintain peak switch current limit over the full duty cycle range by using patented circuitry* to cancel the effects of slope compensation on peak switch current without affecting the frequency compensation it provides.

Maximum load current would be equal to maximum switch current *for an infinitely large inductor*, but with finite inductor size, maximum load current is reduced by one-half peak-to-peak inductor current (I_{LP-P}). The following formula assumes continuous mode operation, implying that the term on the right is less than one-half of IP.

$I_{OUT(MAX)}$ =

Continuous Mode

$$I_P - \frac{I_{LP-P}}{2} = I_P - \frac{(V_{OUT} + V_F)(V_{IN} - V_{OUT} - V_F)}{2(L)(f)(V_{IN})}$$

For V_{OUT} = 5V, V_{IN} = 12V, $V_{F(D1)}$ = 0.52V, f = 200kHz and L = 15µH:

$$I_{OUT(MAX)} = 3 - \frac{(5 + 0.52)(12 - 5 - 0.52)}{2(15 \bullet 10^{-6})(200 \bullet 10^{3})(12)}$$
$$= 3 - 0.5 = 2.5A$$

Note that there is less load current available at the higher input voltage because inductor ripple current increases. At V_{IN} = 24V, duty cycle is 23% and for the same set of conditions:

$$I_{OUT(MAX)} = 3 - \frac{(5 + 0.52)(24 - 5 - 0.52)}{2(15 \bullet 10^{-6})(200 \bullet 10^{3})(24)}$$
$$= 3 - 0.71 = 2.29A$$

To calculate actual peak switch current with a given set of conditions, use:

$$I_{SW(PEAK)} = I_{OUT} + \frac{I_{LP-P}}{2}$$
$$= I_{OUT} + \frac{(V_{OUT} + V_F)(V_{IN} - V_{OUT} - V_F)}{2(L)(f)(V_{IN})}$$

*US Patent # 6,498,466

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Reduced Inductor Value and Discontinuous Mode

If the smallest inductor value is of most importance to a converter design, in order to reduce inductor size/cost, discontinuous mode may yield the smallest inductor solution. The maximum output load current in discontinuous mode, however, must be calculated and is defined later in this section.

Discontinuous mode is entered when the output load current is less than one-half of the inductor ripple current (I_{LP-P}). In this mode, inductor current falls to zero before the next switch turn on (see Figure 8). Buck converters will be in discontinuous mode for output load current given by:

$$I_{OUT\ Discontinuous\ Mode} < \frac{(V_{OUT}+V_F)(V_{IN}-V_{OUT}-V_F)}{(2)(V_{IN})(f)(L)}$$

The inductor value in a buck converter is usually chosen large enough to keep inductor ripple current (I_{LP-P}) low; this is done to minimize output ripple voltage and maximize output load current. In the case of large inductor values, as seen in the equation above, discontinuous mode will be associated with "light loads."

When choosing small inductor values, however, discontinuous mode will occur at much higher output load currents. The limit to the smallest inductor value that can be chosen is set by the LT3430/LT3430-1 peak switch current (I_P) and the maximum output load current required, given by:

$$I_{OUT(MAX)\ Discontinuous\ Mode} = < \frac{I_{LP-P}}{2}$$

$$= \frac{I_P{}^2}{(2)(I_{LP-P})}$$

$$= \frac{I_P{}^2(f \bullet L \bullet V_{IN})}{2(V_{OUT}+V_F)(V_{IN}-V_{OUT}-V_F)}$$

Example: For V_{IN} = 15V, V_{OUT} = 5V, V_F = 0.52V, f = 200kHz and L = 4.7µH.

$$I_{OUT(MAX)\ Discontinuous\ Mode} = \frac{3^2 \bullet (200 \bullet 10^3)(4.7 \bullet 10^{-6})(15)}{2(5+0.52)(15-5-0.52)}$$

$$I_{OUT(MAX)\ Discontinuous\ Mode} = 1.21A$$

What has been shown here is that if high inductor ripple current and discontinuous mode operation can be tolerated, small inductor values can be used. If a higher output load current is required, the inductor value must be increased. If $I_{OUT(MAX)}$ no longer meets the discontinuous mode criteria, use the $I_{OUT(MAX)}$ equation for continuous mode; the LT3430/LT3430-1 are designed to operate well in both modes of operation, allowing a large range of inductor values to be used.

Short-Circuit Considerations

The LT3430/LT3430-1 are current mode controllers. They use the V_C node voltage as an input to a current comparator which turns off the output switch on a cycle-by-cycle basis as this peak current is reached. The internal clamp on the V_C node, nominally 2V, then acts as an output switch peak current limit. This action becomes the switch current limit specification. The maximum available output power is then determined by the switch current limit.

A potential controllability problem could occur under short-circuit conditions. If the power supply output is short circuited, the feedback amplifier responds to the low output voltage by raising the control voltage, V_C, to its peak current limit value. Ideally, the output switch would be turned on, and then turned off as its current exceeded the value indicated by V_C. However, there is finite response time involved in both the current comparator and turnoff of the output switch. These result in a minimum on time $t_{ON(MIN)}$. When combined with the large ratio of V_{IN} to $(V_F + I \bullet R)$, the diode forward voltage plus inductor I • R voltage drop, the potential exists for a loss of control. Expressed mathematically the requirement to maintain control is:

$$f \bullet t_{ON} \leq \frac{V_F + I \bullet R}{V_{IN}}$$

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where:
f = switching frequency
t_{ON} = switch minimum on time
V_F = diode forward voltage
V_{IN} = Input voltage
I • R = inductor I • R voltage drop

If this condition is not observed, the current will not be limited at I_{PK}, but will cycle-by-cycle ratchet up to some higher value. Using the nominal LT3430/LT3430-1 clock frequencies of 200KHz/100kHz, a V_{IN} of 40V and a (V_F + I • R) of say 0.7V, the maximum t_{ON} to maintain control would be approximately 90ns for the LT3430 and 180ns for the LT3430-1, unacceptably short times.

The solution to this dilemma is to slow down the oscillator when the FB pin voltage is abnormally low thereby indicating some sort of short-circuit condition. Oscillator frequency is unaffected until FB voltage drops to about 2/3 of its normal value. Below this point the oscillator frequency decreases roughly linearly down to a limit of about 40kHz. (30kHz for LT3430-1) This lower oscillator frequency during short-circuit conditions can then maintain control with the effective minimum on time.

It is recommended that for [V_{IN}/(V_{OUT} + V_F)] ratios > 10, a soft-start circuit should be used for the LT3430 to control the output capacitor charge rate during start-up or during recovery from an output short circuit, thereby adding additional control over peak inductor current. See Buck Converter with Adjustable Soft-Start later in this data sheet.

OUTPUT CAPACITOR

The output capacitor is normally chosen by its effective series resistance (ESR), because this is what determines output ripple voltage. To get low ESR takes *volume*, so physically smaller capacitors have high ESR. The ESR range for typical LT3430 applications is 0.05Ω to 0.2Ω. A typical output capacitor is an AVX type TPS, 100µF at 10V, with a guaranteed ESR less than 0.1Ω (The LT3430-1 will typically use two of these capacitors in parallel). This is a "D" size surface mount solid tantalum capacitor. TPS capacitors are specially constructed and tested for low ESR, so they give the lowest ESR for a given volume. The value in microfarads is not particularly critical, and values from 22µF to greater than 500µF work well, but you cannot cheat mother nature on ESR. If you find a tiny 22µF solid tantalum capacitor, it will have high ESR, and output ripple voltage will be terrible. Table 3 shows some typical solid tantalum surface mount capacitors.

Table 3. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current

E Case Size	ESR (Max., Ω)	Ripple Current (A)
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
D Case Size		
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
C Case Size		
AVX TPS	0.2 (typ)	0.5 (typ)

Many engineers have heard that solid tantalum capacitors are prone to failure if they undergo high surge currents. This is historically true, and type TPS capacitors are specially tested for surge capability, but surge ruggedness is not a critical issue with the *output* capacitor. Solid tantalum capacitors fail during very high *turn-on* surges, which do not occur at the output of regulators. High *discharge* surges, such as when the regulator output is dead shorted, do not harm the capacitors.

Unlike the input capacitor, RMS ripple current in the output capacitor is normally low enough that ripple current rating is not an issue. The current waveform is triangular with a typical value of 250mA_{RMS}. The formula to calculate this is:

Output capacitor ripple current (RMS):

$$I_{RIPPLE(RMS)} = \frac{0.29(V_{OUT})(V_{IN} - V_{OUT})}{(L)(f)(V_{IN})}$$

Ceramic Capacitors

Higher value, lower cost ceramic capacitors are now becoming available. They are generally chosen for their good high frequency operation, small size and very low ESR (effective series resistance). Their low ESR reduces output ripple voltage but also removes a useful zero in the loop frequency response, common to tantalum capacitors. To compensate for this, a resistor R_C can be placed in series with the V_C compensation capacitor C_C. Care must be taken however, since this resistor sets the high

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frequency gain of the error amplifier, including the gain at the switching frequency. If the gain of the error amplifier is high enough at the switching frequency, output ripple voltage (although smaller for a ceramic output capacitor) may still affect the proper operation of the regulator. A filter capacitor C_F in parallel with the R_C/C_C network is suggested to control possible ripple at the V_C pin. An "All Ceramic" solution is possible for the LT3430/LT3430-1 by choosing the correct compensation components for the given application.

Example: For V_{IN} = 8V to 40V, V_{OUT} = 5V at 2A, the LT3430 can be stabilized, provide good transient response and maintain very low output ripple voltage using the following component values: (refer to the first page of this data sheet for component references) C_{IN} = 4.7µF, R_C = 3.3k, C_C = 22nF, C_F = 220pF and C_{OUT} = 100µF. See Application Note 19 for further detail on techniques for proper loop compensation.

INPUT CAPACITOR

Step-down regulators draw current from the input supply in pulses. The rise and fall times of these pulses are very fast. The input capacitor is required to reduce the voltage ripple this causes at the input of LT3430/LT3430-1 and force the switching current into a tight local loop, thereby minimizing EMI. The RMS ripple current can be calculated from:

$$I_{RIPPLE(RMS)} = I_{OUT}\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)/V_{IN}^2}$$

Ceramic capacitors are ideal for input bypassing. At 200kHz (100kHz) switching frequency, the energy storage requirement of the input capacitor suggests that values in the range of 4.7µF to 20µF (10µF to 47µF) are suitable for most applications. If operation is required close to the minimum input required by the output of the LT3430, a larger value may be required. This is to prevent excessive ripple causing dips below the minimum operating voltage resulting in erratic operation.

Depending on how the LT3430/LT3430-1 circuit is powered up you may need to check for input voltage transients. The input voltage transients may be caused by input voltage steps or by connecting the LT3430/LT3430-1 converter to an already powered up source such as a wall adapter. The sudden application of input voltage will cause a large surge of current in the input leads that will store energy in the parasitic inductance of the leads. This energy will cause the input voltage to swing above the DC level of input power source and it may exceed the maximum voltage rating of input capacitor and LT3430/LT3430-1.

The easiest way to suppress input voltage transients is to add a small aluminum electrolytic capacitor in parallel with the low ESR input capacitor. The selected capacitor needs to have the right amount of ESR in order to critically dampen the resonant circuit formed by the input lead inductance and the input capacitor. The typical values of ESR will fall in the range of 0.5Ω to 2Ω and capacitance will fall in the range of 5µF to 50µF.

If tantalum capacitors are used, values in the 22µF to 470µF range are generally needed to minimize ESR and meet ripple current and surge ratings. Care should be taken to ensure the ripple and surge ratings are not exceeded. The AVX TPS and Kemet T495 series are surge rated. AVX recommends derating capacitor operating voltage by 2:1 for high surge applications.

CATCH DIODE

Highest efficiency operation requires the use of a Schottky type diode. DC switching losses are minimized due to its low forward voltage drop, and AC behavior is benign due to its lack of a significant reverse recovery time.

The use of so-called "ultrafast" recovery diodes is generally not recommended. When operating in continuous mode, the reverse recovery time exhibited by "ultrafast" diodes will result in a slingshot type effect. The power internal switch will ramp up V_{IN} current into the diode in an attempt to get it to recover. Then, when the diode has finally turned off, some tens of nanoseconds later, the V_{SW} node voltage ramps up at an extremely high dV/dt, perhaps 5 to even 10V/ns ! With real world lead inductances, the V_{SW} node can easily overshoot the V_{IN} rail. This can result in

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poor RFI behavior and if the overshoot is severe enough, damage the IC itself.

The suggested catch diode (D1) is an International Rectifier 30BQ060 Schottky. It is rated at 3A average forward current and 60V reverse voltage. Typical forward voltage is 0.52V at 3A. The diode conducts current only during switch off time. Peak reverse voltage is equal to regulator input voltage. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = \frac{I_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}$$

This formula will not yield values higher than 3A with maximum load current of 3A.

BOOST PIN

For most LT 3430 applications, the boost components are a 0.68µF capacitor and a MMSD914TI diode. The anode is typically connected to the regulated output voltage to generate a voltage approximately V_{OUT} above V_{IN} to drive the output stage. However, the output stage discharges the boost capacitor during the on time of the switch. The output driver requires at least 3V of headroom throughout this period to keep the switch fully saturated. If the output voltage is less than 3.3V, it is recommended that an alternate boost supply is used. For output voltages greater than 6V, it is recommended to place a zener diode (D4; page 20) in series with the Boost diode to set Boost-to-SW voltage between 4V to 6V. This minimizes power loss within the IC, improving maximum ambient temperature operation. In addition, D4 minimizes Boost current overshoot during power switch turn on to reduce noise within the regulator loop. For output voltages greater than the standard demoboard 5V output, a location for D4 is provided.

A 0.68µF boost capacitor is recommended for most LT3430 applications. Almost any type of film or ceramic capacitor is suitable, but the ESR should be <1Ω to ensure it can be fully recharged during the off time of the switch. The LT3430 capacitor value is derived from conditions of 4800ns on time, 75mA boost current and 0.7V discharge ripple. The boost capacitor value could be reduced under less demanding conditions, but this will not improve circuit operation or efficiency. Under low input voltage and low load conditions, a higher value capacitor will reduce discharge ripple and improve start-up operation. For the LT3430-1 a 1.5µF boost capacitor is recommended.

SHUTDOWN FUNCTION AND UNDERVOLTAGE LOCKOUT

Figure 4 shows how to add undervoltage lockout (UVLO) to the LT3430/LT3430-1. Typically, UVLO is used in situations where the input supply is *current limited*, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur.

Threshold voltage for lockout is about 2.38V. A 5.5µA bias current flows *out* of the pin at this threshold. The internally generated current is used to force a default high state on the shutdown pin if the pin is left open. When low shutdown current is not an issue, the error due to this current can be minimized by making R_{LO} 10k or less. If shutdown current is an issue, R_{LO} can be raised to 100k, but the error due to initial bias current and changes with temperature should be considered.

$$R_{LO} = 10k \text{ to } 100k \ (25k \text{ suggested})$$

$$R_{HI} = \frac{R_{LO}(V_{IN} - 2.38V)}{2.38V - R_{LO}(5.5\mu A)}$$

V_{IN} = Minimum input voltage

Keep the connections from the resistors to the shutdown pin short and make sure that interplane or surface capacitance to the switching nodes are minimized. If high resistor values are used, the shutdown pin should be bypassed with a 1000pF capacitor to prevent coupling problems from the switch node. If hysteresis is desired in the undervoltage lockout point, a resistor R_{FB} can be added to the output node. Resistor values can be calculated from:

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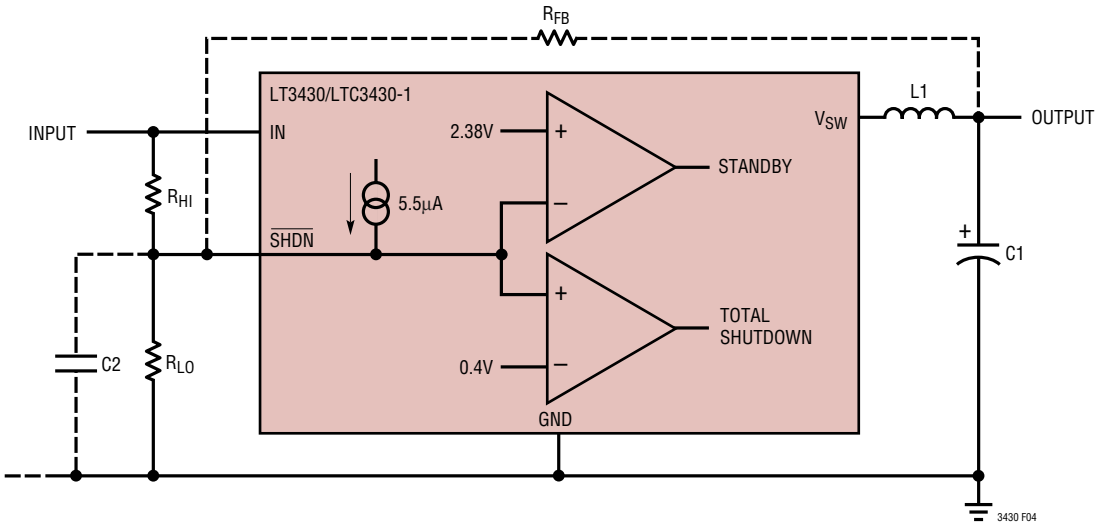

Figure 4. Undervoltage Lockout

$$R_{HI} = \frac{R_{LO}\left[V_{IN} - 2.38\left(\Delta V/V_{OUT} + 1\right) + \Delta V\right]}{2.38 - R_{LO}\left(5.5\mu A\right)}$$

$$R_{FB} = \left(R_{HI}\right)\left(V_{OUT}/\Delta V\right)$$

25k suggested for R_{LO}

V_{IN} = Input voltage at which switching stops as input voltage descends to trip level

ΔV = Hysteresis in input voltage level

Example: output voltage is 5V, switching is to stop if input voltage drops below 12V and should not restart unless input rises back to 13.5V. ΔV is therefore 1.5V and V_{IN} = 12V. Let R_{LO} = 25k.

$$R_{HI} = \frac{25k\left[12 - 2.38\left(1.5/5 + 1\right) + 1.5\right]}{2.38 - 25k\left(5.5\mu A\right)}$$

$$= \frac{25k\left(10.41\right)}{2.24} = 116k$$

$$R_{FB} = 116k\left(5/1.5\right) = 387k$$

SYNCHRONIZING

The SYNC input must pass from a logic level low, through the maximum synchronization threshold with a duty cycle between 10% and 90%. The input can be driven directly from a logic level output. The LT3430 synchronizing range is equal to *initial* operating frequency up to 700kHz. This means that *minimum* practical sync frequency is equal to the worst-case *high* self-oscillating frequency (228kHz), not the typical operating frequency of 200kHz. Caution should be used when synchronizing above 265kHz because at higher sync frequencies the amplitude of the internal slope compensation used to prevent subharmonic switching is reduced. This type of subharmonic switching only occurs at input voltages less than twice output voltage. Higher inductor values will tend to eliminate this problem. See Frequency Compensation section for a discussion of an entirely different cause of subharmonic switching before assuming that the cause is insufficient slope compensation. Application Note 19 has more details on the theory of slope compensation. The LT3430-1 synchronizing range is from 125kHz to 250kHz (slope compensation loss occurs above 133kHz).

At power-up, when V_C is being clamped by the FB pin (see Figure 2, Q2), the sync function is disabled. This allows the frequency foldback to operate in the shorted output condition. During normal operation, switching frequency is controlled by the internal oscillator until the FB pin reaches 0.6V, after which the SYNC pin becomes operational. If no synchronization is required, this pin should be connected to ground.

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LAYOUT CONSIDERATIONS

As with all high frequency switchers, when considering layout, care must be taken in order to achieve optimal electrical, thermal and noise performance. For maximum efficiency, switch rise and fall times are typically in the nanosecond range. To prevent noise both radiated and conducted, the high speed switching current path, shown in Figure 5, must be kept as short as possible. This is implemented in the suggested layout of Figure 6. Shortening this path will also reduce the parasitic trace inductance of approximately 25nH/inch. At switch off, this parasitic inductance produces a flyback spike across the LT3430/LT3430-1 switch. When operating at higher currents and input voltages, with poor layout, this spike can generate voltages across the LT3430/LT3430-1 that may exceed its absolute maximum rating. A ground plane should always be used under the switcher circuitry to prevent interplane coupling and overall noise.

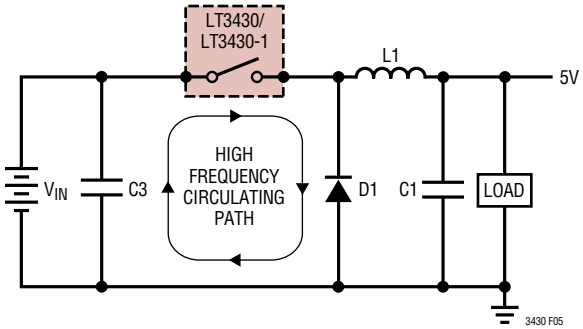

Figure 5. High Speed Switching Path

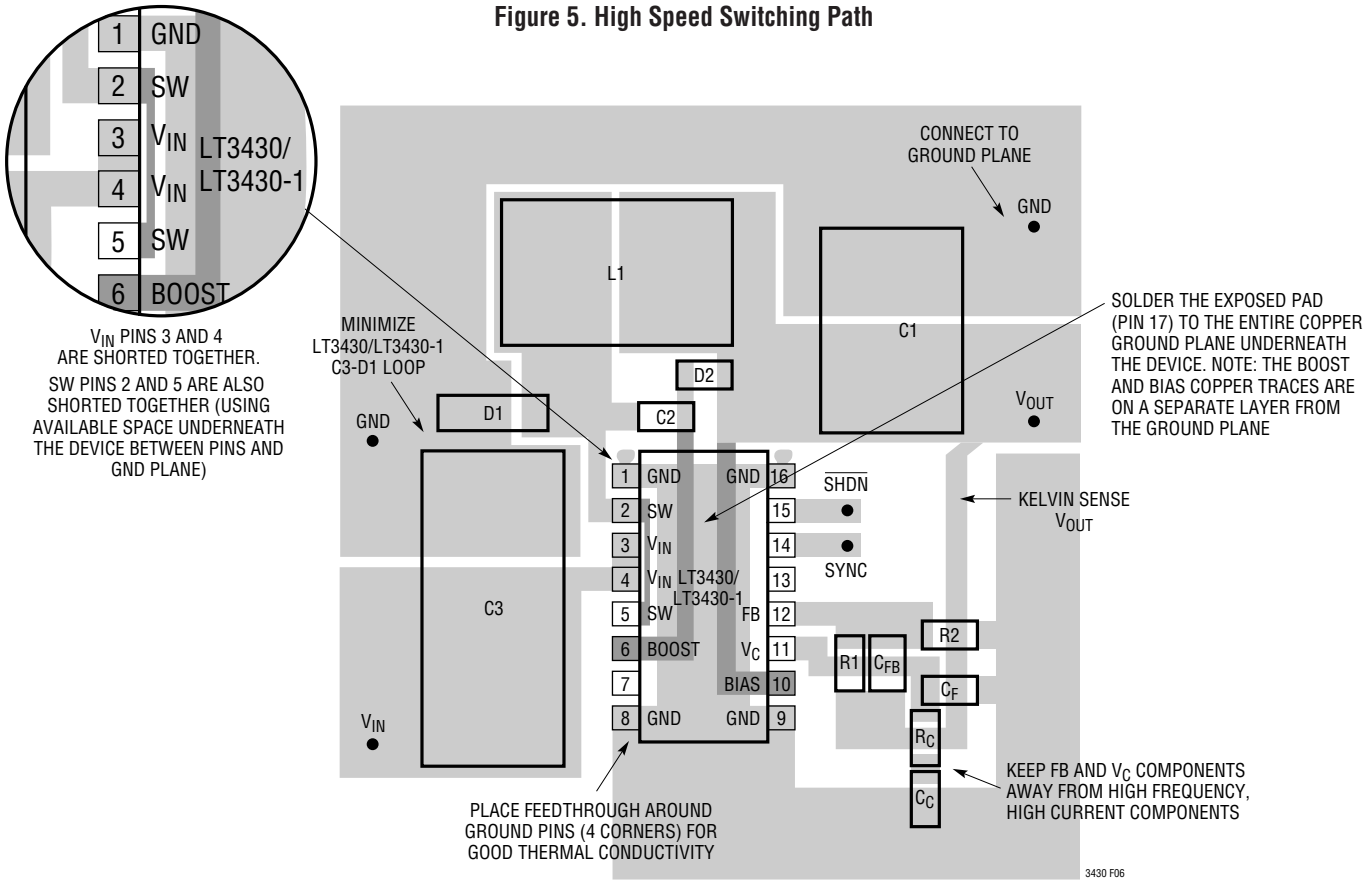

Figure 6. Suggested Layout

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The V_C and FB components should be kept as far away as possible from the switch and boost nodes. The LT3430/LT3430-1 pinout has been designed to aid in this. The ground for these components should be separated from the switch current path. Failure to do so will result in poor stability or subharmonic like oscillation.

Board layout also has a significant effect on thermal resistance. Pins 1, 8, 9 and 16, GND, should be soldered to a continuous copper ground plane under the LT3430/LT3430-1 die. The FE package has an exposed pad (Pin 17) which is the best thermal path for heat out of the package. Soldering the exposed pad to the copper ground plane under the device will reduce die temperature and increase the power capability of the LT3430/LT3430-1. Adding multiple solder filled feedthroughs under and around the four corner pins to the ground plane will also help. Similar treatment to the catch diode and coil terminations will reduce any additional heating effects.

PARASITIC RESONANCE

Resonance or "ringing" may sometimes be seen on the switch node (see Figure 7). Very high frequency ringing following switch rise time is caused by switch/diode/input capacitor lead inductance and diode capacitance. Schottky diodes have very high "Q" junction capacitance that can ring for many cycles when excited at high frequency. If total lead length for the input capacitor, diode and switch path is 1 inch, the inductance will be approximately 25nH. At switch off, this will produce a spike across the NPN output device in addition to the input voltage. At higher currents this spike can be in the order of 10V to 20V or higher with a poor layout, potentially exceeding the absolute max switch voltage. The path around switch, catch diode and input capacitor must be kept as short as possible to ensure reliable operation. When looking at this, a >100MHz oscilloscope must be used, and waveforms should be observed on the leads of the package. This switch off spike will also cause the SW node to go below ground. The LT3430/LT3430-1 have special circuitry inside which mitigates this problem, but negative voltages over 0.8V lasting longer than 10ns should be avoided. Note that 100MHz oscilloscopes are barely fast enough to see the details of the falling edge overshoot in Figure 7.

A second, much lower frequency ringing is seen during switch off time if load current is low enough to allow the inductor current to fall to zero during part of the switch off time (see Figure 8). Switch and diode capacitance resonate with the inductor to form damped ringing at 1MHz to 10MHz. This ringing is not harmful to the regulator and it has not been shown to contribute significantly to EMI. Any attempt to damp it with a resistive snubber will degrade efficiency.

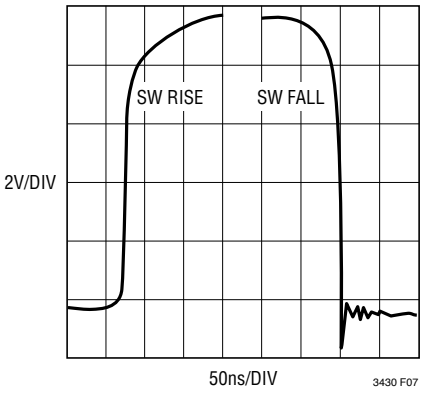

Figure 7. Switch Node Resonance

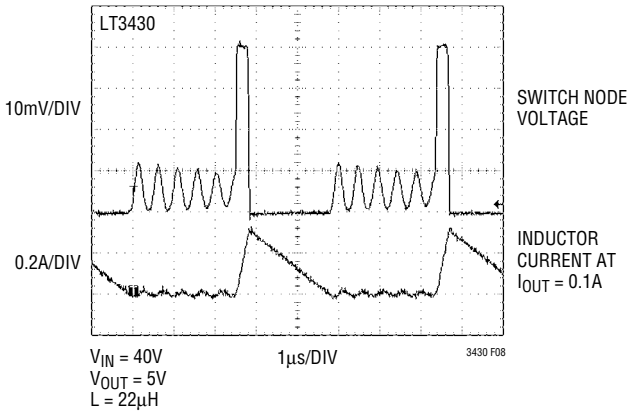

Figure 8. Discontinuous Mode Ringing

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THERMAL CALCULATIONS

Power dissipation in the LT3430/LT3430-1 chip comes from four sources: switch DC loss, switch AC loss, boost circuit current, and input quiescent current. The following formulas show how to calculate each of these losses. These formulas assume continuous mode operation, so they should not be used for calculating efficiency at light load currents.

Switch loss:

$$P_{SW} = \frac{R_{SW}(I_{OUT})^2(V_{OUT})}{V_{IN}} + t_{EFF}(1/2)(I_{OUT})(V_{IN})(f)$$

(Note: Switching losses are less for the LT3430-1 operating at only 100kHz)

Boost current loss:

$$P_{BOOST} = \frac{V_{OUT}{}^2(I_{OUT}/36)}{V_{IN}}$$

Quiescent current loss:

$$P_Q = V_{IN}(0.0015) + V_{OUT}(0.003)$$

R_{SW} = Switch resistance (≈0.15) hot
t_{EFF} = Effective switch current/voltage overlap time
$= (t_r + t_f + t_{lr} + t_{lf})$
$t_r = (V_{IN}/1.2)$ns
$t_f = (V_{IN}/1.1)$ns
$t_{lr} = t_{lf} = (I_{OUT}/0.2)$ns
f = Switch frequency

Example: with V_{IN} = 40V, V_{OUT} = 5V and I_{OUT} = 2A:

$$P_{SW} = \frac{(0.15)(2)^2(5)}{40} + \left(90 \bullet 10^{-9}\right)(1/2)(2)(40)\left(200 \bullet 10^3\right)$$
$$= 0.08 + 0.72 = 0.8W$$

$$P_{BOOST} = \frac{(5)^2(2/36)}{40} = 0.04W$$

$$P_Q = 40(0.0015) + 5(0.003) = 0.08W$$

Total power dissipation in the IC is given by:

$$P_{TOT} = P_{SW} + P_{BOOST} + P_Q$$
$$= 0.8W + 0.04W + 0.08W = 0.92W$$

Thermal resistance for the LT3430/LT3430-1 package is influenced by the presence of internal or backside planes.

TSSOP (Exposed Pad) Package: With a full plane under the TSSOP package, thermal resistance will be about 45°C/W.

To calculate die temperature, use the proper thermal resistance number for the desired package and add in worst-case ambient temperature:

$$T_J = T_A + (\theta_{JA} \bullet P_{TOT})$$

When estimating ambient, remember the nearby catch diode and inductor will also be dissipating power:

$$P_{DIODE} = \frac{(V_F)(V_{IN} - V_{OUT})(I_{LOAD})}{V_{IN}}$$

V_F = Forward voltage of diode (assume 0.52V at 2A)

$$P_{DIODE} = \frac{(0.52)(40-5)(2)}{40} = 0.91W$$

$P_{INDUCTOR} = (I_{LOAD})^2(R_{IND})$

R_{IND} = Inductor DC resistance (assume 0.1Ω)

$P_{INDUCTOR}\ (2)^2(0.1) = 0.4W$

Only a portion of the temperature rise in the external inductor and diode is coupled to the junction of the LT3430. Based on empirical measurements, the thermal effect on the LT3430 junction temperature due to power dissipation in the external inductor and catch diode can be calculated as:

$$\Delta T_J(LT3430) \approx (P_{DIODE} + P_{INDUCTOR})(5°C/W)$$

Using the example calculations for LT3430 dissipation, the LT3430 die temperature will be estimated as:

$$T_J = T_A + (\theta_{JA} \bullet P_{TOT}) + [5 \bullet (P_{DIODE} + P_{INDUCTOR})]$$

With the TSSOP package (θ_{JA} = 45°C/W), at an ambient temperature of 50°C:

$$T_J = 50 + (45 \bullet 0.92) + (5 \bullet 1.31) = 98°C$$

Die temperature can peak for certain combinations of V_{IN}, V_{OUT} and load current. While higher V_{IN} gives greater switch AC losses, quiescent and catch diode losses, a

APPLICATIONS INFORMATION

lower V_{IN} may generate greater losses due to switch DC losses. In general, the maximum and minimum V_{IN} levels should be checked with maximum typical load current for calculation of the LT3430/LT3430-1 die temperature. If a more accurate die temperature is required, a measurement of the SYNC pin resistance (to GND) can be used. The SYNC pin resistance can be measured by forcing a voltage no greater than 0.5V at the pin and monitoring the pin current over temperature in an oven. This should be done with minimal device power (low V_{IN} and no switching (V_C = 0V)) in order to calibrate SYNC pin resistance with ambient (oven) temperature.

Note: Some of the internal power dissipation in the IC, due to BOOST pin voltage, can be transferred outside of the IC to reduce junction temperature, by increasing the voltage drop in the path of the boost diode D2 (see Figure 9). This reduction of junction temperature inside the IC will allow higher ambient temperature operation for a given set of conditions. BOOST pin circuitry dissipates power given by:

$$P_{DISS}\ BOOST\ Pin = \frac{V_{OUT} \bullet (I_{SW}/36) \bullet V_{C2}}{V_{IN}}$$

Typically V_{C2} (the boost voltage across the capacitor C2) equals V_{OUT}. This is because diodes D1 and D2 can be considered almost equal, where:

$$V_{C2} = V_{OUT} - V_{FD2} - (-V_{FD1}) = V_{OUT}$$

Hence the equation used for boost circuitry power dissipation given in the previous Thermal Calculations section is stated as:

$$P_{DISS(BOOST)} = \frac{V_{OUT} \bullet (I_{SW}/36)}{V_{IN}} \bullet V_{OUT}$$

Here it can be seen that boost power dissipation increases as the square of V_{OUT}. It is possible, however, to reduce V_{C2} below V_{OUT} to save power dissipation by increasing the voltage drop in the path of D2. Care should be taken that V_{C2} does not fall below the minimum 3.3V boost voltage required for full saturation of the internal power switch. For output voltages of 5V, V_{C2} is approximately 5V. During switch turn on, V_{C2} will fall as the boost capacitor C2 is dicharged by the BOOST pin. In the previous BOOST Pin section, the value of C2 was designed for a 0.7V droop in $V_{C2} = V_{DROOP}$. Hence, an output voltage as low as 4V would still allow the minimum 3.3V for the boost function using the C2 capacitor calculated. If a target output voltage of 12V is required, however, an excess of 8V is placed across the boost capacitor which is not required for the boost function but still dissipates additional power.

What is required is a voltage drop in the path of D2 to achieve minimal power dissipation while still maintaining minimum boost voltage across C2. A zener, D4, placed in series with D2 (see Figure 9), drops voltage to C2.

Example : the BOOST pin power dissipation for a 20V input to 12V output conversion at 2A is given by:

$$P_{BOOST} = \frac{12 \bullet (2/36) \bullet 12}{20} = 0.4W$$

If a 7V zener D4 is placed in series with D2, then power dissipation becomes :

$$P_{BOOST} = \frac{12 \bullet (2/36) \bullet 5}{20} = 0.167W$$

For an FE package with thermal resistance of 45°C/W, ambient temperature savings would be, T(ambient) sav-

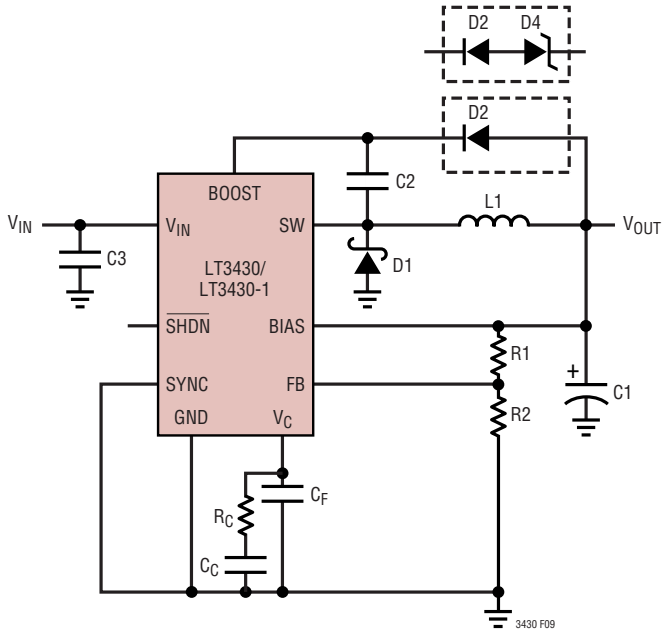

Figure 9. BOOST Pin, Diode Selection

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ings = 0.233W • 45°C/W = 11°C. The 7V zener should be sized for excess of 0.233W operaton. The tolerances of the zener should be considered to ensure minimum V_{C2} exceeds 3.3V + V_{DROOP}.

Input Voltage vs Operating Frequency Considerations

The absolute maximum input supply voltage for the LT3430/LT3430-1 is specified at 60V. This is based solely on internal semiconductor junction breakdown effects. Due to internal power dissipation, the actual maximum V_{IN} achievable in a particular application may be less than this.

A detailed theoretical basis for estimating internal power loss is given in the section, Thermal Considerations. Note that AC switching loss is proportional to both operating frequency and output current. The majority of AC switching loss is also proportional to the *square* of input voltage. For example, while the combination of V_{IN} = 40V, V_{OUT} = 5V at 2A and f_{OSC} = 200kHz may be easily achievable, simultaneously raising V_{IN} to 60V and f_{OSC} to 700kHz is not possible. Nevertheless, input voltage *transients* up to 60V can usually be accommodated, assuming the resulting increase in internal dissipation is of insufficient time duration to raise die temperature significantly.

A second consideration is controllability. A potential limitation occurs with a high step-down ratio of V_{IN} to V_{OUT}, as this requires a correspondingly narrow minimum switch on time. An approximate expression for this (assuming continuous mode operation) is given as follows:

$$\min t_{ON} = \frac{V_{OUT} + V_F}{V_{IN}\left(f_{OSC}\right)}$$

where:

V_{IN} = input voltage
V_{OUT} = output voltage
V_F = Schottky diode forward drop
f_{OSC} = switching frequency

A potential controllability problem arises if the LT3430/LT3430-1 are called upon to produce an on time shorter than it is able to produce. Feedback loop action will lower then reduce the V_C control voltage to the point where some sort of cycle-skipping or odd/even cycle behavior is exhibited.

In summary:

1. Be aware that the simultaneous requirements of high V_{IN}, high I_{OUT} and high f_{OSC} may not be achievable in practice due to internal dissipation. The Thermal Considerations section offers a basis to estimate internal power. In questionable cases a prototype supply should be built and exercised to verify acceptable operation.
2. The simultaneous requirements of high V_{IN}, low V_{OUT} and high f_{OSC} can result in an unacceptably short minimum switch on time. Cycle skipping and/or odd/even cycle behavior will result although correct output voltage is usually maintained. The LT3430-1 100kHz switching frequency will allow higher V_{IN}/V_{OUT} ratios without pulse skipping.

FREQUENCY COMPENSATION

Before starting on the theoretical analysis of frequency response, the following should be remembered—the worse the board layout, the more difficult the circuit will be to stabilize. This is true of almost all high frequency analog circuits, read the Layout Considerations section first. Common layout errors that appear as stability problems are distant placement of input decoupling capacitor and/or catch diode, and connecting the V_C compensation to a ground track carrying significant switch current. In addition, the theoretical analysis considers only first order non-ideal component behavior. For these reasons, it is important that a final stability check is made with production layout and components.

The LT3430/LT3430-1 use current mode control. This alleviates many of the phase shift problems associated with the inductor. The basic regulator loop is shown in Figure 10. The LT3430/LT3430-1 can be considered as two g_m blocks, the error amplifier and the power stage.

Figure 11 shows the overall loop response. At the V_C pin, the frequency compensation components used are: R_C = 3.3k, C_C = 0.022µF and C_F = 220pF. The output capacitor used is a 100µF, 10V tantalum capacitor with typical ESR of 100mΩ. LT3430-1 uses two of these capacitors in parallel.

The ESR of the tantalum output capacitor provides a useful zero in the loop frequency response for maintaining

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stability. This ESR, however, contributes significantly to the ripple voltage at the output (see Output Ripple Voltage in the Applications Information section). It is possible to reduce capacitor size and output ripple voltage by replacing the tantalum output capacitor with a ceramic output capacitor because of its very low ESR. The zero provided by the tantalum output capacitor must now be reinserted back into the loop. Alternatively, there may be cases where, even with the tantalum output capacitor, an additional zero is required in the loop to increase phase margin for improved transient response.

A zero can be added into the loop by placing a resistor (R_C) at the V_C pin in series with the compensation capacitor, C_C, or by placing a capacitor (C_{FB}) between the output and the FB pin.

When using R_C, the maximum value has two limitations. First, the combination of output capacitor ESR and R_C may stop the loop rolling off altogether. Second, if the loop gain is not rolled off sufficiently at the switching frequency, output ripple will perturb the V_C pin enough to cause unstable duty cycle switching similar to subharmonic oscillations. If needed, an additional capacitor (C_F) can be added across the R_C/C_C network from the V_C pin to ground to further suppress V_C ripple voltage.

With a tantalum output capacitor, the LT3430/LT3430-1 already includes a resistor (R_C) and filter capacitor (C_F) at the V_C pin (see Figures 10 and 11) to compensate the loop over the entire V_{IN} range (to allow for stable pulse skipping for high V_{IN}-to-V_{OUT} ratios ≥ 10). A ceramic output capacitor can still be used with a simple adjustment to the resistor R_C for stable operation (see Ceramic Capacitors section for stabilizing LT3430). If additional phase margin is required, a capacitor (C_{FB}) can be inserted between the output and FB pin but care must be taken for high output voltage applications. Sudden shorts to the output can create unacceptably large negative transients on the FB pin.

For V_{IN}-to-V_{OUT} ratios < 10, higher loop bandwidths are possible by readjusting the frequency compensation components at the V_C pin.

When checking loop stability, the circuit should be operated over the application's full voltage, current and temperature range. Proper loop compensation may be obtained by empirical methods as described in Application Notes 19 and 76.

CONVERTER WITH BACKUP OUTPUT REGULATOR

In systems with a primary and backup supply, for example, a battery powered device with a wall adapter input, the output of the LT3430/LT3430-1 can be held up by the backup supply with the LT3430/LT3430-1 input disconnected. In this condition, the SW pin will source current into the V_{IN} pin. If the $\overline{SHDN}$ pin is held at ground, only the shut down current of 30µA will be pulled via the SW pin from the second supply. With the $\overline{SHDN}$ pin floating, the

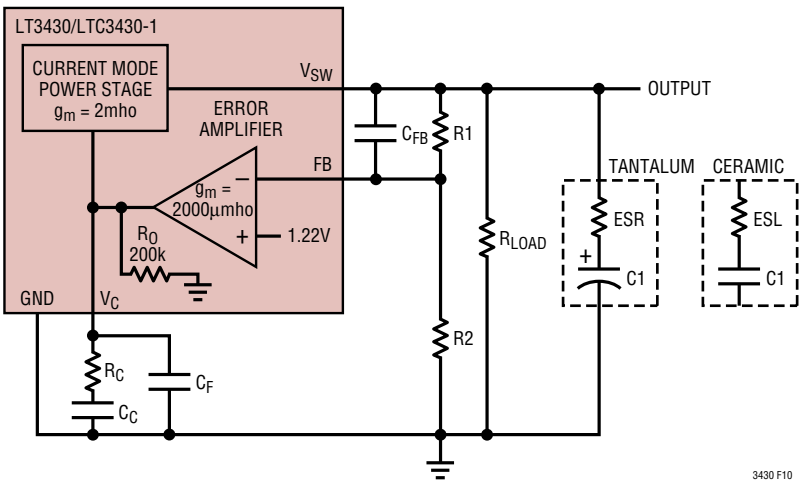

Figure 10. Model for Loop Response

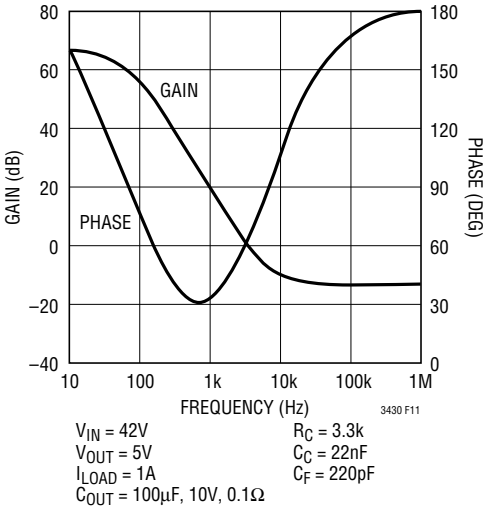

Figure 11. Overall Loop Response

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LT3430/LT3430-1 will consume their quiescent operating current of 1.5mA. The V_{IN} pin will also source current to any other components connected to the input line. If this load is greater than 10mA or the input could be shorted to ground, a series Schottky diode must be added, as shown in Figure 12. With these safeguards, the output can be held at voltages up to the V_{IN} absolute maximum rating.

BUCK CONVERTER WITH ADJUSTABLE SOFT-START

Large capacitive loads or high input voltages can cause high input currents at start-up. Figure 13 shows a circuit that limits the dv/dt of the output at start-up, controlling the capacitor charge rate. The buck converter is a typical configuration with the addition of R3, R4, C_{SS} and Q1. As the output starts to rise, Q1 turns on, regulating switch current via the V_C pin to maintain a constant dv/dt at the output. Output rise time is controlled by the current through C_{SS} defined by R4 and Q1's V_{BE}. Once the output is in regulation, Q1 turns off and the circuit operates normally. R3 is transient protection for the base of Q1.

$$\text{Rise Time} = \frac{(R4)(C_{SS})(V_{OUT})}{V_{BE}}$$

Using the values shown in Figure 10,

$$\text{Rise Time} = \frac{\left(47 \bullet 10^{3}\right)\left(15 \bullet 10^{-9}\right)(5)}{0.7} = 5\text{ms}$$

The ramp is linear and rise times in the order of 100ms are possible. Since the circuit is voltage controlled, the ramp rate is unaffected by load characteristics and maximum output current is unchanged. Variants of this circuit can be used for sequencing multiple regulator outputs.

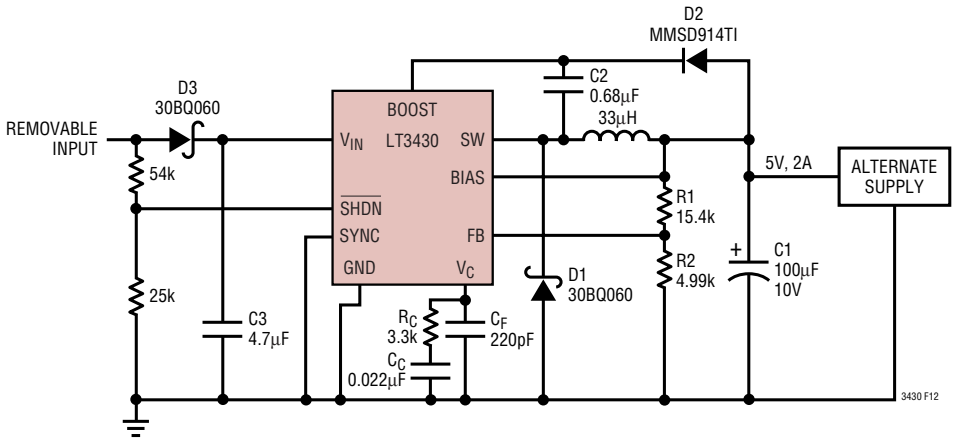

Figure 12. Dual Source Supply with 25µA Reverse Leakage

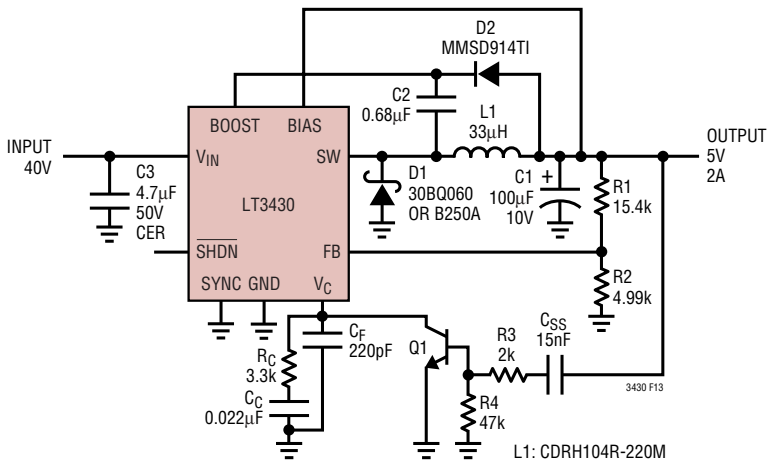

Figure 13. Buck Converter with Adjustable Soft-Start

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DUAL OUTPUT SEPIC CONVERTER

The circuit in Figure 14 generates both positive and negative 5V outputs with a single piece of magnetics. The two inductors shown are actually just two windings on a standard Coiltronics inductor. The topology for the 5V output is a standard buck converter. The –5V topology would be a simple flyback winding coupled to the buck converter if C4 were not present. C4 creates a SEPIC (single-ended primary inductance converter) topology which improves regulation and reduces ripple current in L1. Without C4, the voltage swing on L1B compared to L1A would vary due to relative loading and coupling losses. C4 provides a low impedance path to maintain an equal voltage swing in L1B, improving regulation. In a flyback converter, during switch on time, all the converter's energy is stored in L1A only, since no current flows in L1B. At switch off, energy is transferred by magnetic coupling into L1B, powering the –5V rail. C4 pulls L1B positive during switch on time, causing current to flow, and energy to build in L1B and C4. At switch off, the energy stored in both L1B and C4 supply the –5V rail. This reduces the current in L1A and changes L1B current waveform from square to triangular. For details on this circuit, including maximum output currents, see Design Note 100.

POSITIVE-TO-NEGATIVE CONVERTER

The circuit in Figure 15 is a positive-to-negative topology using a grounded inductor. It differs from the standard approach in the way the IC chip derives its feedback signal because the LT3430/LT3430-1 accepts only positive feedback signals. The ground pin must be tied to the regulated negative output. A resistor divider to the FB pin then provides the proper feedback voltage for the chip.

The following equation can be used to calculate maximum load current for the positive-to-negative converter:

$$I_{MAX} = \frac{\left[I_P - \frac{(V_{IN})(V_{OUT})}{2(V_{OUT}+V_{IN})(f)(L)}\right](V_{OUT})(V_{IN}-0.15)}{(V_{OUT}+V_{IN}-0.15)(V_{OUT}+V_F)}$$

I_P = Maximum rated switch current
V_{IN} = Minimum input voltage
V_{OUT} = Output voltage
V_F = Catch diode forward voltage
0.15 = Switch voltage drop at 3A

Example: with $V_{IN(MIN)}$ = 5.5V, V_{OUT} = 12V, L = 10µH, V_F = 0.52V, I_P = 3A: I_{MAX} = 0.6A.

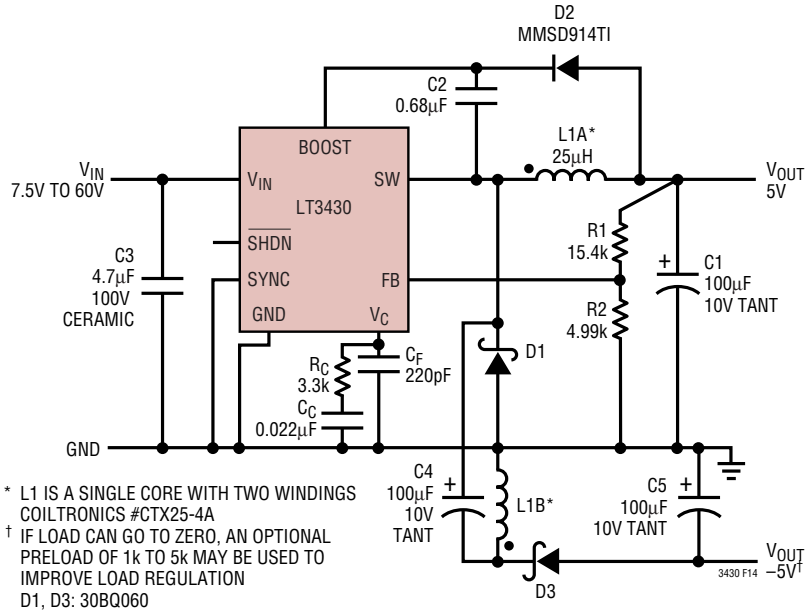

Figure 14. Dual Output SEPIC Converter

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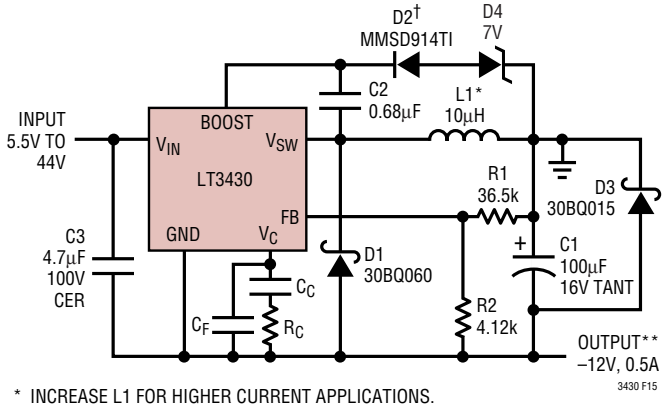

* INCREASE L1 FOR HIGHER CURRENT APPLICATIONS.
SEE APPLICATIONS INFORMATION
** MAXIMUM LOAD CURRENT DEPENDS ON MINIMUM INPUT VOLTAGE
AND INDUCTOR SIZE. SEE APPLICATIONS INFORMATION

Figure 15. Positive-to-Negative Converter

INDUCTOR VALUE

The criteria for choosing the inductor is typically based on ensuring that peak switch current rating is not exceeded. This gives the lowest value of inductance that can be used, but in some cases (lower output load currents) it may give a value that creates unnecessarily high output ripple voltage.

The difficulty in calculating the minimum inductor size needed is that you must first decide whether the switcher will be in continuous or discontinuous mode at the critical point where switch current reaches 3A. The first step is to use the following formula to calculate the load current above which the switcher must use continuous mode. If your load current is less than this, use the discontinuous mode formula to calculate minimum inductor needed. If load current is higher, use the continuous mode formula.

Output current where continuous mode is needed:

$$I_{CONT} > \sqrt{\frac{(V_{IN})^2 (I_P)^2}{4(V_{IN}+V_{OUT})(V_{IN}+V_{OUT}+V_F)}}$$

Minimum inductor discontinuous mode:

$$L_{MIN} = \frac{2(V_{OUT})(I_{OUT})}{(f)(I_P)^2}$$

Minimum inductor continuous mode:

$$L_{MIN} = \frac{(V_{IN})(V_{OUT})}{2(f)(V_{IN}+V_{OUT})\left[I_P - I_{OUT}\left(1+\frac{(V_{OUT}+V_F)}{V_{IN}}\right)\right]}$$

For a 40V to –12V converter using the LT3430/LT3430-1 with peak switch current of 3A and a catch diode of 0.52V:

$$I_{CONT} = \sqrt{\frac{(40)^2 (3)^2}{4(40+12)(40+12+0.52)}} = 1.148A$$

For a load current of 0.5A, this says that discontinuous mode can be used and the minimum inductor needed is found from:

$$L_{MIN} = \frac{2(12)(0.5)}{(200 \bullet 10^3)(3)^2} = 6.7\mu H$$

In practice, the inductor should be increased by about 30% over the calculated minimum to handle losses and variations in value. This suggests a minimum inductor of 10µH for this application.

Ripple Current in the Input and Output Capacitors

Positive-to-negative converters have high ripple current in the input capacitor. For long capacitor lifetime, the RMS value of this current must be less than the high frequency ripple current rating of the capacitor. The following formula will give an *approximate* value for RMS ripple current. *This formula assumes continuous mode and large inductor value*. Small inductors will give somewhat higher ripple current, especially in discontinuous mode. The exact formulas are very complex and appear in Application Note 44, pages 29 and 30. For our purposes here I have simply added a fudge factor (ff). The value for ff is about 1.2 for higher load currents and L ≥15µH. It increases to about 2.0 for smaller inductors at lower load currents.

$$\text{Capacitor } I_{RMS} = (ff)(I_{OUT})\sqrt{\frac{V_{OUT}}{V_{IN}}}$$

ff = 1.2 to 2.0

The output capacitor ripple current for the positive-to-negative converter is similar to that for a typical buck regulator—it is a triangular waveform with peak-to-peak

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value equal to the peak-to-peak triangular waveform of the inductor. The low output ripple design in Figure 15 places the input capacitor between V_{IN} and the regulated negative output. This placement of the input capacitor significantly reduces the size required for the output capacitor (versus placing the input capacitor between V_{IN} and ground).

The peak-to-peak ripple current in both the inductor and output capacitor (assuming continuous mode) is:

$$I_{P-P} = \frac{DC \bullet V_{IN}}{f \bullet L}$$

$$DC = \text{Duty Cycle} = \frac{V_{OUT} + V_F}{V_{OUT} + V_{IN} + V_F}$$

$$I_{COUT}\ (RMS) = \frac{I_{P-P}}{\sqrt{12}}$$

The output ripple voltage for this configuration is as low as the typical buck regulator based predominantly on the inductor's triangular peak-to-peak ripple current and the ESR of the chosen capacitor (see Output Ripple Voltage in Applications Information).

Diode Current

Average diode current is equal to load current. *Peak* diode current will be considerably higher.

Peak diode current:

Continuous Mode =

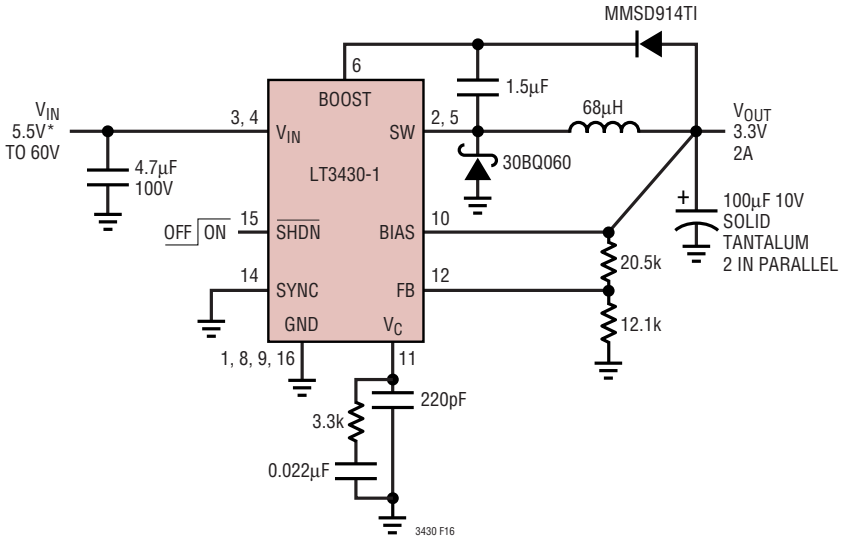
$$I_{OUT}\frac{(V_{IN} + V_{OUT})}{V_{IN}} + \frac{(V_{IN})(V_{OUT})}{2(L)(f)(V_{IN} + V_{OUT})}$$

$$\text{Discontinuous Mode} = \sqrt{\frac{2(I_{OUT})(V_{OUT})}{(L)(f)}}$$

Keep in mind that during start-up and output overloads, average diode current may be much higher than with normal loads. Care should be used if diodes rated less than 1A are used, especially if continuous overload conditions must be tolerated.

TYPICAL APPLICATION

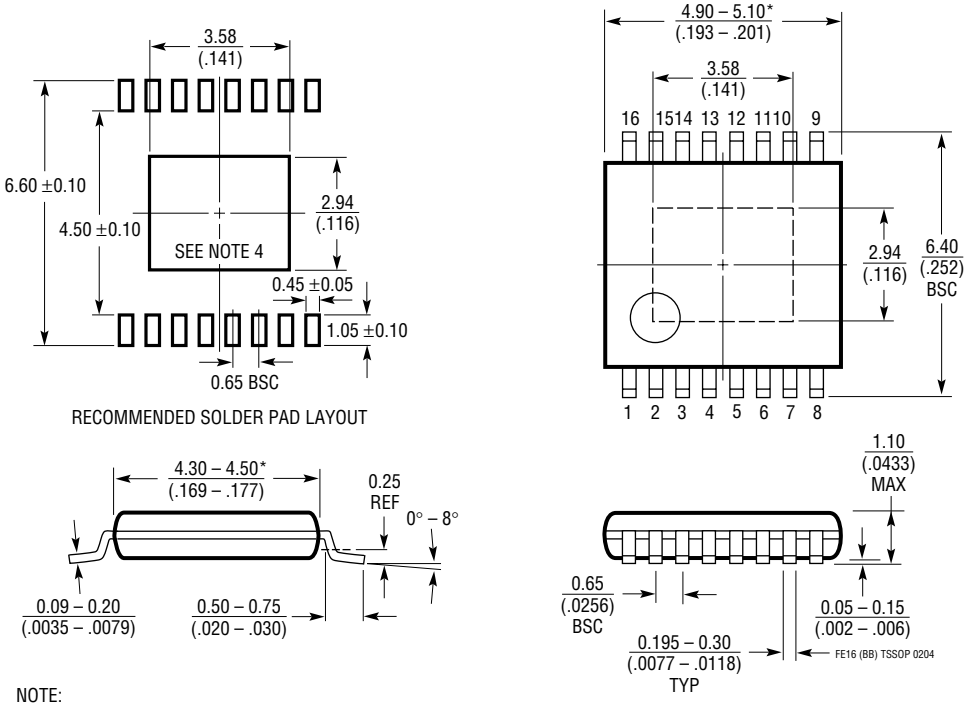
3.3V, 2A Buck Converter



*FOR INPUT VOLTAGES BELOW 7.5V, SOME RESTRICTIONS MAY APPLY

PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1074/LT1074HV	4.4A (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converters	V_{IN}: 7.3V to 45V/64V, $V_{OUT(MIN)}$: 2.21V, I_Q: 8.5mA, I_{SD}: 10µA DD-5/7, TO220-5/7
LT1076/LT1076HV	1.6A (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converters	V_{IN}: 7.3V to 45V/64V, $V_{OUT(MIN)}$: 2.21V, I_Q: 8.5mA, I_{SD}: 10µA DD-5/7, TO220-5/7
LT1676	60V, 440mA (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 60V, $V_{OUT(MIN)}$: 1.24V, I_Q: 3.2mA, I_{SD}: 2.5µA, S8
LT1765	25V, 2.75A (I_{OUT}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$: 1.20V, I_Q: 1mA, I_{SD}: 15µA, S8, TSSOP16E
LT1766	60V, 1.2A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$: 1.20V, I_Q: 2.5mA, I_{SD}: 25µA, TSSOP16/E
LT1767	25V, 1.2A (I_{OUT}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$: 1.20V, I_Q: 1mA, I_{SD}: 6µA, MS8/E
LT1776	40V, 550mA (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 40V, $V_{OUT(MIN)}$: 1.24V, I_Q: 3.2mA, I_{SD}: 30µA, N8, S8
LT1940	25V, Dual 1.2A (I_{OUT}), 1.1MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$: 1.2V, I_Q: 3.8mA, I_{SD}: <1µA, TSSOP16E
LT1956	60V, 1.2A (I_{OUT}), 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$: 1.20V, I_Q: 2.5mA, I_{SD}: 25µA, TSSOP16/E
LT1976	60V, 1.2A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter with Burst Mode® Operation	V_{IN}: 3.3V to 60V, $V_{OUT(MIN)}$: 1.20V, I_Q: 100µA, I_{SD}: <1µA, TSSOP16/E
LT3010	80V, 50mA Low Noise Linear Regulator	V_{IN}: 1.5V to 80V, $V_{OUT(MIN)}$: 1.28V, I_Q: 30µA, I_{SD}: <1µA, MSE8
LTC3407	Dual 600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$: 0.6V, I_Q: 40µA, I_{SD}: <1µA, MS10E
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$: 0.8V, I_Q: 60µA, I_{SD}: <1µA, TSSOP16E
LTC3414	4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	V_{IN}: 2.3V to 5.5V, $V_{OUT(MIN)}$: 0.8V, I_Q: 64µA, I_{SD}: <1µA, TSSOP20E
LT3430/LT3431	60V, 2.75A (I_{OUT}), 200kHz/500kHz, High Efficiency Step-Down DC/DC Converters	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$: 1.20V, I_Q: 2.5mA, I_{SD}: 30µA, TSSOP16E
LT3433	60V, 400mA (I_{OUT}), 200kHz, High Efficiency Step-Up Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 4V to 60V, $V_{OUT(MIN)}$: 3.3V to 20V, I_Q: 100µA, I_{SD}: <1µA, TSSOP16E
LTC3727/LTC3727-1	36V, 500kHz, High Efficiency Step-Down DC/DC Controllers	V_{IN}: 4V to 36V, $V_{OUT(MIN)}$: 0.8V, I_Q: 670µA, I_{SD}: 20µA, QFN-32, SSOP-28

Burst Mode is a registered trademark of Linear Technology Corporation.

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