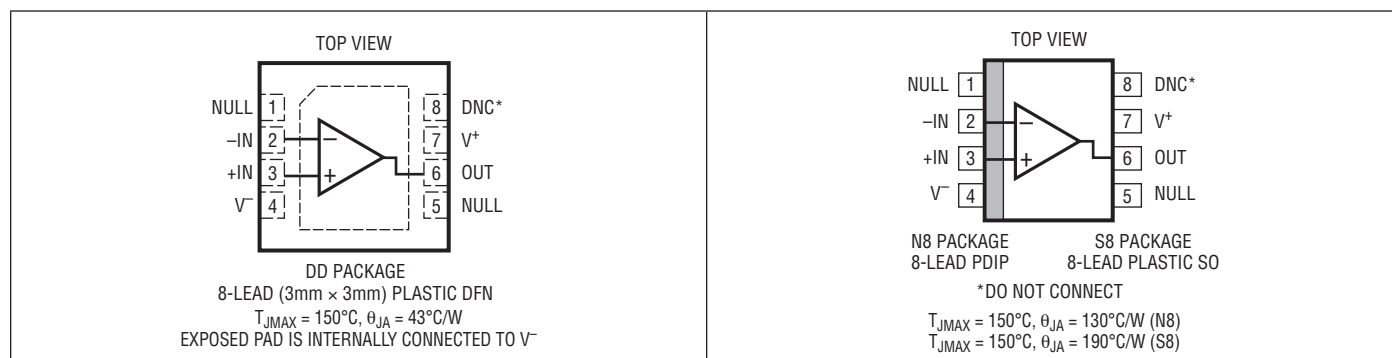


LT1468

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-).....	36V	Specified Temperature Range (Note 4)	-40°C to 85°C
Maximum Input Current (Note 2).....	10mA	Junction Temperature	150°C
Output Short-Circuit Duration (Note 3)	Indefinite	Storage Temperature.....	-65°C to 150°C
Operating Temperature Range	-40°C to 85°C	Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1468CN8#PBF	NA	LT1468CN8	8-Lead PDIP	0°C to 70°C
LT1468IN8#PBF	NA	LT1468IN8	8-Lead PDIP	-40°C to 85°C
LT1468CS8#PBF	LT1468CS8#TRPBF	1468	8-Lead Plastic Small Outline	0°C to 70°C
LT1468IS8#PBF	LT1468IS8#TRPBF	1468I	8-Lead Plastic Small Outline	-40°C to 85°C
LT1468ACDD#PBF	LT1468ACDD#TRPBF	LDJX	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT1468AIDD#PBF	LT1468AIDD#TRPBF	LDJX	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LT1468CDD#PBF	LT1468CDD#TRPBF	LDJX	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT1468IDD#PBF	LT1468IDD#TRPBF	LDJX	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1468CN8	NA	LT1468CN8	8-Lead PDIP	0°C to 70°C
LT1468IN8	NA	LT1468IN8	8-Lead PDIP	-40°C to 85°C
LT1468CS8	LT1468CS8#TR	1468	8-Lead Plastic Small Outline	0°C to 70°C
LT1468IS8	LT1468IS8#TR	1468I	8-Lead Plastic Small Outline	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V _{SUPPLY}		MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	N8, S8	±15V			30	75	μV
			±5V		50	175	μV	
		LT1468A, DD Package	±15V		30	75	μV	
			±5V		50	175	μV	
		LT1468, DD Package	±15V			100	200	μV
			±5V			150	300	μV
I _{OS}	Input Offset Current		±5V to ±15V			13	50	nA
I _B [−]	Inverting Input Bias Current		±5V to ±15V			3	±10	nA
I _B ⁺	Noninverting Input Bias Current		±5V to ±15V			−10	±40	nA
	Input Noise Voltage	0.1Hz to 10Hz	±5V to ±15V			0.3		μV _{P-P}
e _n	Input Noise Voltage	f = 10kHz	±5V to ±15V			5		nV/√Hz
i _n	Input Noise Voltage	f = 10kHz	±5V to ±15V			0.6		pA/√Hz
R _{IN}	Input Resistance	V _{CM} = ±12.5V Differential	±15V		100	240		MΩ
			±15V		50	150		kΩ
C _{IN}	Input Capacitance		±15V		4			pF
	Input Voltage Range +		±15V		12.5	13.5		V
			±5V		2.5	3.5		V
	Input Voltage Range −		±15V		−14.3	−12.5		V
		±5V		−4.3	−2.5		V	
CMRR	Common Mode Rejection Ratio	V _{CM} = ±12.5V	±15V		96	110		dB
		V _{CM} = ±2.5V	±5V		96	112		dB
PSRR	Power Supply Rejection Ratio	V _S = ±4.5V to ±15V			100	112		dB
A _{VOL}	Large-Signal Voltage Gain	V _{OUT} = ±12.5V, R _L = 10k	±15V		1000	9000		V/mV
		V _{OUT} = ±12.5V, R _L = 2k	±15V		500	5000		V/mV
		V _{OUT} = ±2.5V, R _L = 10k	±5V		1000	6000		V/mV
		V _{OUT} = ±2.5V, R _L = 2k	±5V		500	3000		V/mV
V _{OUT}	Output Swing	R _L = 10k	±15V		±13.0	±13.6		V
		R _L = 2k	±15V		±12.8	±13.5		V
		R _L = 10k	±5V		±3.0	±3.6		V
		R _L = 2k	±5V		±2.8	±3.5		V
I _{OUT}	Output Current	V _{OUT} = ±12.5V	±15V		±15	±22		mA
		V _{OUT} = ±2.5V	±5V		±15	±22		mA
I _{SC}	Short-Circuit Current	V _{OUT} = 0V, V _{IN} = ±0.2V	±15V		±25	±40		mA
SR	Slew Rate	A _V = −1, R _L = 2k (Note 5)	±15V		15	22		V/μs
			±5V		11	17		V/μs
	Full-Power Bandwidth	10V Peak, (Note 6) 3V Peak, (Note 6)	±15V			350		kHz
			±5V			900		kHz
GBW	Gain Bandwidth	f = 100kHz, R _L = 2k	±15V		60	90		MHz
			±5V		55	88		MHz
THD	Total Harmonic Distortion	A _V = 2, V _O = 10V _{P-P} , f = 1kHz	±15V		0.00007			%
		A _V = 2, V _O = 10V _{P-P} , f = 100kHz	±15V		0.0015			%
t _r , t _f	Rise Time, Fall Time	A _V = 1, 10% to 90%, 0.1V	±15V		11			ns
			±5V		12			ns
		Overshoot	A _V = 1, 0.1V	±15V		30		%
			±5V		35		%	
	Propagation Delay	A _V = 1, 50% V _{IN} to 50% V _{OUT} , 0.1V	±15V		9			ns
			±5V		10			ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
t_s	Settling Time	10V Step, 0.01%, $A_V = -1$	$\pm 15\text{V}$		760		ns
		10V Step, $150\mu\text{V}$, $A_V = -1$	$\pm 15\text{V}$		900		ns
		5V Step, 0.01%, $A_V = -1$	$\pm 5\text{V}$		770		ns
R_O	Output Resistance	$A_V = 1$, $f = 100\text{kHz}$	$\pm 15\text{V}$		0.02		Ω
I_S	Supply Current		$\pm 15\text{V}$		3.9	5.2	mA
			$\pm 5\text{V}$		3.6	5.0	mA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	N8, S8	$\pm 15\text{V}$	●		150	μV
			$\pm 5\text{V}$	●		250	μV
		LT1468A, DD Package	$\pm 15\text{V}$	●		150	μV
			$\pm 5\text{V}$	●		250	μV
		LT1468, DD Package	$\pm 15\text{V}$	●		300	μV
			$\pm 5\text{V}$	●		400	μV
	Input V_{OS} Drift	(Note 7)	$\pm 5\text{V}$ to $\pm 15\text{V}$	●	0.7	2.0	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●		65	nA
	Input Offset Current Drift		$\pm 5\text{V}$ to $\pm 15\text{V}$		60		$\text{pA}/^\circ\text{C}$
I_{B^-}	Inverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●		± 15	nA
	Negative Input Current Drift		$\pm 5\text{V}$ to $\pm 15\text{V}$		40		$\text{pA}/^\circ\text{C}$
I_{B^+}	Noninverting Input Bias Current		$\pm 5\text{V}$ to $\pm 15\text{V}$	●		± 50	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12.5\text{V}$	$\pm 15\text{V}$	●	94		dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	94		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 15\text{V}$		●	98		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12.5\text{V}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	●	500		V/mV
		$V_{OUT} = \pm 12.5\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	250		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 10\text{k}$	$\pm 5\text{V}$	●	500		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	●	250		V/mV
V_{OUT}	Output Swing	$R_L = 10\text{k}$	$\pm 15\text{V}$	●	± 12.9		V
		$R_L = 2\text{k}$	$\pm 15\text{V}$	●	± 12.7		V
		$R_L = 10\text{k}$	$\pm 5\text{V}$	●	± 2.9		V
		$R_L = 2\text{k}$	$\pm 5\text{V}$	●	± 2.7		V
I_{OUT}	Output Current	$V_{OUT} = \pm 12.5\text{V}$	$\pm 15\text{V}$	●	± 12.5		mA
		$V_{OUT} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	± 12.5		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 0.2\text{V}$	$\pm 15\text{V}$	●	± 17		mA
SR	Slew Rate	$A_V = -1$, $R_L = 2\text{k}$ (Note 5)	$\pm 15\text{V}$	●	13		V/ μs
			$\pm 5\text{V}$	●	9		V/ μs
GBW	Gain Bandwidth	$f = 100\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	●	55		MHz
			$\pm 5\text{V}$	●	50		MHz
I_S	Supply Current		$\pm 15\text{V}$	●		6.5	mA
			$\pm 5\text{V}$	●		6.3	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V _{SUPPLY}		MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	N8, S8	±15V	●			230	μV
			±5V	●			330	μV
		LT1468A, DD Package	±15V	●			230	μV
			±5V	●			330	μV
		LT1468, DD Package	±15V	●			400	μV
			±5V	●			500	μV
	Input V _{OS} Drift	(Note 7)	±5V to ±15V	●		0.7	2.5	μV/°C
I _{OS}	Input Offset Current		±5V to ±15V	●			80	nA
	Input Offset Current Drift		±5V to ±15V			120		pA/°C
I _B ⁻	Inverting Input Bias Current		±5V to ±15V	●			±30	nA
	Negative Input Current Drift		±5V to ±15V			80		pA/°C
I _B ⁺	Noninverting Input Bias Current		±5V to ±15V	●			±60	nA
CMRR	Common Mode Rejection Ratio	V _{CM} = ±12.5V V _{CM} = ±2.5V	±15V	●	92			dB
			±5V	●	92			dB
PSRR	Power Supply Rejection Ratio	V _S = ±4.5V to ±15V		●	96			dB
A _{VOL}	Large-Signal Voltage Gain	V _{OUT} = ±12V, R _L = 10k	±15V	●	300			V/mV
		V _{OUT} = ±10V, R _L = 2k	±15V	●	150			V/mV
		V _{OUT} = ±2.5V, R _L = 10k	±5V	●	300			V/mV
		V _{OUT} = ±2.5V, R _L = 2k	±5V	●	150			V/mV
V _{OUT}	Output Swing	R _L = 10k	±15V	●	±12.8			V
		R _L = 2k	±15V	●	±12.6			V
		R _L = 10k	±5V	●	±2.8			V
		R _L = 2k	±5V	●	±2.6			V
I _{OUT}	Output Current	V _{OUT} = ±12.5V	±15V	●	±7			mA
		V _{OUT} = ±2.5V	±5V	●	±7			mA
I _{SC}	Short-Circuit Current	V _{OUT} = 0V, V _{IN} = ±0.2V	±15V	●	±12			mA
SR	Slew Rate	A _V = -1, R _L = 2k (Note 5)	±15V	●	9			V/μs
			±5V	●	6			V/μs
GBW	Gain Bandwidth	f = 100kHz, R _L = 2k	±15V	●	45			MHz
			±5V	●	40			MHz
I _S	Supply Current		±15V	●			7.0	mA
			±5V	●			6.8	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes and two 100Ω series resistors. If the differential input voltage exceeds 0.7V, the input current should be limited to 10mA. Input voltages outside the supplies will be clamped by ESD protection devices and input currents should also be limited to 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: The LT1468C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended temperature limits, but is not tested at -40°C and at 85°C. The LT1468I is guaranteed to meet the extended temperature limits.

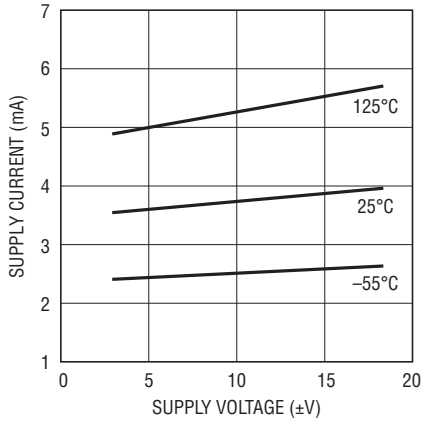
Note 5: Slew rate is measured between ±8V on the output with ±12V input for ±15V supplies and ±2V on the output with ±3V input for ±5V supplies.

Note 6: Full power bandwidth is calculated from the slew rate measurement: $\text{FPBW} = \text{SR}/2\pi V_p$

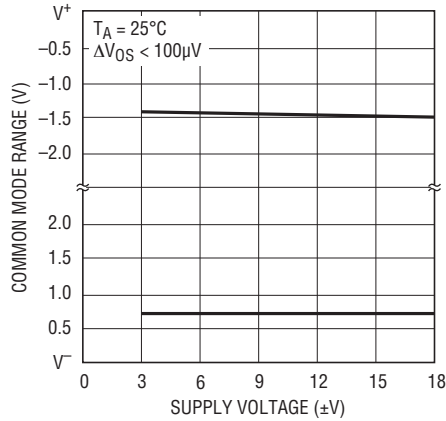
Note 7: This parameter is not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

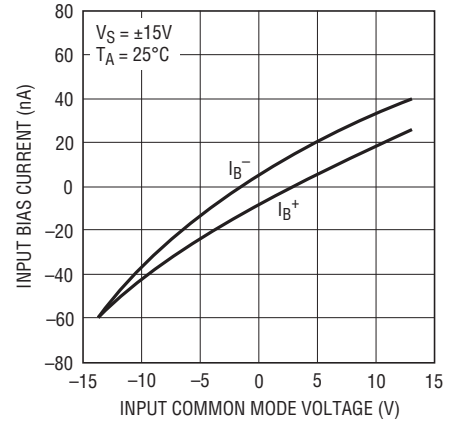
Supply Current vs Supply Voltage and Temperature



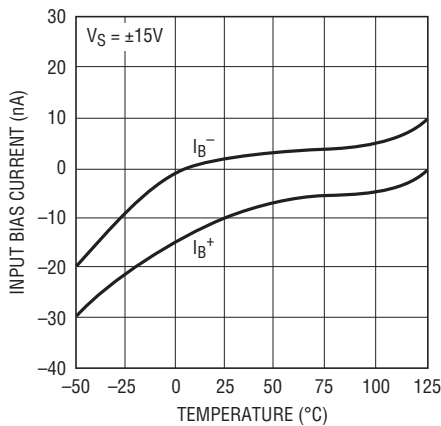
Input Common Mode Range vs Supply Voltage



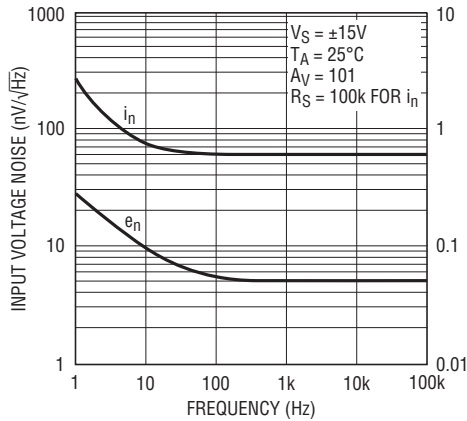
Input Bias Current vs Input Common Mode Voltage



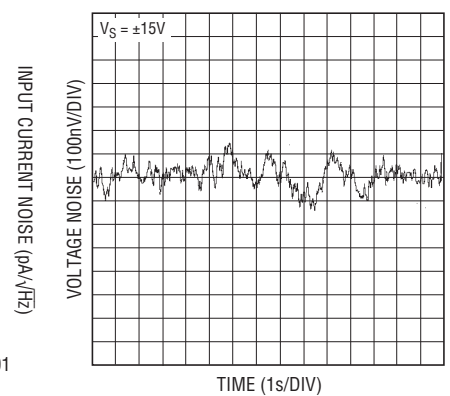
Input Bias Current vs Temperature



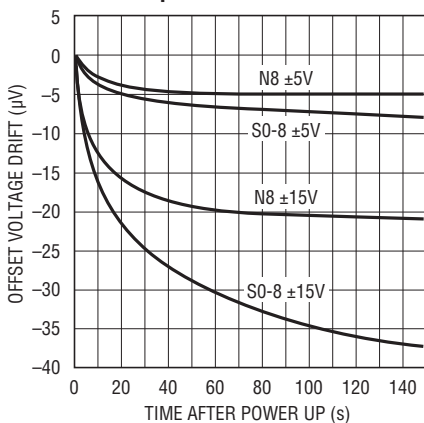
Input Noise Spectral Density



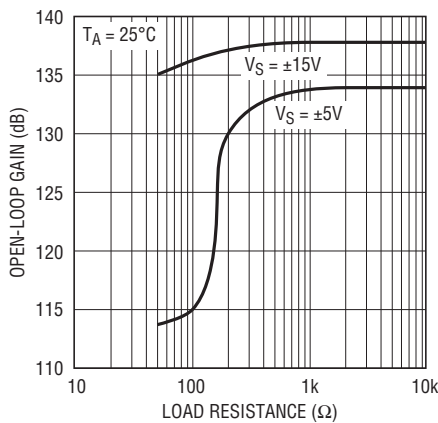
0.1Hz to 10Hz Voltage Noise



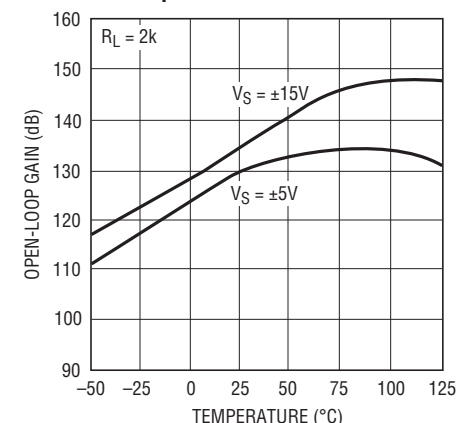
Warm-Up Drift vs Time



Open-Loop Gain vs Resistive Load

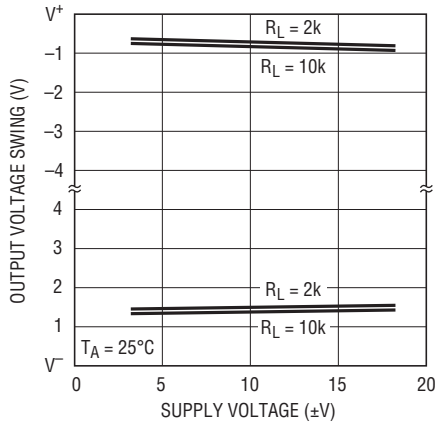


Open-Loop Gain vs Temperature

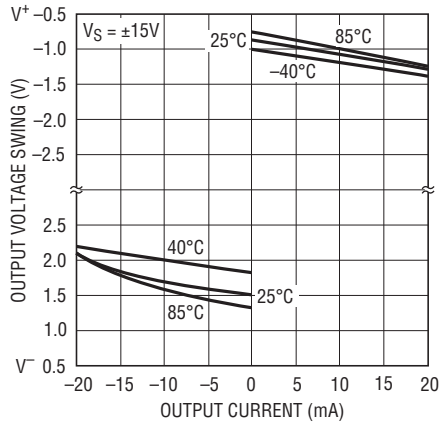


TYPICAL PERFORMANCE CHARACTERISTICS

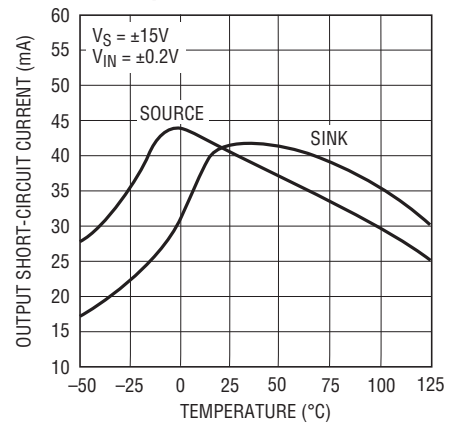
Output Voltage Swing vs Supply Voltage



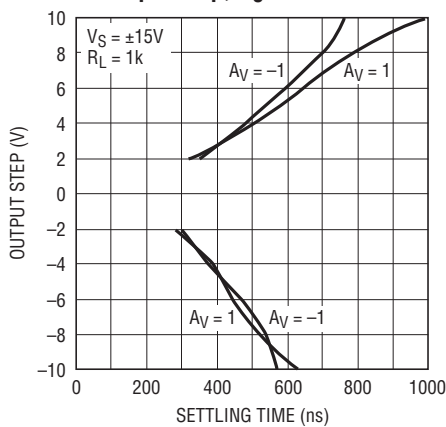
Output Voltage Swing vs Load Current



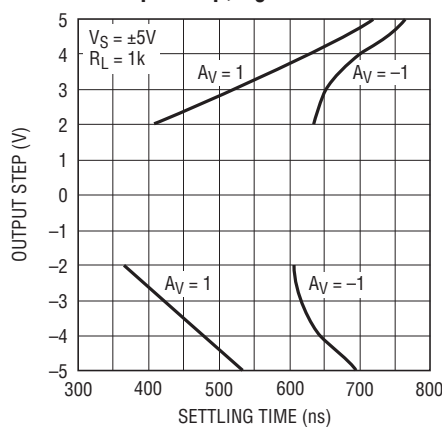
Output Short-Circuit Current vs Temperature



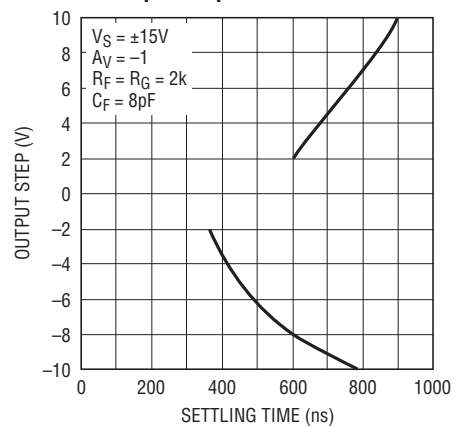
Settling Time to 0.01% vs Output Step, VS = ±15V



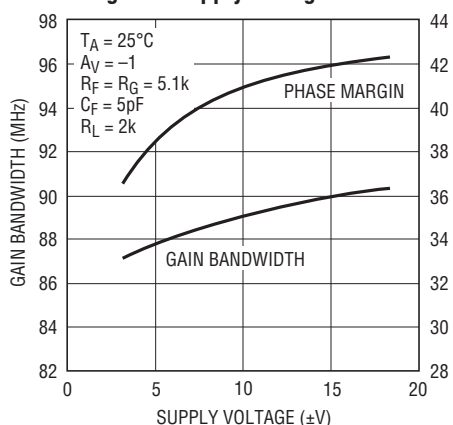
Settling Time to 0.01% vs Output Step, VS = ±5V



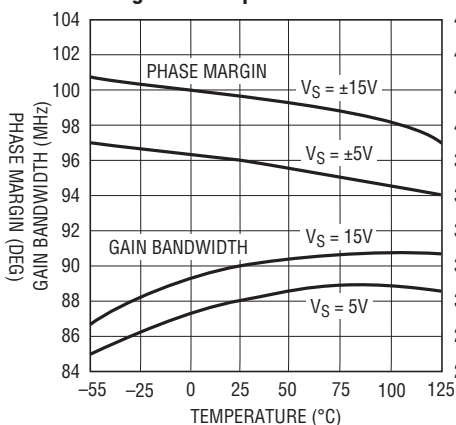
Settling Time to 150µV vs Output Step



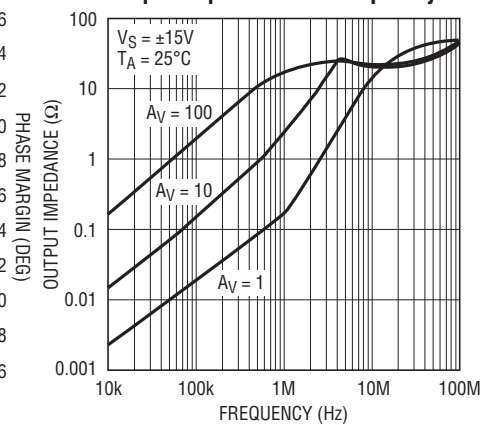
Gain Bandwidth and Phase Margin vs Supply Voltage



Gain Bandwidth and Phase Margin vs Temperature

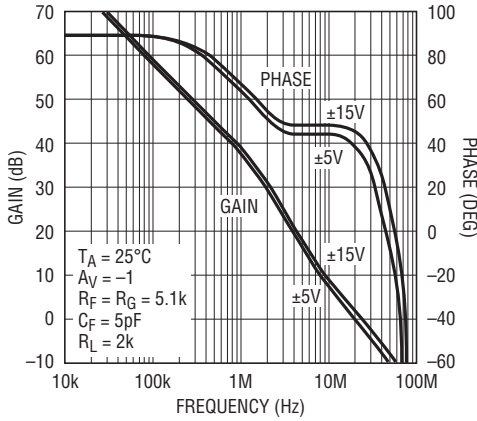


Output Impedance vs Frequency

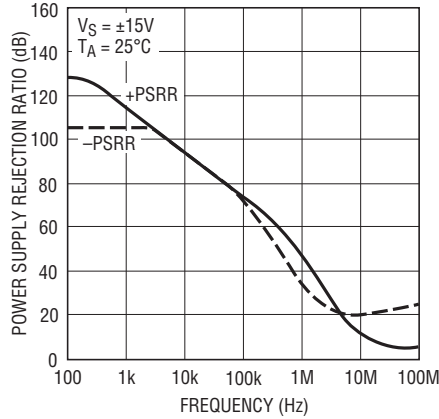


TYPICAL PERFORMANCE CHARACTERISTICS

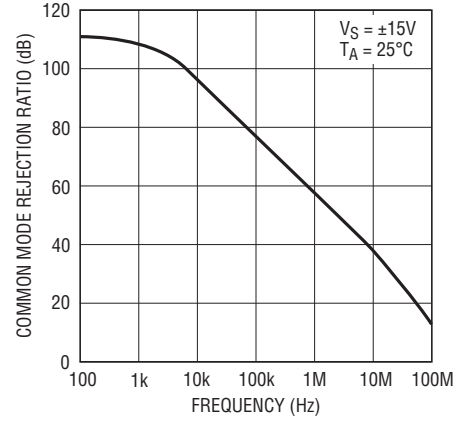
Gain and Phase vs Frequency



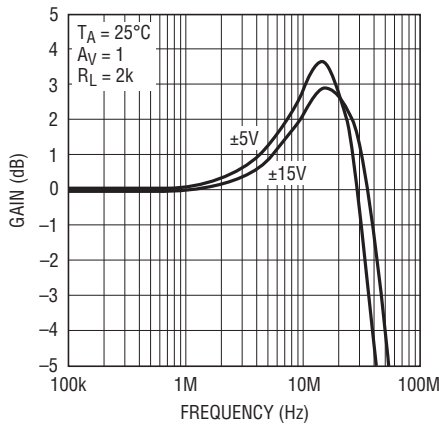
Power Supply Rejection Ratio vs Frequency



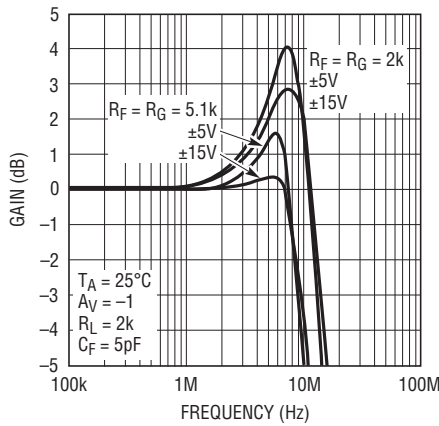
Common Mode Rejection Ratio vs Frequency



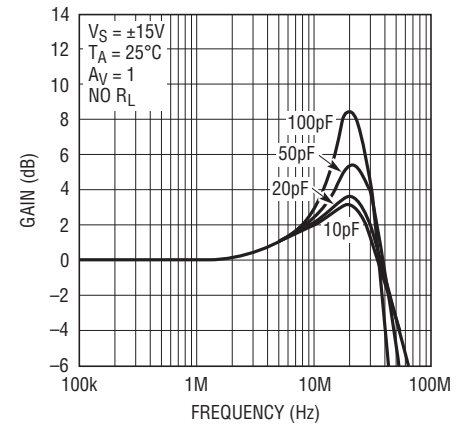
Frequency Response vs Supply Voltage, $A_V = 1$



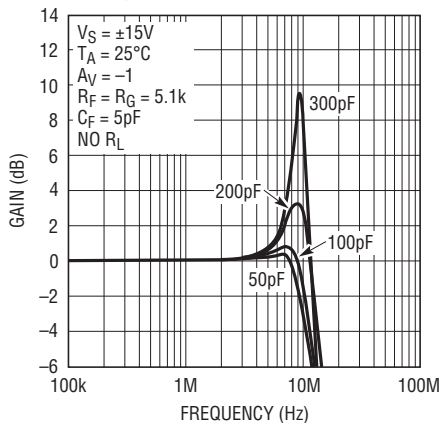
Frequency Response vs Supply Voltage, $A_V = -1$



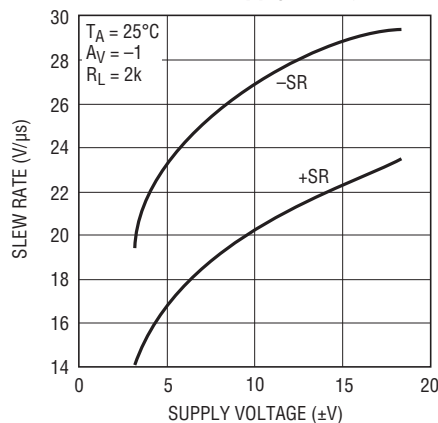
Frequency Response vs Capacitive Load, $A_V = 1$



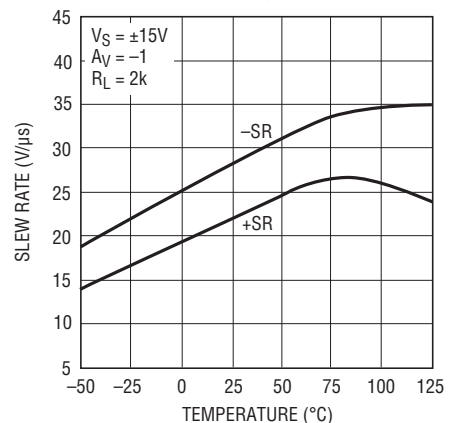
Frequency Response vs Capacitive Load, $A_V = -1$



Slew Rate vs Supply Voltage

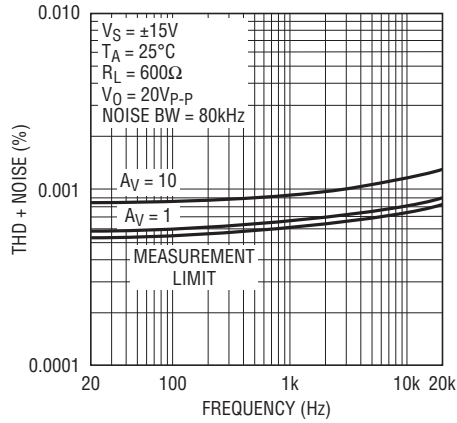


Slew Rate vs Temperature

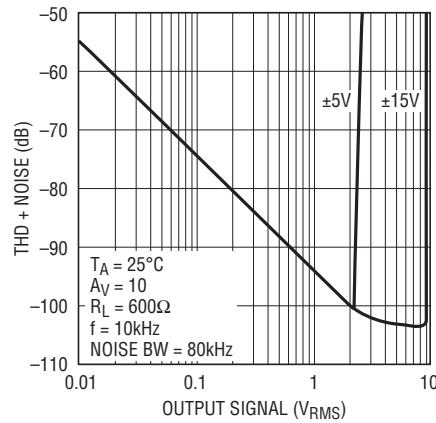


TYPICAL PERFORMANCE CHARACTERISTICS

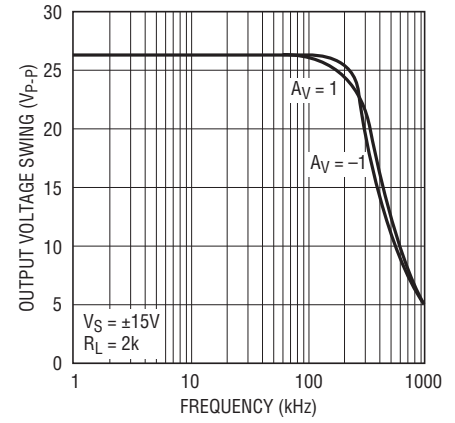
Total Harmonic Distortion + Noise vs Frequency



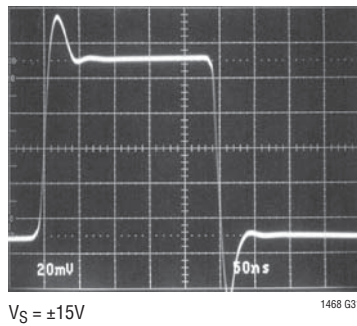
Total Harmonic Distortion + Noise vs Amplitude



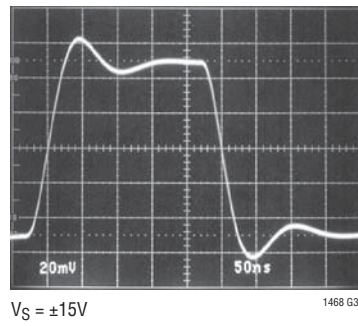
Undistorted Output Swing vs Frequency, ±15V



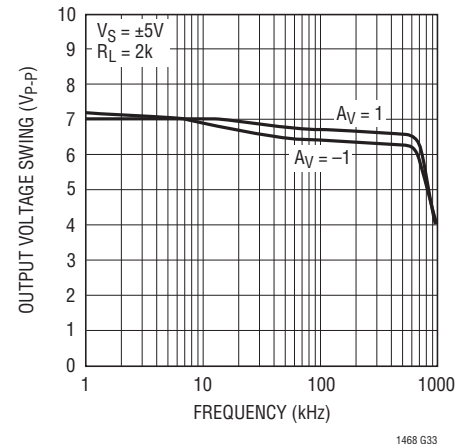
Small-Signal Transient, AV = 1



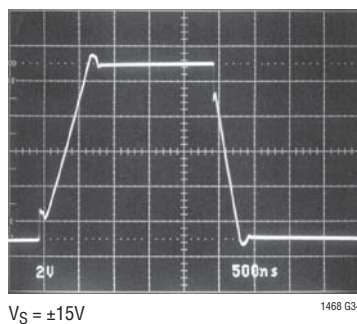
Small-Signal Transient, AV = -1



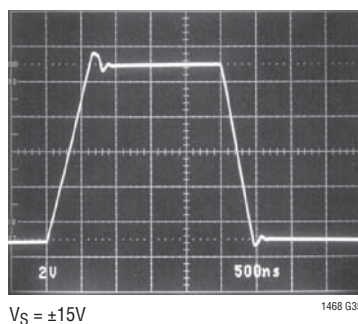
Undistorted Output Swing vs Frequency, ±5V



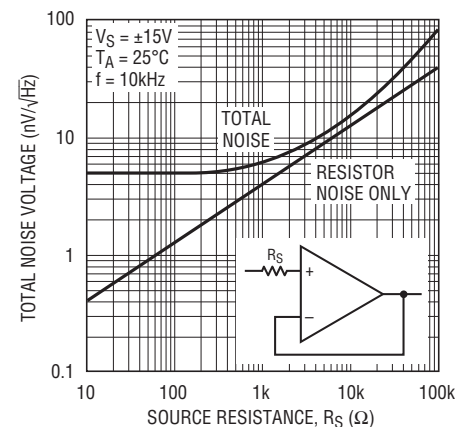
Large-Signal Transient, AV = 1



Large-Signal Transient, AV = -1

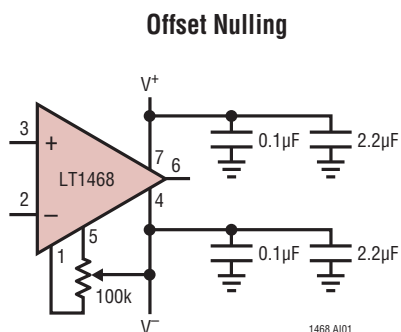


Total Noise vs Unmatched Source Resistance



APPLICATIONS INFORMATION

The LT1468 may be inserted directly into many operational amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1468 is shown below.



Layout and Passive Components

The LT1468 requires attention to detail in board layout in order to maximize DC and AC performance. For best AC results (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF) in parallel with low ESR bypass capacitors (1µF to 10µF tantalum). For best DC performance, use “star” grounding techniques, equalize input trace lengths and minimize leakage (i.e., 1.5GΩ of leakage between an input and a 15V supply will generate 10nA—equal to the maximum I_{B^-} specification.)

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs. For inverting configurations tie the ring to ground, in noninverting connections tie the ring to the inverting input (note the input capacitance will increase which may require a compensating capacitor as discussed below.)

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the

contacts to the inputs can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

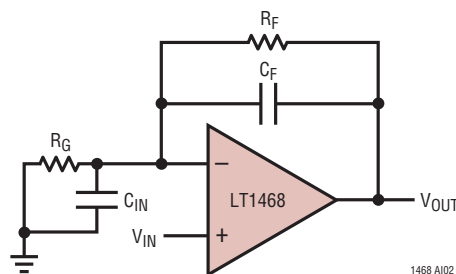
Make no connection to Pin 8. This pin is used for factory trim of the inverting input current.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole that can cause peaking or even oscillations. For feedback resistors greater than 2k, a feedback capacitor of the value:

$$C_F > (R_G)(C_{IN}/R_F)$$

should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one, and a large feedback resistor is used, C_F should be greater than or equal to C_{IN} . An example would be a DAC I-to-V converter as shown on the front page of this data sheet where the DAC can have many tens of pF of output capacitance. Another example would be a gain of –1 with 5k resistors; a 5pF to 10pF capacitor should be added across the feedback resistor. The frequency response in a gain of –1 is shown in the Typical Performance curves with 2k and 5.1k resistors with a 5pF feedback capacitor.

Nulling Input Capacitance



APPLICATIONS INFORMATION

Input Considerations

Each input of the LT1468 is protected with a 100Ω series resistor and back-to-back diodes across the bases of the input devices. If the inputs can be pulled apart, the input current should be limited to less than 10mA with an external series resistor. Each input also has two ESD clamp diodes—one to each supply. If an input is driven above the supply, limit the current with an external resistor to less than 10mA.

The LT1468 employs bias current cancellation at the inputs. The inverting input current is trimmed at zero common mode voltage to minimize errors in inverting applications such as I-to-V converters. The noninverting input current is not trimmed and has a wider variation and therefore a larger maximum value. As the input offset current can be greater than either input current, the use of balanced source resistance is NOT recommended as it actually degrades DC accuracy and also increases noise.

The input bias currents vary with common mode voltage as shown in the Typical Performance Characteristics. The cancellation circuitry was not designed to track this common mode voltage because the settling time would have been adversely affected.

The LT1468 inputs can be driven to the negative supply and to within 0.5V of the positive supply without phase reversal. As the input moves closer than 0.5V to the positive supply, the output reverses phase.

Total Input Noise

The curve of Total Noise vs Unmatched Source Resistance in the Typical Performance Characteristics shows that with source resistance below 1k, the voltage noise of the amplifier dominates. In the 1k to 20k region the increase in noise is due to the source resistance. Above 20k the input current noise component is larger than the resistor noise.

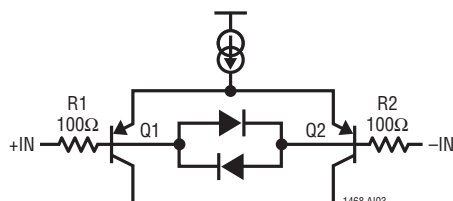
Capacitive Loading

The LT1468 drives capacitive loads of up to 100pF in unity gain and 300pF in a gain of -1 . When there is a need to drive a larger capacitive load, a small series resistor should be inserted between the output and the load. In addition, a capacitor should be added between the output and the inverting input as shown in Driving Capacitive Loads.

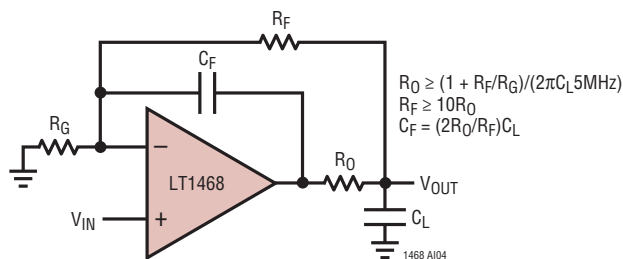
Settling Time

The LT1468 is a single stage amplifier with an optimal thermal layout that leads to outstanding settling performance. Measuring settling, even at the 12-bit level is very challenging, and at the 16-bit level requires a great deal of subtlety and expertise. Fortunately, there are two excellent Linear Technology reference sources for settling measurements, Application Notes 47 and 74. Appendix B of AN47 is a vital primer on 12-bit settling measurements, and AN74 extends the state of the art while concentrating on settling time with a 16-bit current output DAC input.

Input Stage Protection



Driving Capacitive Loads



APPLICATIONS INFORMATION

The 150 μ V settling curve in the Typical Performance Characteristics is measured using the Differential Amplifier method of AN74 followed by a clamped, nonsaturating gain of 100. The total gain of 500 allows a resolution of 100 μ V/DIV with an oscilloscope setting of 0.05V/DIV

The settling of the DAC I-to-V converter on the front page was measured using the exact methods of AN74. The optimum nulling of the DAC output capacitance requires 20pF across the 6k feedback resistor. The theoretical limit for 16-bit settling is 11.1 times this RC time constant or 1.33 μ s. The actual settling time is 1.7 μ s at the output of the LT1468. The LT1468 is the fastest Linear Technology amplifier in this application.

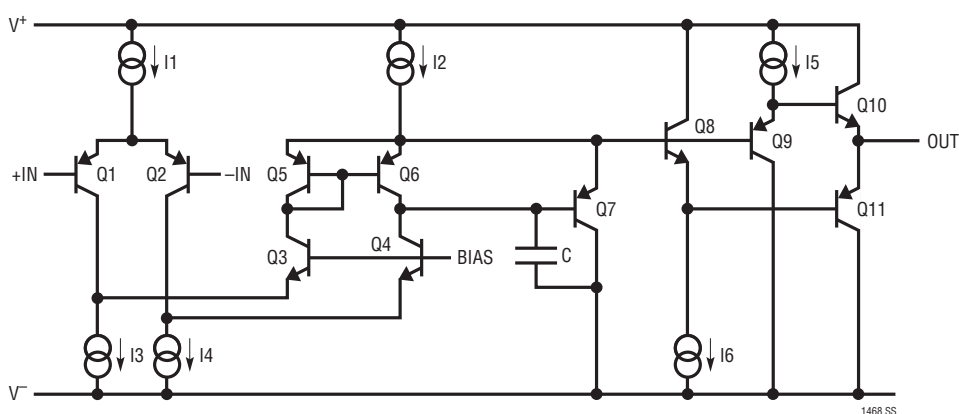
The optional noise filter adds a slight delay of 100ns, but reduces the noise bandwidth to 1.6MHz which increases the output resolution for 16-bit accuracy.

Distortion

The LT1468 has outstanding distortion performance as shown in the Typical Performance curves of Total Harmonic Distortion + Noise vs Frequency and Amplitude. The high open-loop gain and inherently balanced architecture reduce errors to yield 16-bit accuracy to frequencies as high as 100kHz. An example of this performance is the Typical Application titled 100kHz Low Distortion Bandpass Filter. This circuit is useful for cleaning up the output of a high performance signal generator such as the B & K type 1051 or HP3326A.

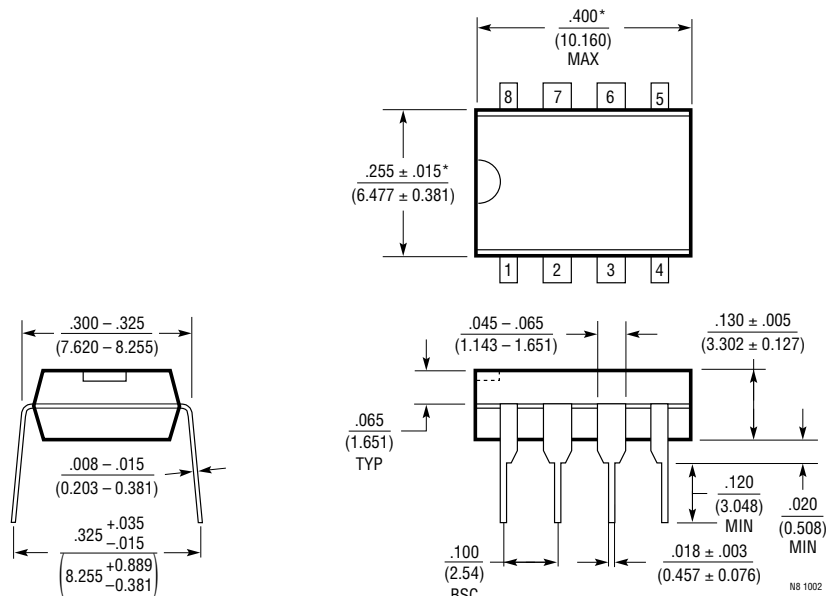
Another key application for LT1468 is buffering the input to a 16-bit A/D converter. In a gain of 1 or 2 this straightforward circuit provides uncorrupted AC and DC levels to the converter, while buffering the A/D input sample-and-hold circuit from high source impedance which can reduce the maximum sampling rate. The front page graph shows better than 16-bit distortion for a gain of 2 with a 10V_{P-P} output.

SIMPLIFIED SCHEMATIC

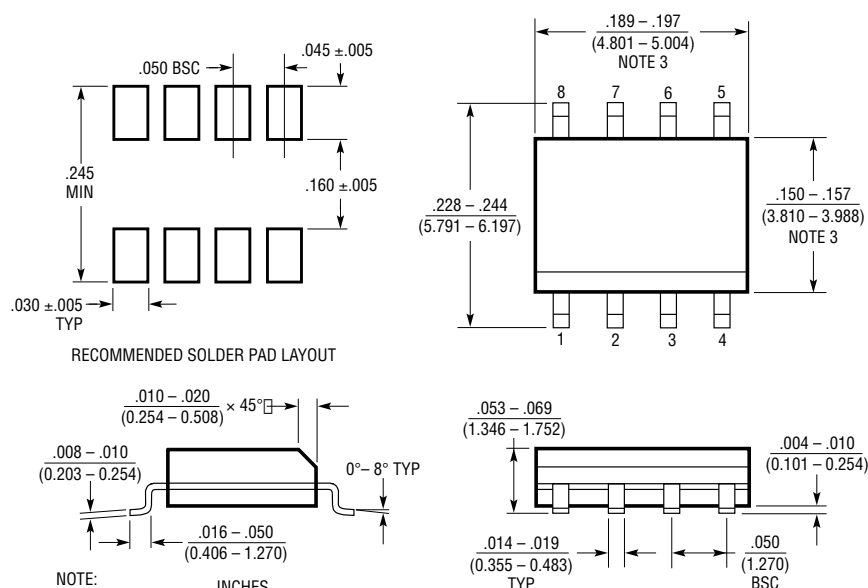


PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow 0.300)
 (LTC DWG # 05-08-1510)



S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
 (LTC DWG # 05-08-1610)



S08 0303

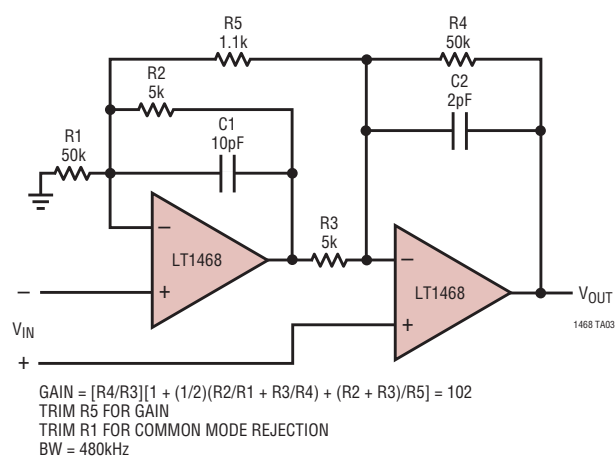
1468fb

REVISION HISTORY (Revision history begins at Rev B)

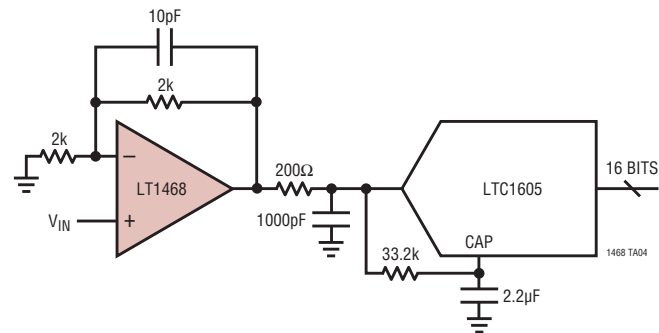
REV	DATE	DESCRIPTION	PAGE NUMBER
B	10/09	Change to Both Packages in Pin Configuration	2

TYPICAL APPLICATIONS

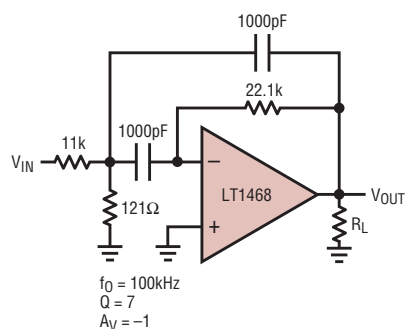
Instrumentation Amplifier



16-Bit ADC Buffer



100kHz Low Distortion Bandpass Filter



100kHz Distortion

SIGNAL LEVEL	R _L	2ND HARMONIC	3RD HARMONIC
1VRMS	1M	-106dB	-103dB
2VRMS	1M	-105dB	-105dB
3.5VRMS	1M	-106dB	-104dB
1VRMS	2k	-103dB	-103dB
2VRMS	2k	-99dB	-103dB
3.5VRMS	2k	-96.5dB	-102dB

1468 TA05

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1167	Precision Instrumentation Amplifier	Single Resistor Gain Set, 0.04% Max Gain Error, 10ppm Max Gain Nonlinearity
LTC1595/LTC1596	16-Bit Serial Multiplying I _{OUT} DACs	±1LSB Max INL/DNL, Low Glitch, DAC8043 16-Bit Upgrade
LTC1597	16-Bit Parallel Multiplying I _{OUT} DAC	±1LSB Max INL/DNL, Low Glitch, On-Chip Bipolar Resistors
LTC1604	16-Bit, 333ksps Sampling ADC	±2.5V Input, SINAD = 90dB, THD = -100dB
LTC1605	Single 5V, 16-Bit, 100ksps Sampling ADC	Low Power, ±10V Inputs, Parallel/Byte Interface
LT1469	Dual 90MHz 16-Bit Accurate Op Amp	Dual Version of LT1468
LT1800	80MHz, 25V/μs Low Power Rail-to-Rail Precision Op Amp	V _S ≤ ±5V, I _{CC} = 1.6mA, V _{OS} ≤ 350μV
LT6220	60MHz, 20V/μs Low Power Rail-to-Rail Precision Op Amp	V _S ≤ ±5V, I _{CC} = 0.9mA, V _{OS} ≤ 350μV
LT1722	200MHz, 70V/μs Low Noise Precision Op Amp	V _S ≤ ±5V, e _n = 3.8nV/√Hz, -85dBc at 1MHz
LTC6244HV	Dual 50MHz, Low Noise, Precision CMOS Op Amp	V _S ≤ ±5V, V _{OS} ≤ 100μV, I _B ≤ 75pA