

LT1431

ABSOLUTE MAXIMUM RATINGS (Note 1)

V^+ , $V_{\text{COLLECTOR}}$	36V
V_{COMP} , R_{TOP} , R_{MID} , V_{REF}	6V
GND-F to GND-S	0.7V
Ambient Temperature Range	
LT1431M, LT1431MP	-55°C to 125°C
LT1431I.....	-40°C to 85°C
LT1431C.....	0°C TO 70°C

Junction Temperature Range	
LT1431M, LT1431MP	-55°C to 150°C
LT1431I.....	-40°C to 100°C
LT1431C.....	0°C to 100°C
Storage Temperature Range	
-65°C to 150°C	
Lead Temperature (Soldering, 10 sec).....	
300°C	

PIN CONFIGURATION

TOP VIEW J8 PACKAGE 8-LEAD CERDIP $T_{\text{JMAX}} = 150^{\circ}\text{C}$, $\theta_{\text{JA}} = 100^{\circ}\text{C/W}$	TOP VIEW N8 PACKAGE 8-LEAD PLASTIC DIP $T_{\text{JMAX}} = 100^{\circ}\text{C}$, $\theta_{\text{JA}} = 130^{\circ}\text{C/W}$
TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SO $T_{\text{JMAX}} = 100^{\circ}\text{C}$, $\theta_{\text{JA}} = 170^{\circ}\text{C/W}$	BOTTOM VIEW Z PACKAGE 3-LEAD TO-92 PLASTIC $T_{\text{JMAX}} = 100^{\circ}\text{C}$, $\theta_{\text{JA}} = 150^{\circ}\text{C/W}$

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1431CN8#PBF	LT1431CN8#TRPBF	LT1431 CN8	8-Lead Plastic DIP	0°C to 70°C
LT1431IN8#PBF	LT1431IN8#TRPBF	LT1431 IN8	8-Lead Plastic DIP	-40°C to 85°C
LT1431CS8#PBF	LT1431CS8#TRPBF	LT1431	8-Lead Plastic SO	0°C to 70°C
LT1431IS8#PBF	LT1431IS8#TRPBF	LT1431I	8-Lead Plastic SO	-40°C to 85°C
LT1431MPS8#PBF	LT1431MPS8#TRPBF	LT1431	8-Lead Plastic SO	-55°C to 125°C
LT1431MJ8#PBF	LT1431MJ8#TRPBF	LT1431 MJ8	8-Lead CERDIP	-55°C to 125°C
LT1431CZ#PBF	LT1431CZ#TRPBF	LT1431 CZ	3-Lead TO-92 Plastic	0°C to 70°C
LT1431IZ#PBF	LT1431IZ#TRPBF	LT1431 IZ	3-Lead TO-92 Plastic	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $I_K = 10\text{mA}$ unless otherwise specified (Note 2)

SYMBOL	PARAMETER	CONDITIONS		LT1431I, LT1431M			LT1431C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{REF}	Reference Voltage	$V_{KA} = 5\text{V}$, $I_K = 2\text{mA}$, (Note 3)	●	2.490 2.465	2.500	2.510 2.535	2.490 2.480	2.500	2.510 2.520	V V
$\Delta V_{REF}/\Delta T$	Reference Drift	$V_{KA} = 5\text{V}$, $I_K = 2\text{mA}$	●	50			30			ppm/ $^\circ\text{C}$
$\Delta V_{REF}/\Delta V_{KA}$	Voltage Ratio, Reference to Cathode (Open-Loop Gain)	$I_K = 2\text{mA}$, $V_{KA} = 3\text{V}$ to 36V	●	0.2		0.5	0.2		0.5	mV/V
$ I_{REF} $	Reference Input Current	$V_{KA} = 5\text{V}$, $T_A = 25^\circ\text{C}$	●	0.2		1.0 1.5	0.2		1.0 1.2	μA μA
I_{MIN}	Minimum Operating Current	$V_{KA} = V_{REF}$ to 36V		0.6		1.0	0.6		1.0	mA
$ I_{OFF} $	Off-State Cathode Current	$V_{KA} = 36\text{V}$, $V_{REF} = 0\text{V}$	●			1 15			1 2	μA μA
$ I_{LEAK} $	Off-State Collector Leakage Current	$V_{COLL} = 36\text{V}$, $V^+ = 5\text{V}$, $V_{REF} = 2.4\text{V}$	●			1 5			1 2	μA μA
$ Z_{KA} $	Dynamic Impedance	$V_{KA} = V_{REF}$, $I_K = 1\text{mA}$ to 100mA , $f \leq 1\text{kHz}$				0.2			0.2	Ω
I_{LIM}	Collector Current Limit	$V_{KA} = V_{REF} + 50\text{mV}$	●	80		360	100		260	mA
	5V Reference Output	Internal Divider Used, $I_K = 2\text{mA}$		4.950	5.000	5.050	4.950	5.000	5.050	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

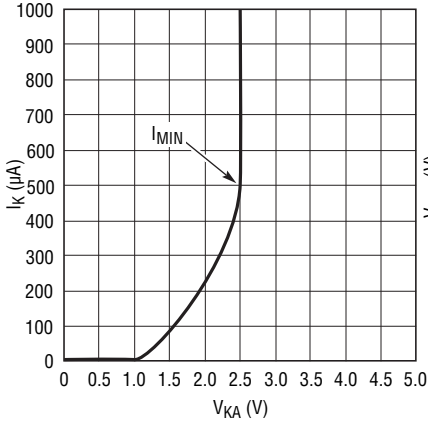
Note 2: V_{KA} is the cathode voltage of the LT1431CZ/IZ and corresponds to V^+ of the LT1431CN8/IN8/CS8/IS8. I_K is the cathode current of the

LT1431CZ/IZ and corresponds to $I(V^+) + I_{COLLECTOR}$ of the LT1431CN8/IN8/CS8/IS8.

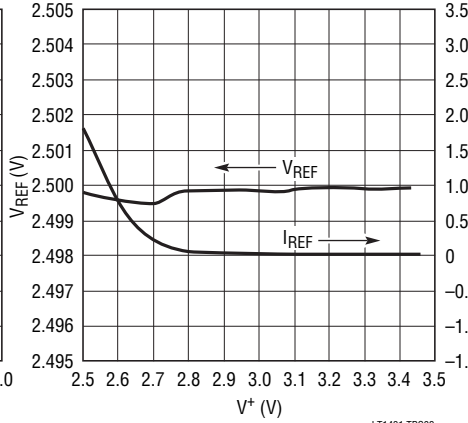
Note 3: The LT1431 has bias current cancellation which is effective only for $V_{KA} \geq 3\text{V}$. A slight ($\approx 2\text{mV}$) shift in reference voltage occurs when V_{KA} drops below 3V . For this reason, these tests are not performed at $V_{KA} = V_{REF}$.

TYPICAL PERFORMANCE CHARACTERISTICS

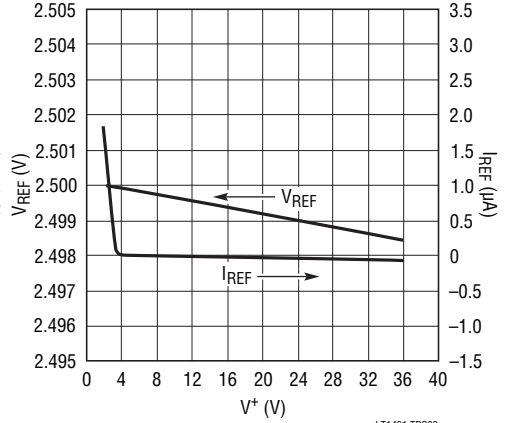
2.5V Reference I_K vs V_{KA}



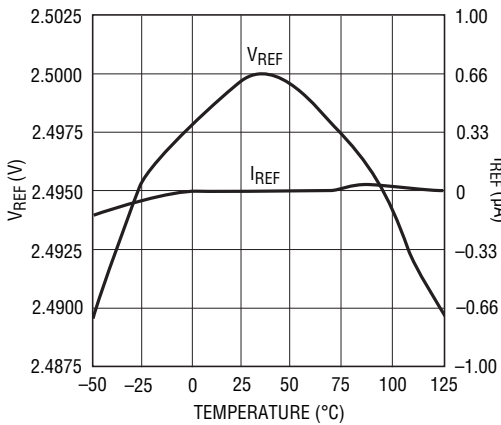
V_{REF} and I_{REF} vs V^+



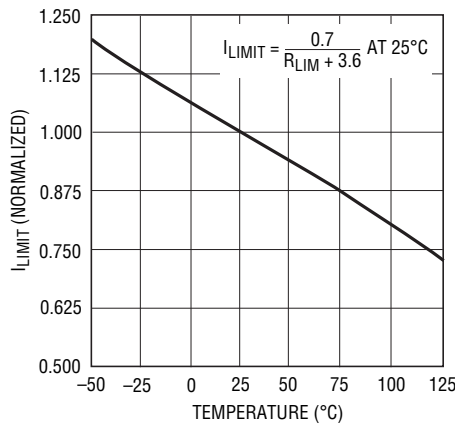
V_{REF} and I_{REF} vs V^+



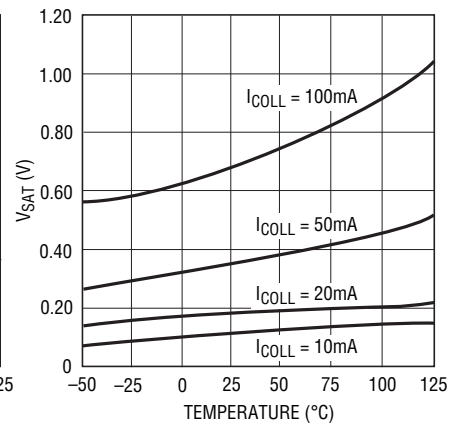
V_{REF} and I_{REF} vs Temperature



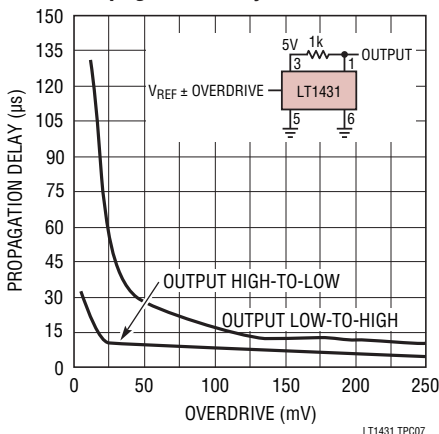
I_{LIMIT} vs Temperature with External Resistor



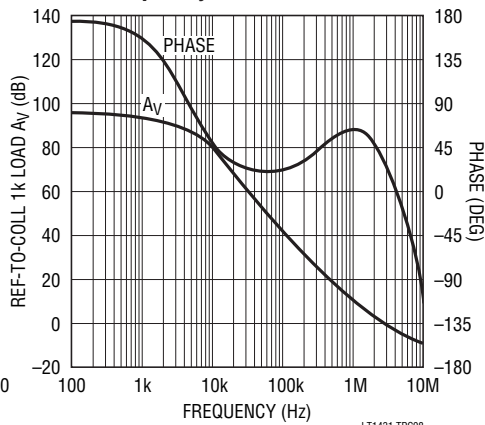
COLLECTOR V_{SAT} vs Temperature vs Current



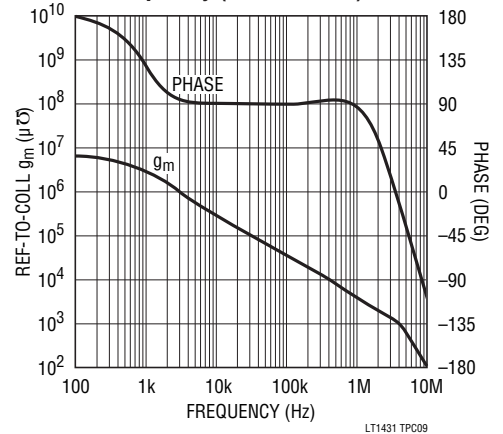
Propagation Delay vs Overdrive



Voltage Gain and Phase vs Frequency

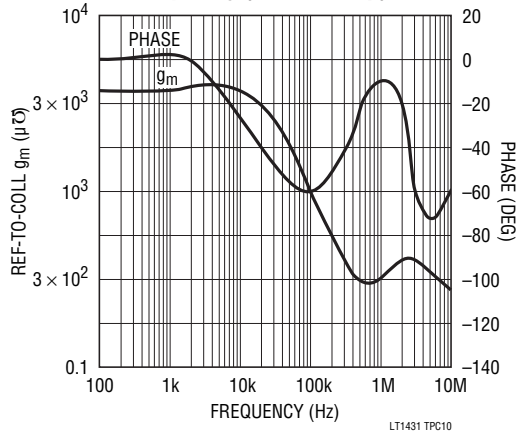


Transconductance and Phase vs Frequency (REF to COLL)

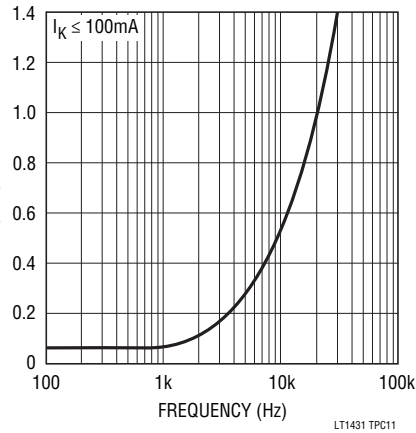


TYPICAL PERFORMANCE CHARACTERISTICS

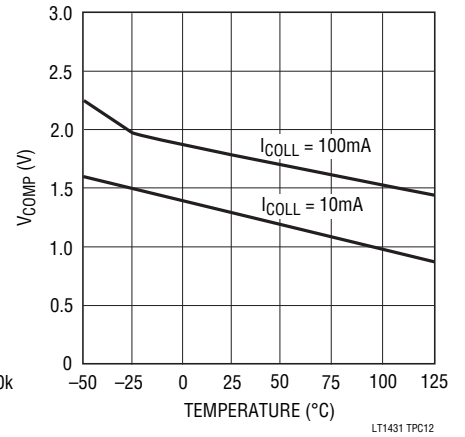
Transconductance and Phase vs Frequency (Ref to Comp)



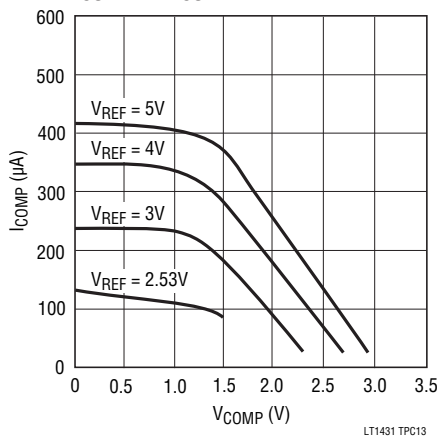
Dynamic Impedance vs Frequency



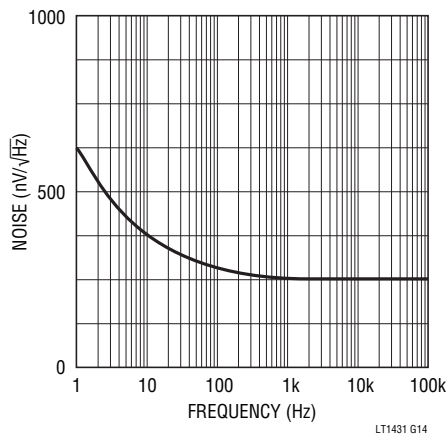
V_{COMP} vs Temperature vs I_{COLL}



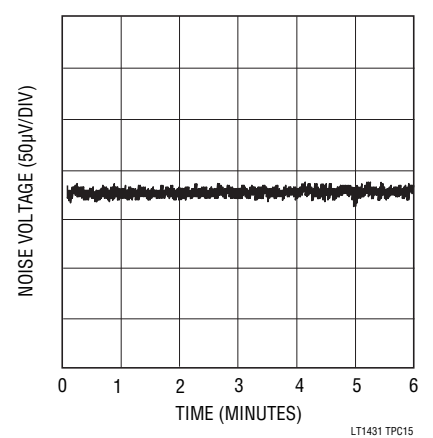
I_{COMP} vs V_{COMP} vs V_{REF}



Noise vs Frequency



0.1Hz to 10Hz Noise



PIN FUNCTIONS

COLL (Pin 1): Open collector of the output transistor. The maximum pin voltage is 36V. The saturation voltage at 100mA is approximately 1V.

COMP (Pin 2): Base of the driver for the output transistor. This pin allows additional compensation for complex feedback systems and shutdown of the regulator. It must be left open if unused.

V⁺ (Pin 3): Bias voltage for the entire shunt regulator. The maximum input voltage is 36V and the minimum to operate is equal to V_{REF} (2.5V). The quiescent current is typically 0.6mA.

R_{TOP} (Pin 4): Top of the on-chip 5k-5k resistive divider that guarantees 1% accuracy of operation as a 5V shunt regulator with no external trim. The pin is tied to COLL for self-contained 5V operation. It may be left open if unused. See note on parasitic diodes below.

GND-S (Pin 5): Ground reference for the on-chip resistive divider and shunt regulator circuitry except for the output transistor. This pin allows external current limit of the output transistor with one resistor between GND-F (force) and GND-S (sense).

GND-F (Pin 6): Emitter of the output transistor and substrate connection for the die.

R_{MID} (Pin 7): Middle of the on-chip resistive divider string between R_{TOP} and GND-S. The pin is tied to REF for self-contained 5V operation. It may be left open if unused.

REF (Pin 8): Control pin of the shunt regulator with a 2.5V threshold. If V⁺ > 3V, input bias current cancellation reduces I_B to 0.2μA typical.

COMP, R_{TOP}, R_{MID}, and REF have static discharge protection circuits that must not be activated on a continuous basis. Therefore, the absolute maximum DC voltage on these pins is 6V, well beyond the normal operating conditions.

As with all bipolar ICs, the LT1431 contains parasitic diodes which must not be forward biased or else anomalous behavior will result. Pin conditions to be avoided are R_{TOP} below R_{MID} in voltage and any pin below GND-F in voltage (except for GND-S).

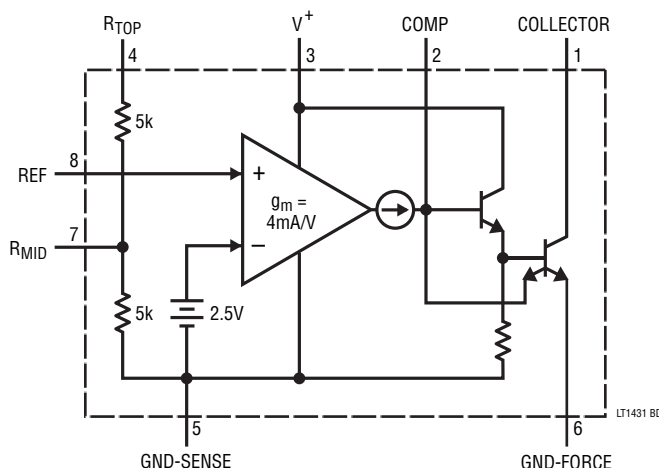
The following pin definitions apply to the Z package.

CATHODE: Corresponds to COLL and V⁺ tied together.

ANODE: Corresponds to GND-S and GND-F tied together.

REF: Corresponds to REF.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Frequency Compensation

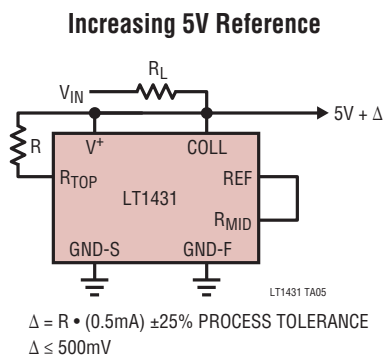
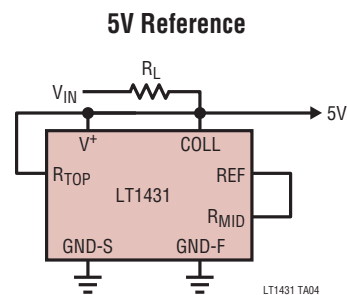
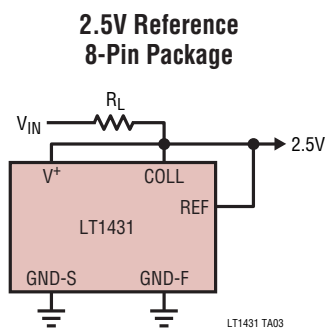
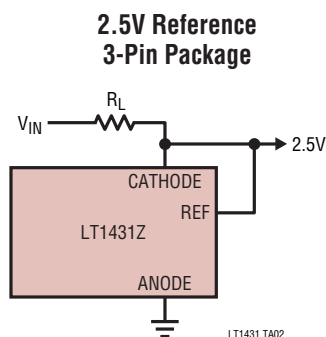
As a shunt regulator, the LT1431 is stable for all capacitive loads on the COLL pin. Capacitive loading between 0.01 μ F and 18 μ F causes reduced phase margin with some ringing under transient conditions. Output capacitors should not be used arbitrarily because output noise is not necessarily reduced.

Excess capacitance on the REF pin can introduce enough phase shift to induce oscillation when configured as a reference >2.5V. This can be compensated with capacitance between COLL and REF (phase lead). More complicated feedback loops may require shaping of the frequency

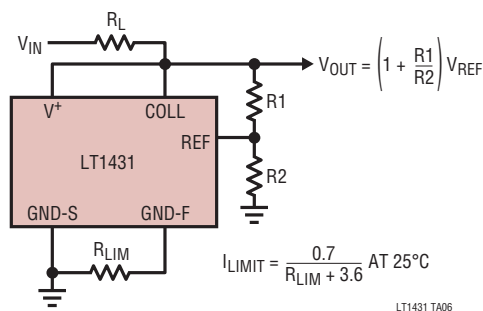
response of the LT1431 with dominant pole or pole-zero compensation. This can be accomplished with a capacitor or series resistor and capacitor between COLL and COMP.

The compensation schemes mentioned above use voltage feedback to stabilize the circuits. There must be voltage gain at the COLL pin for them to be effective, so the COLL pin must see a reasonable AC impedance. Capacitive loading of the COLL pin reduces the AC impedance, voltage gain, and frequency response, thereby decreasing the effectiveness of the compensation schemes, but also decreasing their necessity.

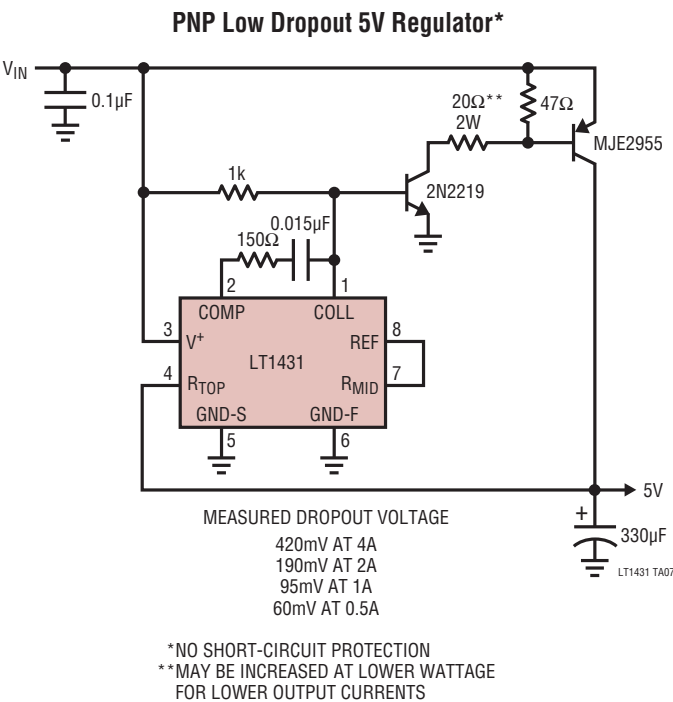
TYPICAL APPLICATIONS



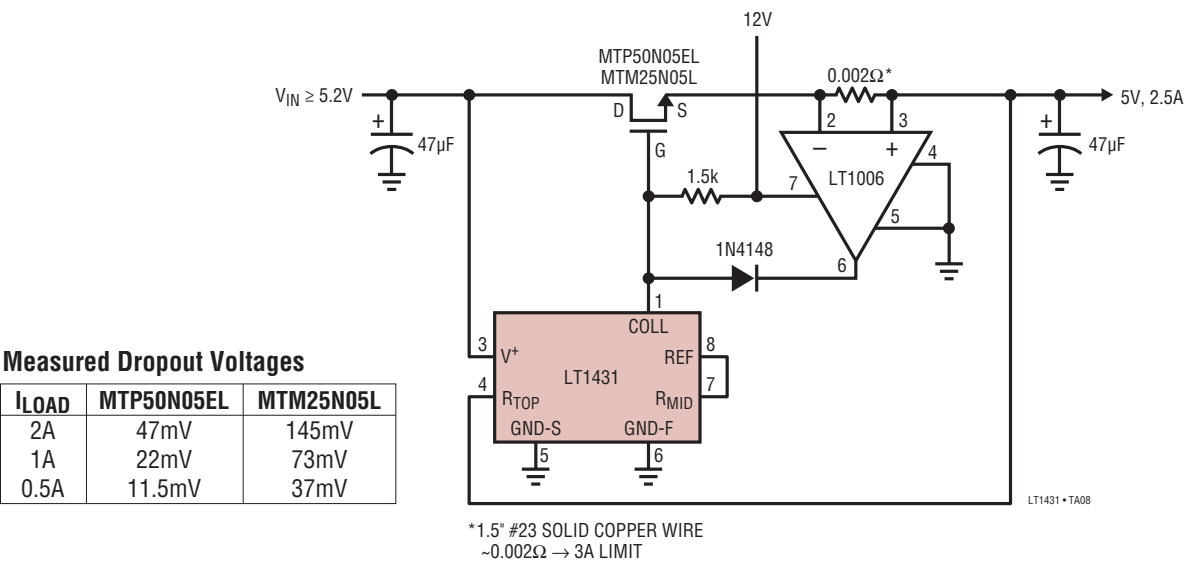
Programmable Reference with Adjustable Current Limit



TYPICAL APPLICATIONS

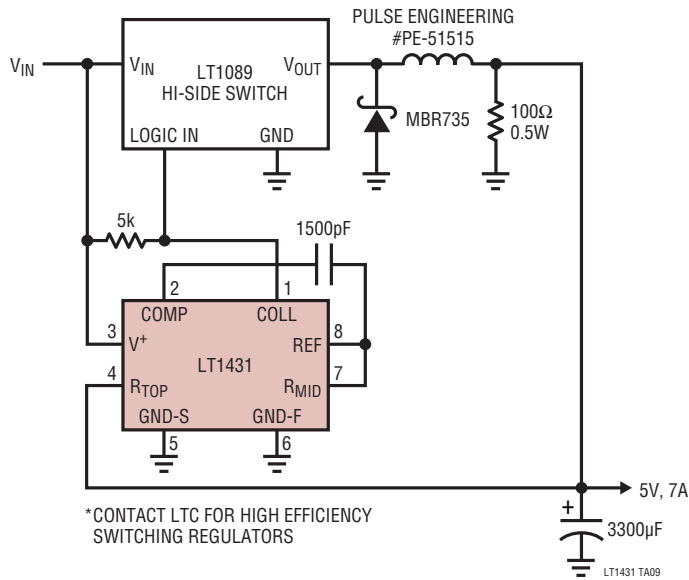


FET Low Dropout 5V Regulator with Current Limit

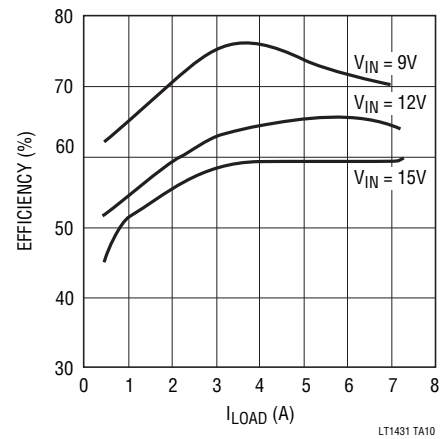


TYPICAL APPLICATIONS

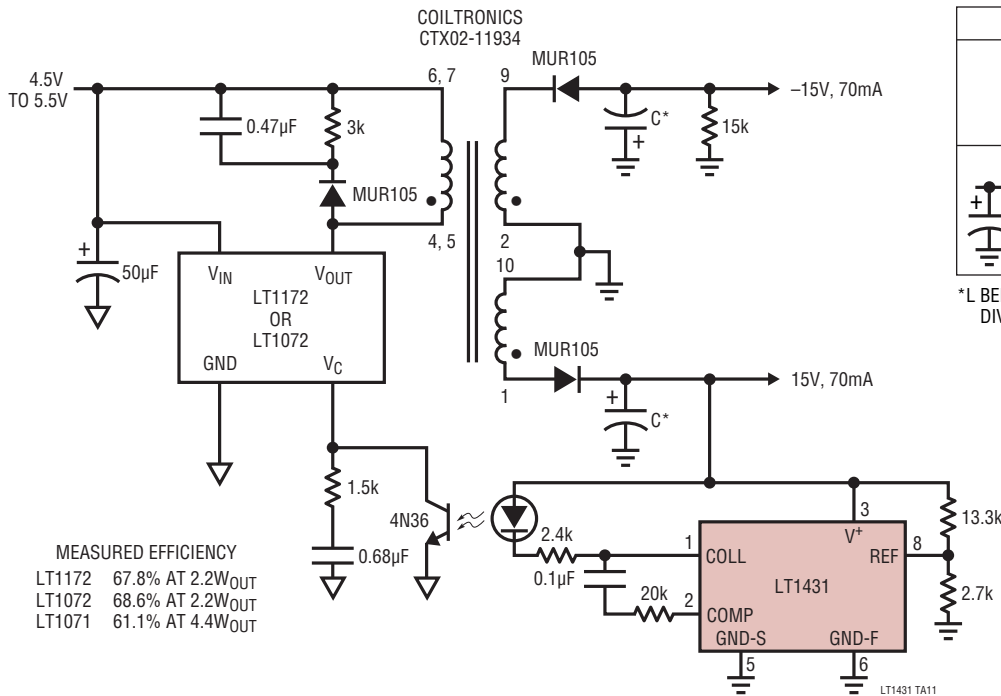
12V to 5V Buck Converter with Foldback Current Limit*



Buck Converter Efficiency



Isolated 5V to $\pm 15V$ Flyback Converter



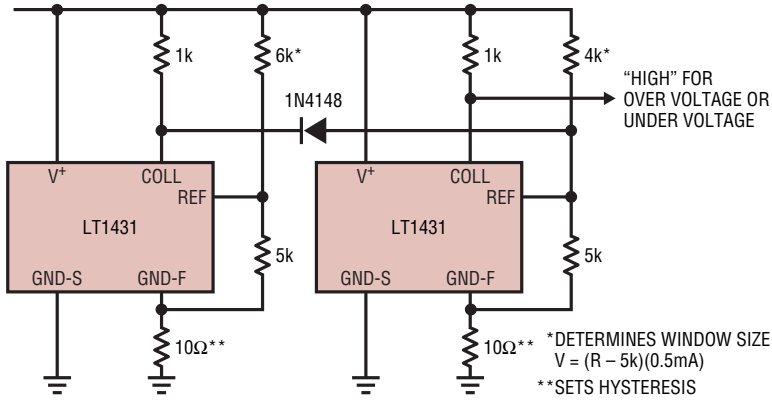
Fully Loaded Output Ripple vs Filtering

C*	LT1172	LT1072
	210μF	30mV _{p-p}
	100μF	6mV _{p-p}
	100μF	8mV _{p-p}

*L BELL INDUSTRIES J.W. MILLER
DIVISION 9310-36 10μH, 450mA

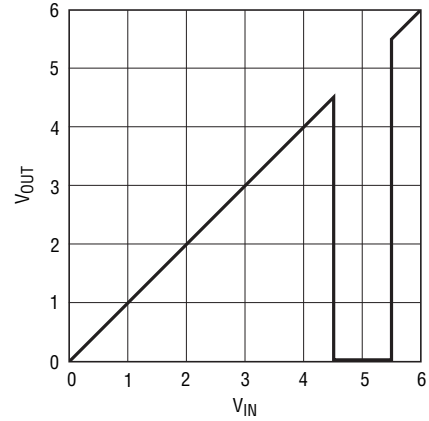
TYPICAL APPLICATIONS

5V Power Supply Monitor with $\pm 500\text{mV}$ Window and 50mV Hysteresis

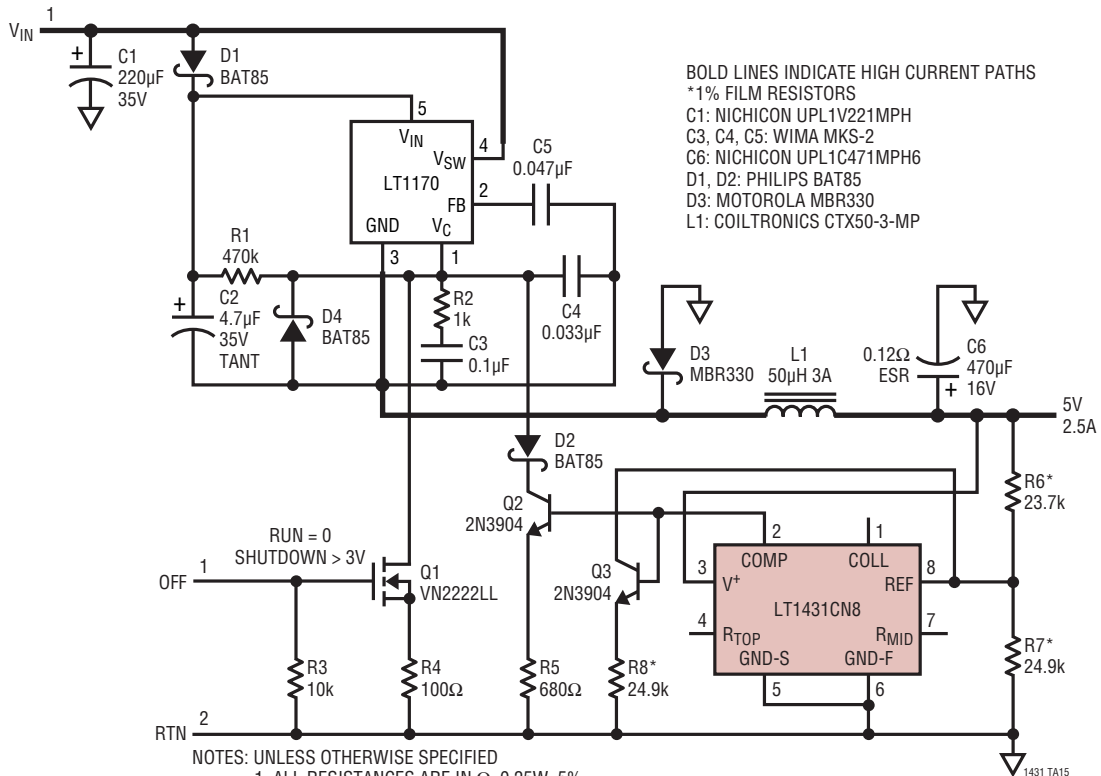


LT1431 TA13

Transfer Function

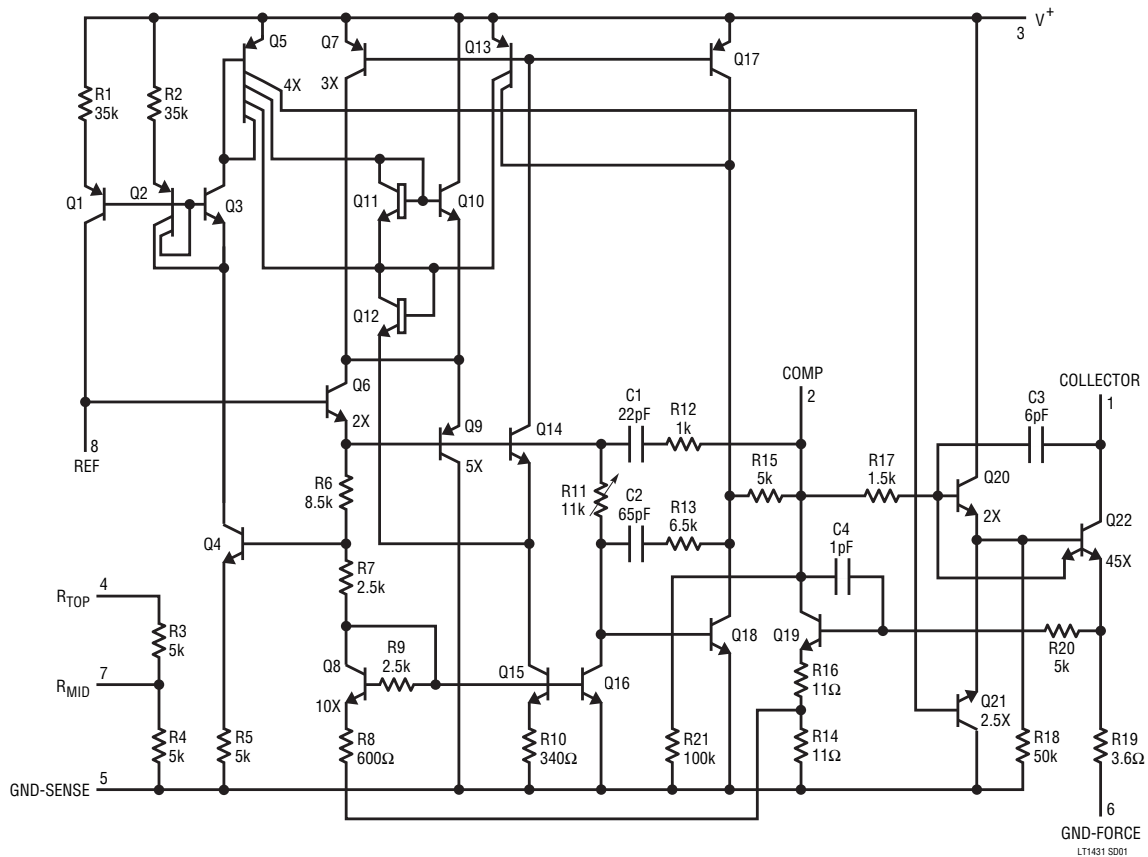


High Efficiency Buck Converter $E = 85\%$ to 89%



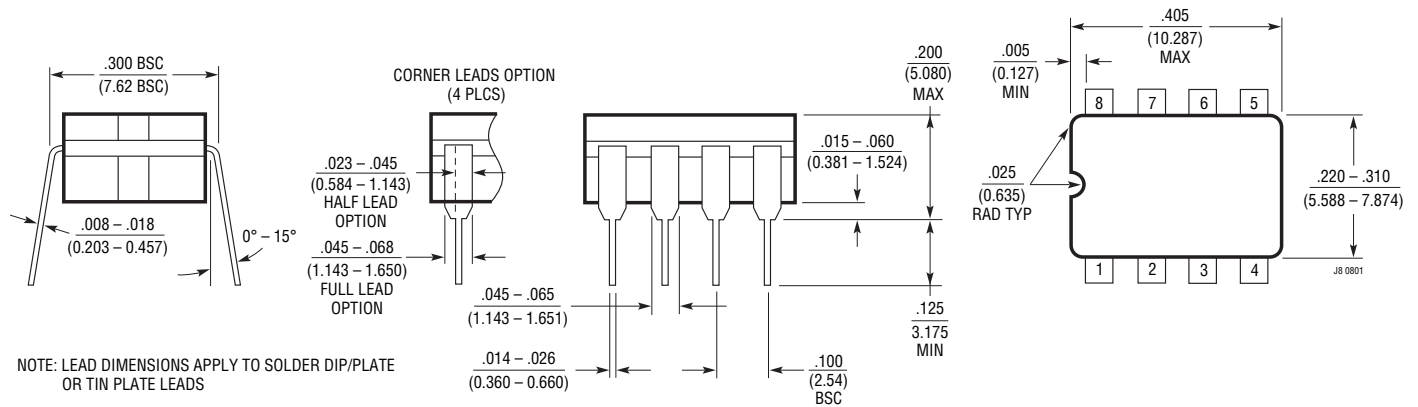
1431 TA15

SCHEMATIC DIAGRAM



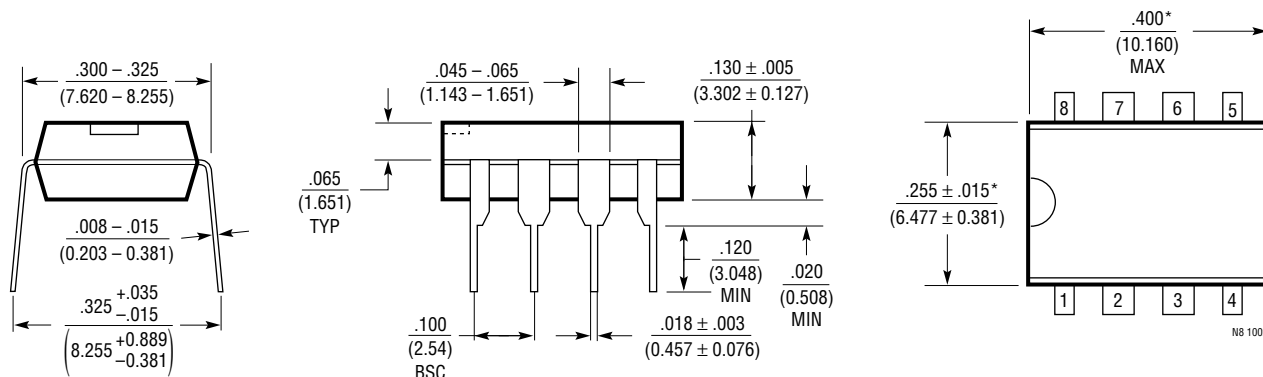
PACKAGE DESCRIPTION

J8 Package
8-Lead Cerdip (Narrow .300 Inch, Hermetic)
 (Reference LTC DWG # 05-08-1110)



PACKAGE DESCRIPTION

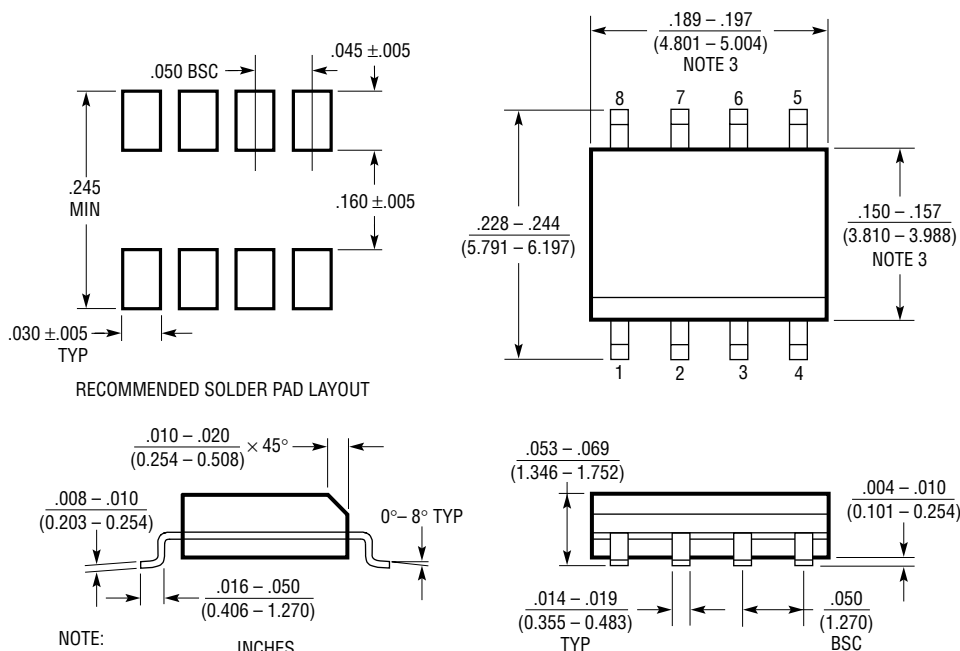
N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



NOTE:

1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$ *THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



NOTE:

1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

2. DRAWING NOT TO SCALE

3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

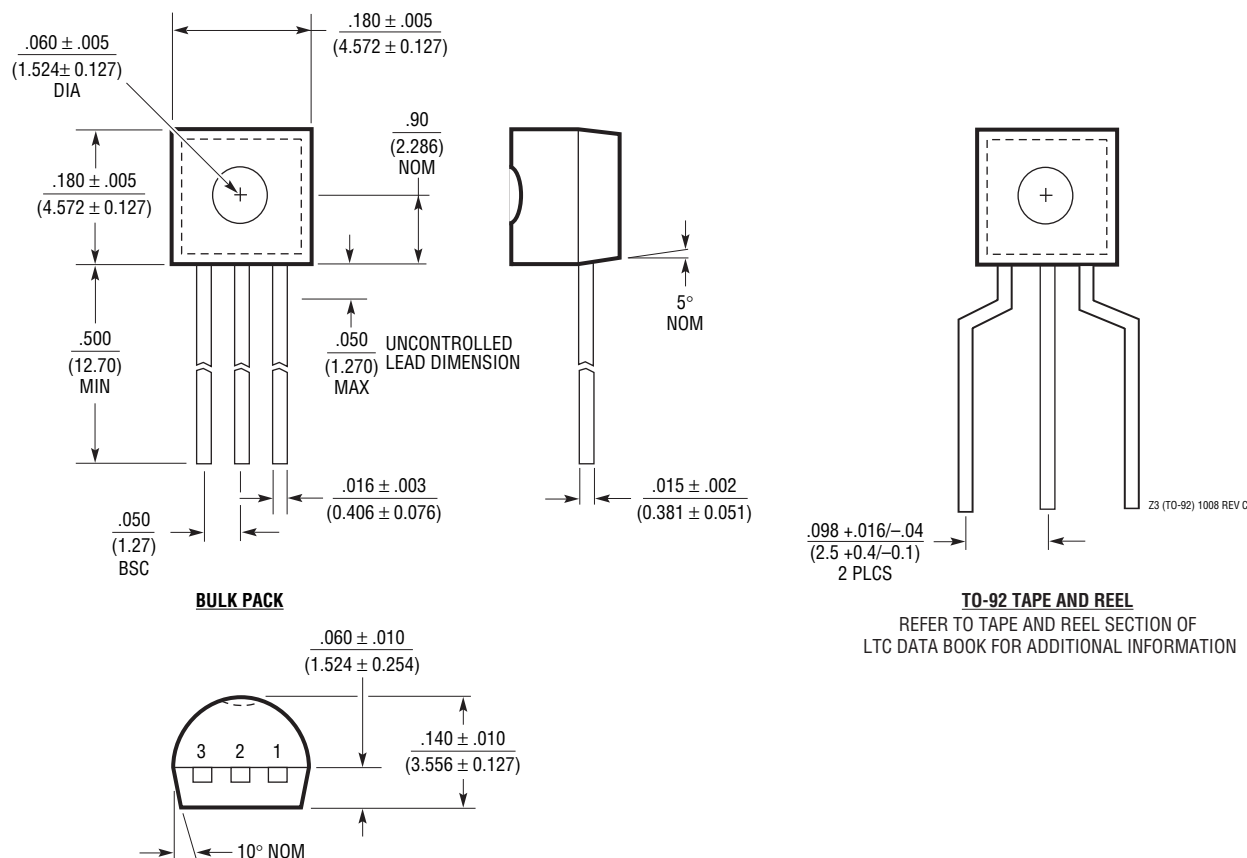
S08 0303

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	4/10	M-grade parts re-released. Obsolete package shading removed.	2, 11
E	7/11	Added LT1431MPS8 to data sheet. Changes reflected throughout.	1 to 14

PACKAGE DESCRIPTION

Z Package 3-Lead Plastic TO-92 (Similar to TO-226) (Reference LTC DWG # 05-08-1410 Rev C)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT4430	Secondary-Side Optocoupler Driver with Reference Voltage	Overshoot Control Prevents Output Overshoot during Start-Up and Short-Circuit Recovery
LT3757/LT3758	Boost, Flyback, SEPIC and Inverting Controller	2.9V/5.5V ≤ V _{IN} ≤ 40V/100V, 100kHz to 1MHz Fixed Frequency, 3mm × 3mm DFN-10 and MSOP-10E Packages
LTC3803/LTC3803-3/ LTC3803-5	Flyback DC/DC Controller with Fixed 200kHz or 300kHz Operating Frequency	V _{IN} and V _{OUT} Limited by External Components, 6-Pin ThinSOT™ Package
LTC3873/LTC3873-5	No R _{SENSE} Constant Frequency Flyback, Boost, SEPIC Controller	V _{IN} and V _{OUT} Limited Only by External Components, 8-Pin ThinSOT and 2mm × 3mm DFN-8 Packages
LTC3805/LTC3805-5	Adjustable Constant Frequency (70KHz to 700kHz) Frequency Flyback DC/DC Controller	V _{IN} and V _{OUT} Limited by External Components, MSOP-10E and 3mm × 3mm DFN-10 Packages
LT1952/LT1952-1	Isolated Synchronous Forward Controllers	Ideal for Medium Power 24V and 48V Input Applications
LTC3723-1/LTC3723-2	Synchronous Push-Pull and Full-Bridge Controllers	High Efficiency with On-Chip MOSFET Drivers
LTC3721-1/LTC3721-2	Non-Synchronous Push-Pull and Full-Bridge Controllers	Minimizes External Components, On-Chip MOSFET Drivers
LTC3722/LTC3722-2	Synchronous Isolated Full Bridge Controllers	Ideal for High Power 24V and 48V Input Applications