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- Equipped with a serial data input pin. Possible to switch with demodulation output automatically according to the state of the PLL circuit.
- The fs reception range of S/PDIF interface can be limited. LC89058W-E can be set to a no-signal input state if the reception range is exceeded.
- Supports I^2S data output that facilitates interfacing with DSP.

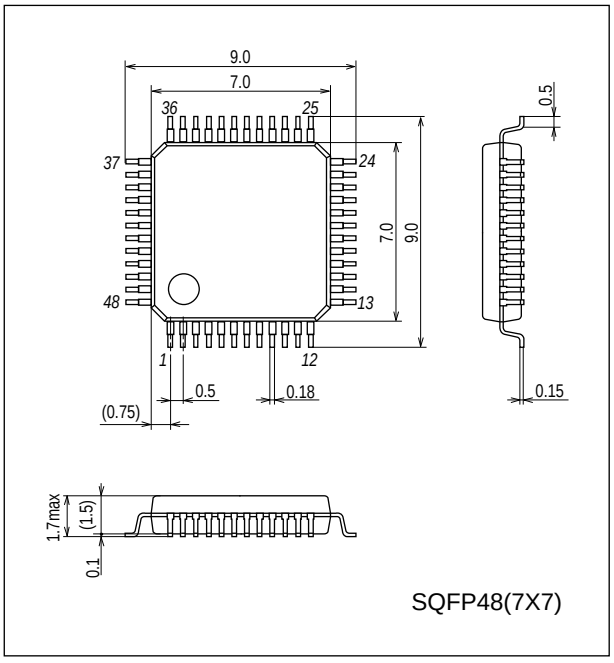
2.3 Other

- Supports Multi-channel transfer and reception, using master/slave function.
- Equipped with a 4bits general-purpose I/O pins. They can be used for interface with peripheral ICs.
- The general-purpose I/O pins can also serve as selector inputs. Possible to switch with HDMI and XM-radio signals.
- Generates a DTS-CD/LD detection flag on detection of a DTS synchronization signal.
- Outputs interrupt signal for microcontroller (interrupt source can be selected).
- Calculates sampling frequency of input signal and outputs it from the terminal or microcontroller interface.
- Outputs IEC61937 burst preamble Pc from microcontroller interface.
- Outputs IEC60958 bit 1 of channel status (non-PCM data delimiter bit).
- Outputs emphasis information of channel status.
- Can use up to four LC89058W-Es at the same time by setting the 2-bit chip address.
- Runs on a single 3.3V power supply (S/PDIF input and microcontroller interface support 5V TTL interface.)
- SQFP48 package

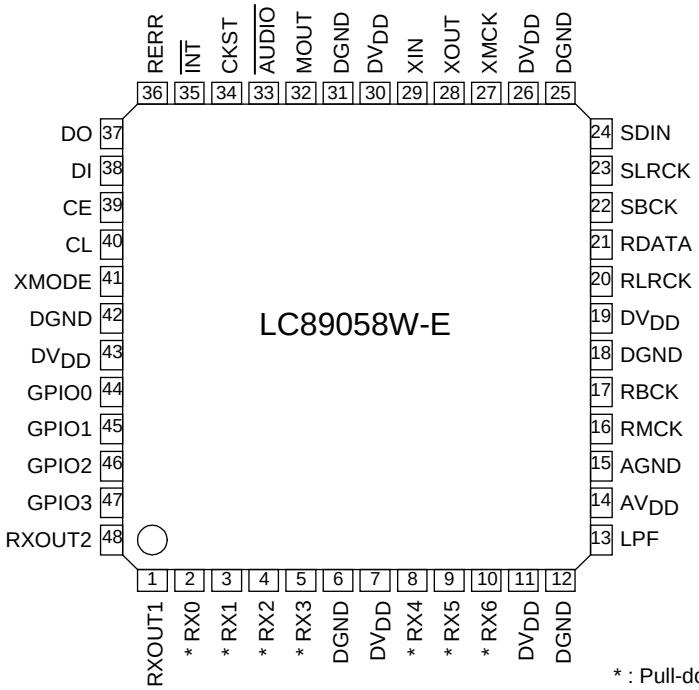
Package Dimensions

unit : mm (typ)

3163B



4. Pin Assignment



* : Pull-down resistor internal at no selection

Top view

5. Pin Functions

Table 5.1 Pin Functions

Pin No.	Name	I/O	Function
1	RXOUT1	O	RX0-6 input S/PDIF through output pin 1
2	RX0	I_5(pd)	5V withstand voltage TTL input level compatible S/PDIF input pin (connected to GND when RX1 is set)
3	RX1	I(pd)	Co-axial compatible S/PDIF input pin (supported demodulation sampling frequency of up to 96kHz)
4	RX2	I_5(pd)	5V withstand voltage TTL input level compatible S/PDIF input pin (connected to GND when RX1 is set)
5	RX3	I_5(pd)	5V withstand voltage TTL input level compatible S/PDIF input pin
6	DGND		Digital GND
7	DV_{DD}		Digital power supply (3.3V)
8	RX4	I_5(pd)	5V tolerable TTL input level compatible S/PDIF input pin
9	RX5	I_5(pd)	5V tolerable TTL input level compatible S/PDIF input pin
10	RX6	I_5(pd)	5V tolerable TTL input level compatible S/PDIF input pin
11	DV_{DD}		Digital power supply (3.3V)
12	DGND		Digital GND
13	LPF	O	PLL loop filter connection pin
14	AV_{DD}		Analog power supply (3.3V)
15	AGND		Analog GND
16	RMCK	O	R system clock output pin (VCO, 512fs, XIN)
17	RBCK	O/I	R system bit clock I/O pin (64fs)
18	DGND		Digital GND
19	DV_{DD}		Digital power supply (3.3V)
20	RLRCK	O/I	R system LR clock I/O pin (fs)
21	RDATA	O	Serial audio data output pin
22	SBCK	O	S system bit clock output pin (16fs, 32fs, 64fs, 128fs)
23	SLRCK	O	S system LR clock output pin (fs/4, fs/2, fs, 2fs)
24	SDIN	I_5	External serial audio data input pin

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Pin No.	Name	I/O	Function
25	DGND		Digital GND
26	DV_{DD}		Digital power supply (3.3V)
27	XMCK	O	Oscillation amplifier clock output pin
28	XOUT	O	Output pin connected to the resonator
29	XIN	I	External clock input pin, connected to the resonator (12.288MHz/24.576MHz)
30	DV_{DD}		Digital power supply
31	DGND		Digital GND
32	MOUT	I/O	Emphasis information || Input fs monitor output || Chip address setting input pin
33	$\overline{\text{AUDIO}}$	I/O	Channel status bit 1 output || Chip address setting input pin
34	CKST	I/O	Clock switching transition period signal output || Master/slave setting input pin
35	$\overline{\text{INT}}$	I/O	Microcontroller interrupt signal output || Pins44-48 I/O setting input pin
36	RERR	O	PLL lock error, data error flag output pin
37	DO	O	CCB microcontroller I/F, read data output pin (3-state)
38	DI	I_5	CCB microcontroller I/F, write data input pin
39	CE	I_5	CCB microcontroller I/F, chip enable input pin
40	CL	I_5	CCB microcontroller I/F, clock input pin
41	XMODE	I_5	System reset input pin
42	DGND		Digital GND
43	DV_{DD}		Digital power supply (3.3V)
44	GPIO0	O/I	General-purpose I/O pin || Selector input pin (output referred to RDATA pin)
45	GPIO1	O/I	General-purpose I/O pin || Selector input pin (output referred to RLRCK pin)
46	GPIO2	O/I	General-purpose I/O pin || Selector input pin (output referred to RBCK pin)
47	GPIO3	O/I	General-purpose I/O pin || Selector input pin (output referred to RMCK pin)
48	RXOUT2	O	RX0-6 input S/PDIF through output pin 2

* Input voltage: I= -0.3 to 3.6V, I_5 = -0.3 to 5.5V
* Output voltage: O= -0.3 to 3.6V
* Pins 2, 4, 5, 8, 9, 10, 24, 38, 39, 40, and 41 have an internal pull-down resistor (pd).
  Their level is fixed when they are unselected.
* Pins 32 and 33 are input pins for chip address setting when pin 41 is held at the low level.
* Pin 34 serves as the input pin for designating as the master or slave when pin 41 is held at the low level.
* Pin 35 serves as the input pin for configuring the I/O of pins 44 to 47 when pin 41 is held at the low level.
* The DV_{DD} and AV_{DD} pins must be held at the same level and turned on and off at the same timing to preclude Latch-up conditions.

6. Block Diagram

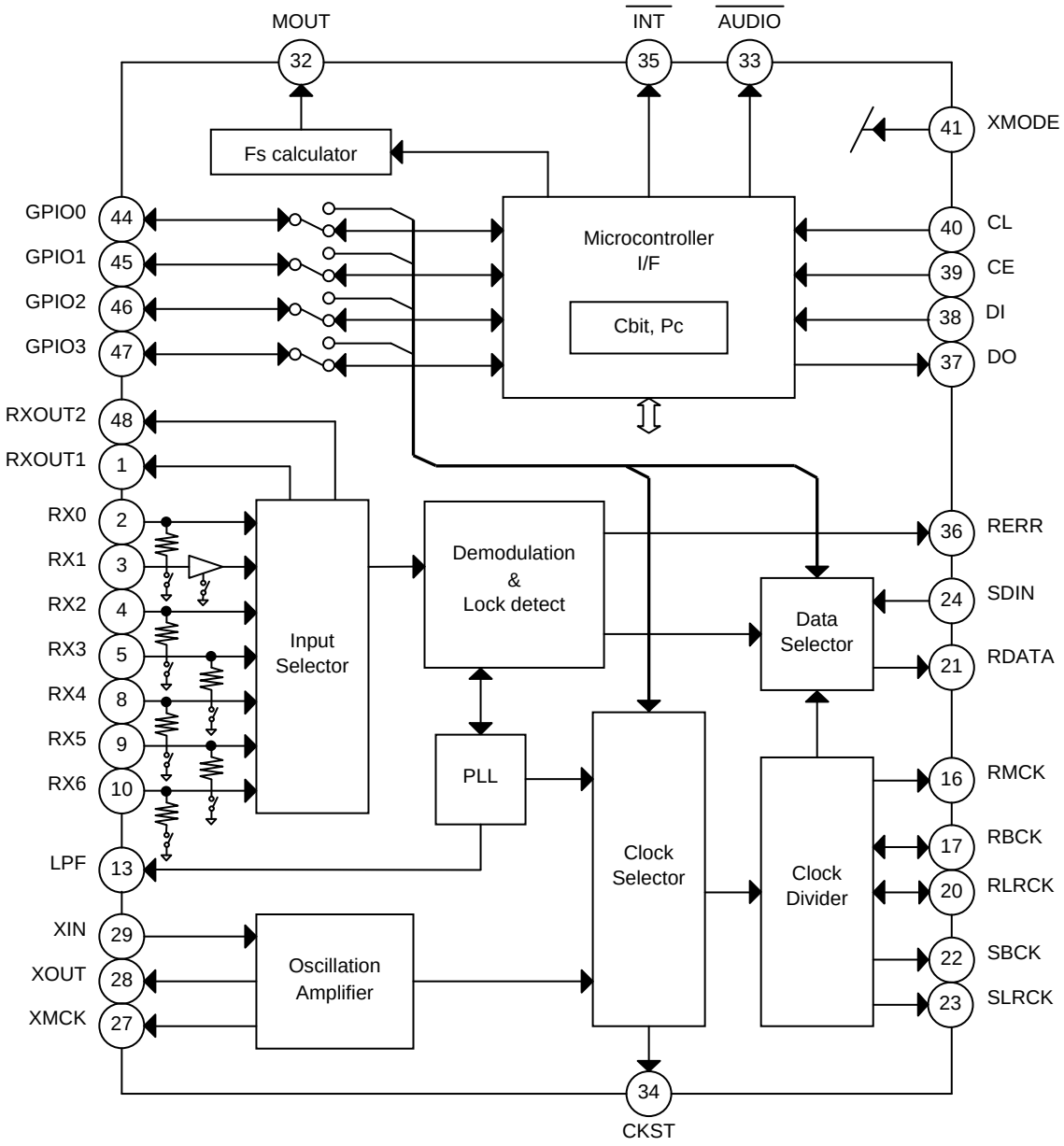


Figure 6.1 LC89058W-E Block Diagram

7 Common and Different Points between LC89057W-VF4A-E and LC89058W-E

7.1 Common Features

Table 7.1: Common of LC89057W-VF4A-E and LC89058W-E functions (Hardware/Software Compatibility)

Item	LC89057W-VF4A-E	LC89058W-E
Package	SQFP48(9x9)	←
Supply voltage	3.3V single source	←
DIR reception range	32kHz to 192kHz	←
Oscillation amplifier input frequency	12.288MHz/24.576MHz	←
2-system-clock pin output	RMCK, RBCK, RLRCK, SBCK, SLRCK	← SBCK: 16fs, SLRCK: 1/4 output added
S/PDIF inputs	7 maximum (1 coaxial, 6 optical)	←
Serial data input	SDIN	←
Non-PCM flag output	$\overline{\text{AUDIO}}$	←
Emphasis information output	EMPHA (consumer and professional)	← MOUT (consumer only)
DTS-CD/LD detection function	14-bit format detection supported	←
General-purpose I/O	4 bits	←
Chip address setting	4 addresses maximum (master/salve supported)	←
Mode setting external resistor	4 resistors used	←
Microcontroller interface	CCB (Our company proprietary IF)	← DI input regulations has.
Register configuration	4 command address bits, 8 data bits	←

7.2 Removed Functions

Table 7.2: Differences between LC89057W-VF4A-E and LC89058W-E (Removed Functions)

Item	LC89057W-VF4A-E	LC89058W-E
Function	Modulation and demodulation	Modulation removed (demodulation only)
S/PDIF unlock path switching	Yes	Removed
External clock synchronization mode	Yes	Removed
R and S system clock synchronization	Asynchronous system	Synchronization clock (SELMTD, RCKSEL removed)
Data output format	16, 20, 24 bits/left-justified/right-justified MSB, I^2S	Right-justified removed (left-justified MSB, I^2S only)
C, V, U pin output	Yes	Removed
Input fs computed output	16kHz to 192kHz	32kHz to 192kHz (fs < 32kHz, removed)
Microcontroller interrupt signal	Yes (Low pulse, Low level output)	Pulse output mode removed (level output only)

7.3 Added or Modified Functions

Table 7.3: Differences between LC89057W-VF4A-E and LC89058W-E (Added or Modified Functions)

Item	LC89057W-VF4A-E	LC89058W-E	Page
Oscillation amplifier initial setting	Suspended while PLL is locked	Permanent operation	19
PLL clock output	256fs or 512fs	512fs	20-26
Master clock output	Multiple of input fs is output	Multiple of input fs on each band is output	22
Clock output when XIN source	No limitation	RBCK and SBCK must 1/2 or less of RMCK	23
Clock switching	Clock count is preserved (to maintain continuity)	Switched during the CKST pulse output	25
RMCK and CKST polarity	Polarity cannot be switched	Polarity can be switched	23, 25
S/PDIF reception limitation	Reflected only to error flag.	Reflected to both error flag and clock output	26
S/PDIF input detection range	32kHz to 96kHz (XIN=24.57M/12.28MHz)	32kHz to 192kHz (XIN=24.576MHz only)	27
Input fs value monitor output	Microcontroller interface output only	Microcontroller interface and pin outputs	32
General-purpose I/O input pin	No timing control	Polling supported (with interrupt)	36
General-purpose I/O input/output pin	Parallel I/O function only	Internal selector input also supported.	37

7.4 Differences in Microcontroller Registers

7.4.1 Differences in write commands

Table 7.4: LC89057W-VF4A-E Write Register Map

Addr	Setting Item	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	All system	TESTM	0	TXOPR	RXOPR	INTOPF	0	DOEN	SYSRST
1	Demodulator system	PBSEL1	PBSEL0	FSLIM1	FSLIM0	RXMON	AOSEL	VOSEL	UOSEL
2	Master clock	AMPOPR1	AMPOPR0	EXSYNC	PLLOPR	XMSEL1	XMSEL0	XINSEL	PLLSEL
3	R system output clock	XRLRCK1	XRLRCK0	XRBCK1	XRBCK0	XRSEL1	XRSEL0	PRSEL1	PRSEL0
4	S system output clock	XSLRCK1	XSLRCK0	XSBCK1	XSBCK0	PSLRCK1	PSLRCK0	PSBCK1	PSBCK0
5	Source switching	0	RDTMUT	RDTSTA	RDTSEL	0	RCKSEL	OCKSEL	SELMTD
6	Data input/output	RXOFF	ROSEL2	ROSEL1	ROSEL0	ULSEL	RISEL2	RISEL1	RISEL0
7	Output format	SLRCKP	SBCKP	RLRCKP	RBCKP	0	OFSEL2	OFSEL1	OFSEL0
8	$\overline{\text{INT}}$ source selection	EMPF	SLIPO	PCRNW	UNPCM	CSRNW	FSCHG	INDET	ERROR
9	RERR conditions	ERWT1	ERWT0	FSERR	RESTA	XTWT1	XTWT0	REDER	RESEL
10	Modulation system	PI3	PI2	PI1	PI0	0	VMODE	VISEL	UISEL
11	Modulation data	TCKSEL	0	TXMOD1	TXMOD0	TXMUT	TDTSEL	TXLRP	TXDFS
12	Test	0	0	0	0	0	0	0	0
13	Test	0	0	0	0	0	0	0	0
14	Test	0	0	0	0	0	0	0	0
15	Test	0	0	0	0	0	0	0	0

Table 7.5: LC89058W-E Write Register Map

Addr	Setting Item	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	System setting 1	TESTM	0	“0”	“0”	“0”	0	DOEN	SYSRST
1	System setting 2	“0”	“0”	FSLIM1	FSLIM0	RXMON	AOSEL	“0”	MOSEL
2	Master clock	AMPOPR1	AMPOPR0	“0”	PLLOPR	XMSEL1	XMSEL0	XINSEL	“0”
3	R system output clock	XRLRCK1	XRLRCK0	XRBCK1	XRBCK0	XRSEL1	XRSEL0	PRSEL1	PRSEL0
4	S system output clock	XSLRCK1	XSLRCK0	XSBCK1	XSBCK0	PSLRCK1	PSLRCK0	PSBCK1	PSBCK0
5	Source switching	0	RDTMUT	RDTSTA	RDTSEL	0	0	OCKSEL	0
6	Data input/output 1	“0”	ROSEL2	ROSEL1	ROSEL0	“0”	RISEL2	RISEL1	RISEL0
7	Output format	SLRCKP	SBCKP	RLRCKP	RBCKP	0	“0”	“0”	OFDSEL
8	$\overline{\text{INT}}$ source selection	EMPF	GPIO	PCRNW	UNPCM	CSRNW	FSCHG	INDET	ERROR
9	RERR condition setting	ERWT1	ERWT0	FSERR	RESTA	“0”	“0”	REDER	RESEL
10	General-purpose I/O	PI3	PI2	PI1	PI0	0	“0”	“0”	“0”
11	Test	“0”	0	“0”	“0”	“0”	“0”	“0”	“0”
12	System setting 3	0	0	CKSTP	RMCKP	0	PLLDV1	PLLDV0	PLLACC
13	Data input/output 2	0	RXSEL2	RXSEL1	RXSEL0	EDTMUT	EMCKP	EXTSEL	GPIOS
14	Other output settings	FSSEL1	FSSEL0	0	0	PTOXW1	PTOXW0	0	0
15	Test	0	0	0	0	0	0	0	0

- Except MOSEL, PRSEL [1:0], OFDSEL, GPIO, SELMTD and RCKSEL, the command address of any inadvertently specified commands that are removed from the LC89057W-VF4A-E is assumed to be “0” and ignored.
  The new commands added to the LC89058W-E are allocated to command addresses 12, 13, and 14.

7.4.2 Differences in read commands

Table 7.6: Changes in the Register Function between LC89057W-VF4A-E and LC89058W-E

CCB Address	LC89057W-VF4A-E	LC89058W-E
0xE9	DIT channel status write register	Removed

Table 7.7: Differences in Read Registers between the LC89057W-VF4A-E and LC89058W-E

Register	LC89057W-VF4A-E		LC89058W-E	
	0xEA	0xEB	0xEA	0xEB
DO0	RXDET0	PO0	RXDET0	PO0
DO1	RXDET1	PO1	RXDET1	PO1
DO2	RXDET2	PO2	RXDET2	PO2
DO3	RXDET3	PO3	RXDET3	PO3
DO4	RXDET4	FSC0	RXDET4	FSC0
DO5	RXDET5	FSC1	RXDET5	FSC1
DO6	RXDET6	FSC2	RXDET6	FSC2
DO7	RXDET7	FSC3	0	FSC3
DO8	OERROR	FSDAT0	OERROR	-
DO9	OINDET	FSDAT1	OINDET	-
DO10	OFSCHG	FSDAT2	OFSCHG	-
DO11	OCSRNW	FSDAT3	OCSRNW	-
DO12	OUNPCM	FSDAT4	OUNPCM	-
DO13	OPCRNW	FSDAT5	OPCRNW	-
DO14	OSLIPO	FSDAT6	OGPIO	-
DO15	OEMPF	FSDAT7	OEMPF	-
DO16	CSBIT1	-	CSBIT1	-
DO17	IEC1937	-	IEC1937	-
DO18	DTS51	-	DTS51	-
DO19	DTSES	-	DTSES	-
DO20	F0512	-	0	-
DO21	F1024	-	0	-
DO22	F2048	-	0	-
DO23	F4096	-	0	-

- The CCB addresses 0xEC and 0xED remain the same for both the LC89057W-VF4A-E and LC89058W-E.

7.5 Points to Notice about Replacing

- When replacing the LC89057W-VF4A-E with the LC89058W-E, it may be necessary to review the circuit pattern design of the printed circuit board in advance depending how the device is used. Particular attention should be directed to pins 44 to 48 whose I/O functionality can be set according to the $\overline{\text{INT}}$ pin setting. This section contains the notes and cautions to be observed when replacing the LC89057W-VF4A-E with the LC89058W-E. For details of the $\overline{\text{INT}}$ pin, see Chapter 9, Initial System Settings and Chapter 10, Description of Demodulation Function.
- Refer to the specifications of LC89057W-VF4A-E when replacing LC89058W-E with LC89057W-VF4A-E.

Table 7.8: Differences between LC89057W-VF4A-E and LC89058W-E (Pins 44 to 48)

$\overline{\text{INT}}$ Pin	LC89057W-VF4A-E					LC89058W-E				
Pull-down	Modulation function					General-purpose I/O function				S/PDIF
	Pin.44	Pin.45	Pin.46	Pin.47	Pin.48	Pin.44	Pin.45	Pin.46	Pin.47	Pin.48
	TMCK	TBCK	TLRCK	TDATA	TXO	GPIO0	GPIO1	GPIO2	GPIO3	RXOUT2
	Input	Input	Input	Input	Output	Input	Input	Input	Input	Output
Pull-up	General-purpose I/O function					General-purpose I/O function				S/PDIF
	Pin.44	Pin.45	Pin.46	Pin.47	Pin.48	Pin.44	Pin.45	Pin.46	Pin.47	Pin.48
	PIO0	PIO1	PIO2	PIO3	PIOEN	GPIO0	GPIO1	GPIO2	GPIO3	RXOUT2
	In/Output	In/Output	In/Output	In/Output	Input	Output	Output	Output	Output	Output

7.5.1 Change from LC89057W-VF4A-E to LC89058W

7.5.1 When the $\overline{\text{INT}}$ pin is set to pull-down

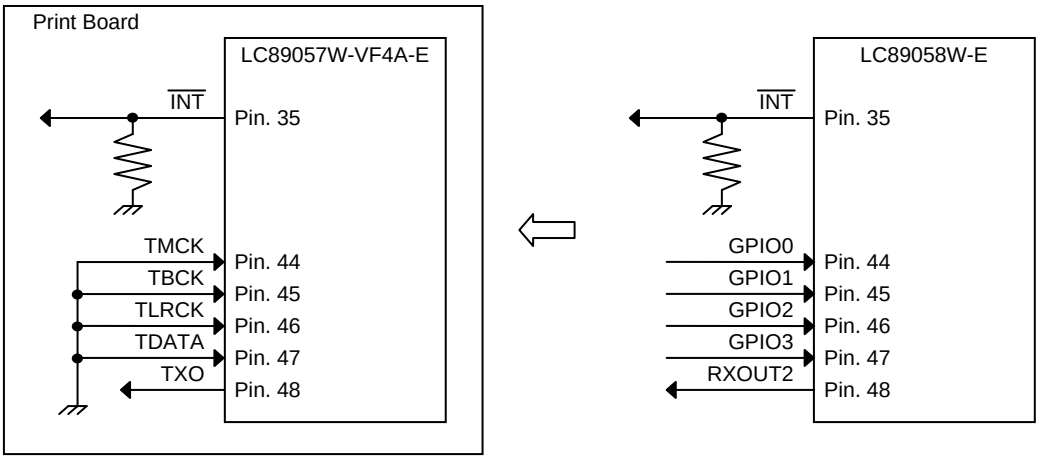


Figure 7.1 Change from LC89057W-VF4A-E to LC89058W-E (when the $\overline{\text{INT}}$ pin is set to pull-down)

- In this case, the system that doesn't use a modulation function or a general-purpose I/O function can be replaced with LC89058W-E.
- After the replacement, LC89058W-E is used on condition that it pins 44 to 47 connect with GND and pin 48 open.

7.5.1.2 When the $\overline{INT}$ pin is set to pull-up

7.5.1.2.1 In case of "Pin 48 = GND"

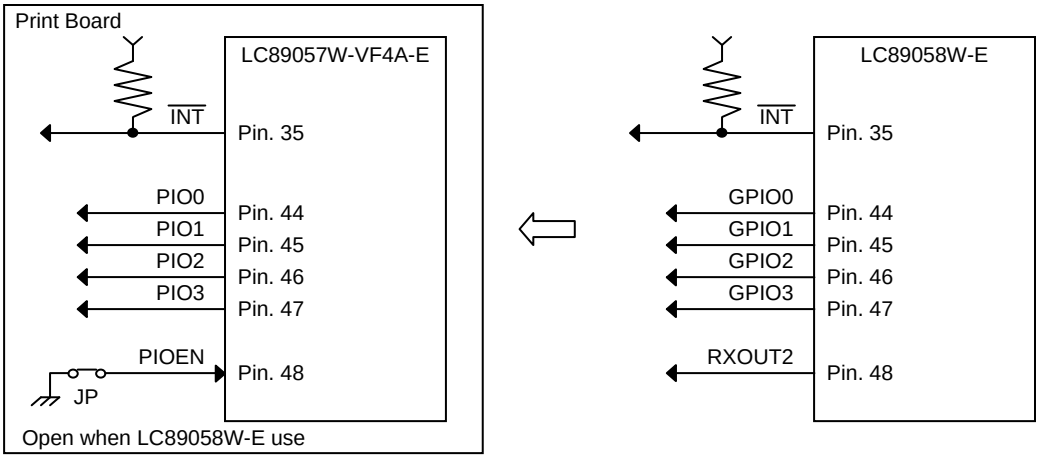


Figure 7.2 Change from LC89057W-VF4A-E to LC89058W-E (when the $\overline{INT}$ pin is set to pull-up) 1

- After the replacement, pins 44 to 47 can be used as general purpose I/O output function. (pin 48 open)
- It is necessary to review the circuit pattern of the printed circuit board because the I/O setting of pin 48 differs from each other.

7.5.1.2.2 In case of "Pin 48 = V_{DD}"

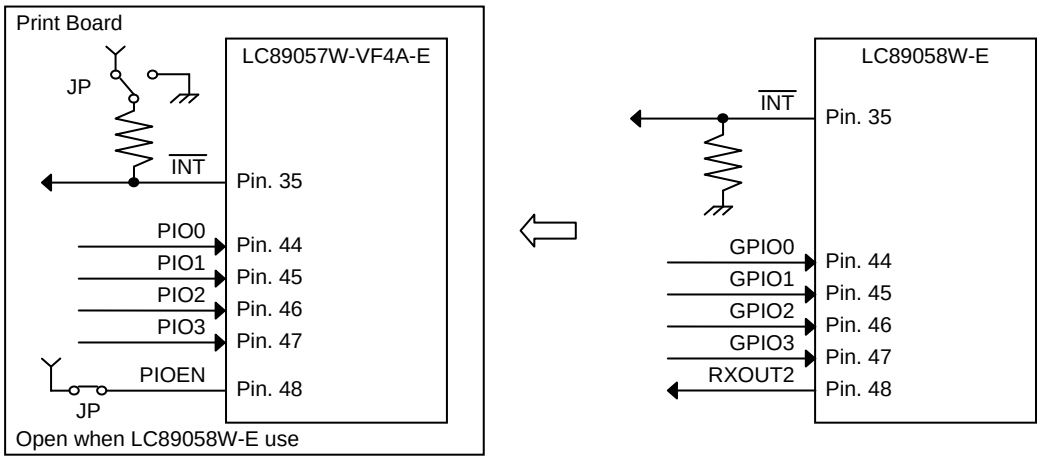


Figure 7.3 Change from LC89057W-VF4A-E to LC89058W-E (when the $\overline{INT}$ pin is set to pull-up) 2

- It is necessary to review the circuit pattern of the printed circuit board to change the pull-up resistor of pin 35 to the pull-down resistor because pins 44 to 47 is used as general purpose I/O input function.
- It is necessary to review the circuit pattern of the printed circuit board because the I/O setting of pin 48 differs from each other.

7.5.2 Change from LC89058W-E to LC89057W-VF4A-E

7.5.2.1 When the $\overline{\text{INT}}$ pin is set to pull-down

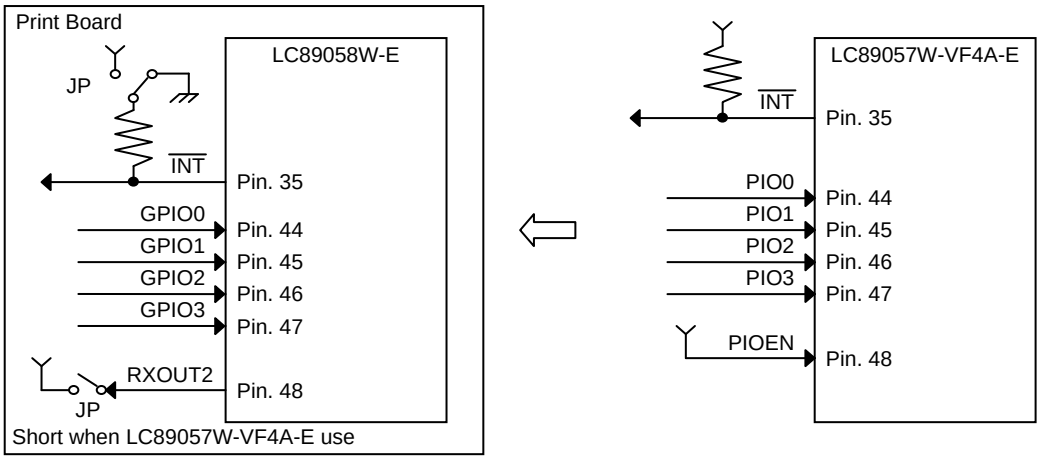


Figure 7.4 Change from LC89058W-E to LC89057W-VF4A-E (when the $\overline{\text{INT}}$ pin is set to pull-down)

- It is necessary to review the circuit pattern of the printed circuit board to change the pull-up resistor of pin 35 to the pull-down resistor because pins 44 to 47 is used as general purpose I/O input function.
- It is necessary to review the circuit pattern of the printed circuit board because the I/O setting of pin 48 differs from each other.
- After the replacement, the RXOUT2 output of LC89057W-VF4A-E cannot be used.

7.5.2.2 When the $\overline{\text{INT}}$ pin is set to pull-up

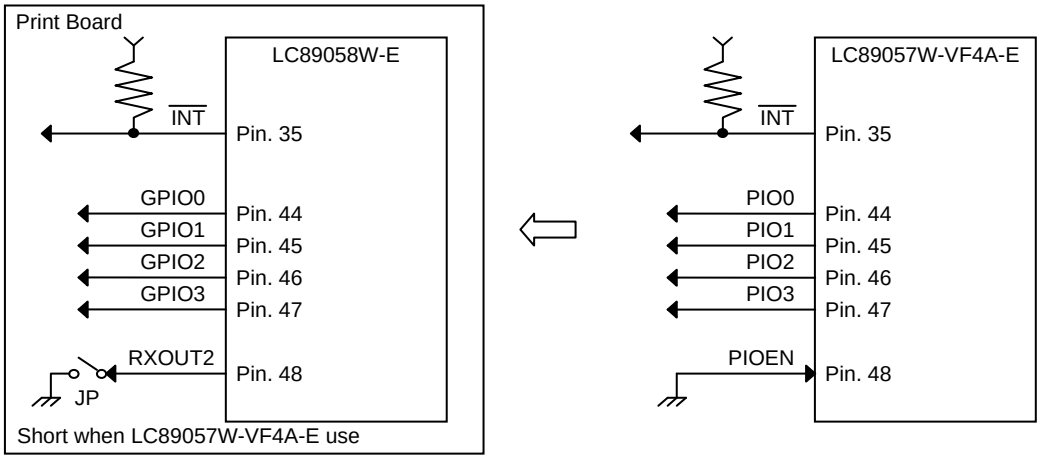


Figure 7.5 Change from LC89058W-E to LC89057W-VF4A-E (when the $\overline{\text{INT}}$ pin is set to pull-up)

- After the replacement, pins 44 to 47 can be used as general purpose I/O output function. However, it is necessary to review the circuit pattern of printed circuit board because pin 48 has to GND.
- After the replacement, the RXOUT2 output of LC89057W-VF4A-E cannot be used.

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 8.1: Absolute Maximum Ratings at AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	AV_{DD} max	8-1-1	-0.3 to +4.6	V
Maximum supply voltage	DV_{DD} max	8-1-2	-0.3 to +4.6	V
Input voltage 1	$V_{IN}1$	8-1-3	-0.3 to V_{DD}+0.3 (max.3.9V)	V
Input voltage 2	$V_{IN}2$	8-1-4	-0.3 to +5.8	V
Output voltage	V_{OUT}	8-1-5	-0.3 to V_{DD}+0.3 (max.3.9V)	V
Storage ambient temperature	Tstg		-55 to +125	°C
Operating ambient temperature	Topr		-30 to +70	°C
Maximum input/output current	I_{IN}, I_{OUT}	8-1-6	±20	mA

8-1-1: AV_{DD} pin
8-1-2: DV_{DD} pin
8-1-3: RX1, RBCK, RLRCK, XIN, GPIO0, GPIO1, GPIO2, GPIO3 pins
8-1-4: RX0, RX2, RX3, RX4, RX5, RX6, SDIN, DI, CE, CL, XMODE pins
8-1-5: RXOUT1, RMCK, RBCK, RLRCK, RDATA, SBCK, SLRCK, XMCK, XOUT, MOUT, $\overline{\text{AUDIO}}$ pins, CKST, $\overline{\text{INT}}$, RERR, DO, GPIO0, GPIO1, GPIO2, GPIO3, RXOUT2 pins
8-1-6: Per input/output pin

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

8.2 Allowable Operating Ranges

Table 8.2: Recommended Operating Conditions at AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	AV_{DD}, DV_{DD}		3.0	3.3	3.6	V
Input voltage range 1	$V_{IN}1$	8-2-1	0	3.3	AV_{DD}, DV_{DD}	V
Input voltage range 2	$V_{IN}2$	8-2-2	0	3.3	5.5	V
Operating temperature	Topr		-30		70	°C

8-2-1: RX1, RBCK, RLRCK, XIN, GPIO0, GPIO1, GPIO2, GPIO3 pins
8-2-2: RX0, RX2, RX3, RX4, RX5, RX6, SDIN, DI, CE, CL, XMODE pins

8.3 DC Characteristics

Table 8.3: DC Characteristics at Ta = -30 to 70°C, AV_{DD} = DV_{DD} = 3.0 to 3.6V, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input, High	V_{IH}	8-3-1	$0.7V_{DD}$			V
Input, Low	V_{IL}				$0.2V_{DD}$	V
Input, High	V_{IH}	8-3-2	2.0		5.8	V
Input, Low	V_{IL}		-0.3		0.8	V
Output, High	V_{OH}	8-3-3	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Output, High	V_{OH}	8-3-4	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Output, High	V_{OH}	8-3-5	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Output, High	V_{OH}	8-3-6	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Input amplitude	V_{PP}	8-3-7	200			mV
Consumption current	I_{DD}	8-3-8			40	mA
Pull-down resistance	R_{DN}	8-3-9	25	50	100	kΩ

8-3-1: CMOS compatible: RBCK, RLRCK input pins during XIN and slave settings
8-3-2: TTL compatible: Input pins other than those listed above
8-3-3: I_{OH} = −12mA, I_{OL} = 8mA: RMCK output pin
8-3-4: I_{OH} = −8mA, I_{OL} = 8mA: XOUT, XMCK output pins
8-3-5: I_{OH} = −4mA, I_{OL} = 4mA: RXOUT1, RBCK, RLRCK, RDATA, SBCK, SLRCK, RERR, MOUT, GPIO0, GPIO1, GPIO2, GPIO3, RXOUT2 output pins
8-3-6: I_{OH} = −2mA, I_{OL} = 2mA: Output pins other than those listed above
8-3-7: Before capacitance of RX1 input pin, and reception frequency is possible up to 96kHz.
8-3-8: Ta=25°C, fs=96kHz
8-3-9: RX0, RX2, RX3, RX4, RX5, RX6 input pins

8.4 AC Characteristics

Table 8.4: AC Characteristics at Ta=-30 to 70°C, AV_{DD}=DV_{DD}=3.0 to 3.6V, AGND=DGND=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
RX0, RX2 to RX6 fs frequency	f_{RFS1}		28		195	kHz
RX1 fs frequency	f_{RFS2}		28		108	kHz
RX0, RX2 to RX6 pulse width	t_{WDI1}		20			ns
RX1 pulse width	t_{WDI2}		40			ns
RX0 to RX6 duty factor	t_{DUY}		40		60	%
XIN clock frequency	f_{XF}	8-4-1	12		25	MHz
RMCK clock frequency	f_{MCK}		4		50	MHz
RMCK clock jitter	tj			200		ps
RMCK, RBCK delay	t_{MBO}				10	ns
RBCK, RDATA delay	t_{BDO}				10	ns
RMCK, SBCK delay	t_{MBO}	8-4-2			10	ns
SBCK, RDATA delay	t_{BDO}	8-4-3			10	ns

8-4-1 A frequency compatible with the XINSEL setting must be applied to XIN.
8-4-2: When RMCK and SBCK source clocks are identical
8-4-3: When SBCK is the PLL source clock

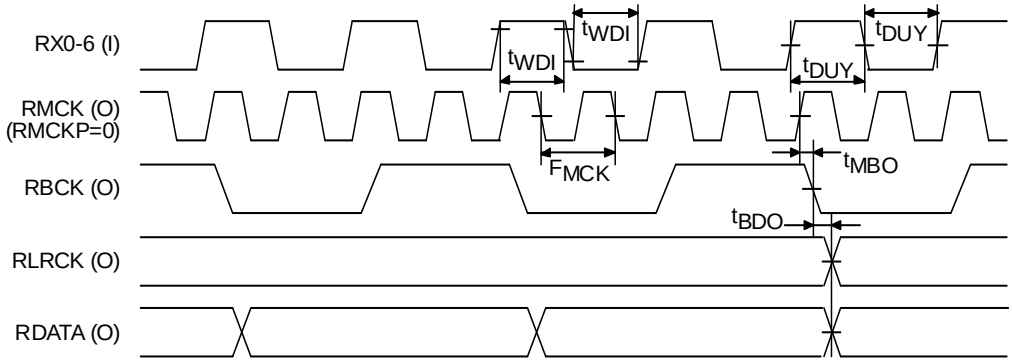


Figure 8.1 AC Characteristics of Demodulation function

8.5 CCB Microcontroller Interface AC Characteristics

Table 8.5: CCB Microcontroller Interface AC Characteristics at Ta=-30 to 70°C, AV_{DD}=DV_{DD}=3.0 to 3.6V, AGND=DGND=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
XMODE pulse width, Low	$t_{RST\ dw}$		200			µs
CL pulse width, Low	$t_{CL\ dw}$		100			ns
CL pulse width, High	$t_{CL\ uw}$		100			ns
CL to CE setup time	$t_{CE\ setup}$		50			ns
CL to CE hold time	$t_{CE\ hold}$	8-5-1	50			ns
CL to CE hold time	$t_{CE\ hold}$	8-5-2	0			ns
CL to DI setup time	$t_{DI\ setup}$		50			ns
CL to DI hold time	$t_{DI\ hold}$		50			ns
CL to CE hold time	$t_{CL\ hold}$		50			ns
CL to DO delay time	$t_{CL\ to\ DO}$				20	ns
CE to DO delay time	$t_{CE\ to\ DO}$				20	ns
DI pulse width	$t_{DI\ dw}$	8-5-3	200			ns

8-5-1: CL has to lower before CE is H when CL is normal H clock.
8-5-2: Only when data write with CL of normal H clock.
8-5-3: DI has to L period for the reset period when DI is normal H.

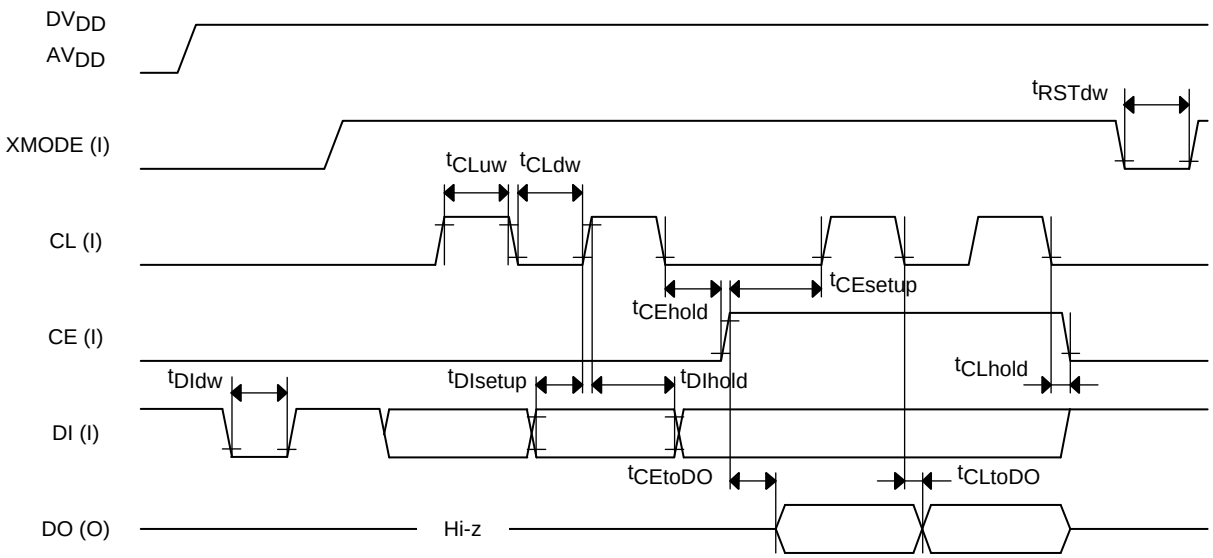


Figure 8.2 CCB Microcontroller Interface AC Characteristics

9. Initial System Settings

9.1 System Reset (XMODE)

- The system operates correctly when XMODE is set to "H" after 3.0V or higher supply voltage is applied. When XMODE is set to "L" after power is turned on, the system is reset.
- To set chip address, master/slave, or pins 44 to 47 I/O, 10kΩ pull-down or pull-up resistors must be connected to MOUT, $\overline{\text{AUDIO}}$, CKST, and $\overline{\text{INT}}$.
- If none of MOUT, $\overline{\text{AUDIO}}$, CKST, and $\overline{\text{INT}}$ are pulled down or pulled up, their pin state will get unstable when the settings are entered, resulting in wrong setting. Pull-up or pull-down resistors must be connected to these pins without fail.

Table 9.1: Pin Names and Settings

Setting	Pins
Chip address	MOUT
	$\overline{\text{AUDIO}}$
Master/slave setting	CKST
Pins 44 to 47 I/O setting	$\overline{\text{INT}}$

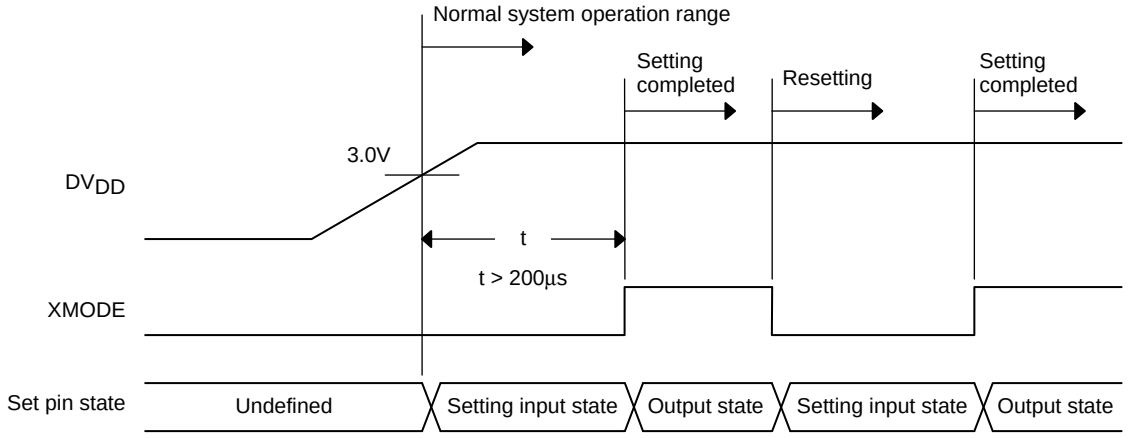


Figure 9.1 Setting Timing Chart of Function Setting Input Pins

Table 9.2: Output Pin State When XMODE is Reset (XMODE=L)

No.	Pin name	Pin State	No.	Pin name	Pin State
1	RXOUT1	RXO output	32	MOUT	Input state
16	RMCK	XIN output	33	$\overline{\text{AUDIO}}$	Input state
17	RBCK	Low output	34	CKST	Input state
20	RLRCK	High output	35	$\overline{\text{INT}}$	Input state
21	RDATA	Low output	36	RERR	High output
22	SBCK	Low output	37	DO	Hi-z output
23	SLRCK	High output	48	RXOUT2	Low output
27	XMCK	XIN output			

9.2 Chip Address Settings (MOUT, $\overline{\text{AUDIO}}$)

- The LC89058W-E comes with a function to set a unique chip address to allow the use of several LC89058W-E on the same microcontroller interface bus.
- In chip address setting, connect a 10kΩ pull-down or pull-up resistor to MOUT and $\overline{\text{AUDIO}}$. By this setting, 4 kinds of chip addresses can be set at a maximum.
- Chip addresses in the microcontroller interface are set with CAL and CAU provided as the first two bits on the LSB side. CAL corresponds to the lower chip address and CAU to the higher chip address.
- Command writing is enabled by making the chip address settings with MOUT and $\overline{\text{AUDIO}}$ identical to the chip addresses sent from the microcontroller.
- The chip address setting is required even when only one LC89058W-E is used in the system. If the chip address is not set, the chip address is undefined and the microcontroller cannot control the system. When the microcontroller is not used, a chip address-setting pin is input open while XMODE is "L". Be sure to connect either a pull-down resistor or a pull-up resistor to MOUT and $\overline{\text{AUDIO}}$.

Table 9.3: Chip Address Settings (Resistor Connection)

$\overline{\text{AUDIO}}$	MOUT	CAU	CAL
Pull-down	Pull-down	0	0
Pull-down	Pull-up	0	1
Pull-up	Pull-down	1	0
Pull-up	Pull-up	1	1

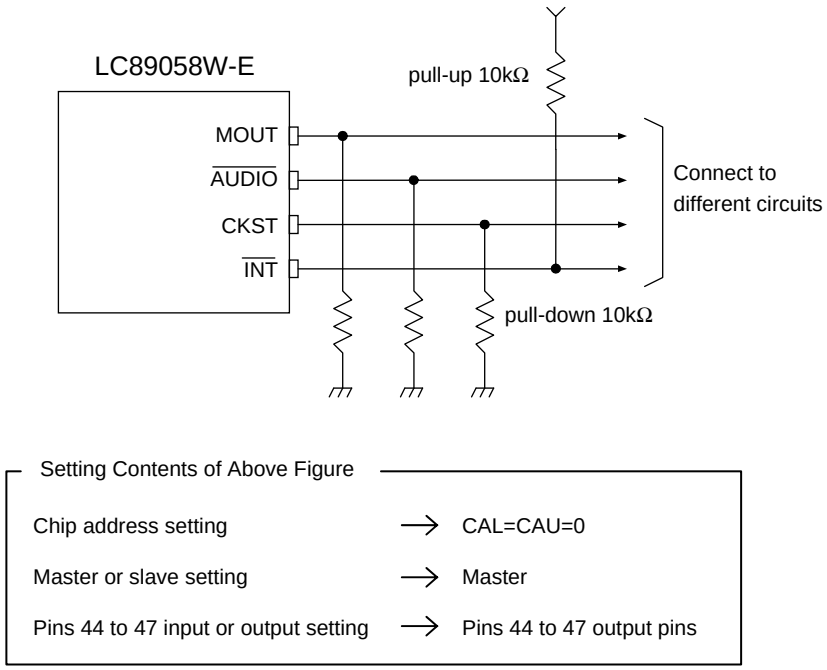


Figure 9.2 Setting Example of Function Setting Input Pin

9.3 Master/Slave Settings (CKST)

- A master/slave function that allows multi-channel synchronized transfer using multiple LC89058W-Es is included. For this setting, connects either a 10kΩ pull-down or a pull-up resistor to CKST.
- Set to the master mode normally, when single LC89058W-E IC is used. When multiple LC89058W-Es are used, set one of them to the master mode and the others to the slave mode.
- In the multi-channel synchronous transfer mode using multiple LC89058W-Es, connect RBCK and RLRCK (output) on the master side to RBCK and RLRCK (input) on the slave side. Also connect XMCK on the master side to XIN on the slave side. At this time, the polarity of RBCK and RLRCK, and the frequency of XIN and XMCK must be identical.
- The master/slave function runs correctly with the multiple LC89058W-Es connected.
- Be sure to connect either a pull-down resistor or a pull-up resistor to CKST.
- Always supply the clock to RBCK and RLRCK when the slave function is set.

Table 9.4: Master/Slave Switching (Register Connection)

CKST	Mode
Pull-down	Master
Pull-up	Slave

Table 9.5: Clock Pin State

Pin	Master mode	Slave mode
RMCK	Output	Output
RBCK	Output	Input
RLRCK	Output	Input

9.4 Pins 44 to 47 I/O settings ($\overline{\text{INT}}$)

- Pins 44 to 47 are provided with a bidirectional buffer.
- When setting I/O function of pins 44 to 47, connect a 10kΩ pull-down or pull-up resistor to $\overline{\text{INT}}$.
- Be sure to connect either a pull-down resistor or a pull-up resistor to $\overline{\text{INT}}$.

Table 9.6: Pins 44 to 47 I/O Settings (Resistor Connection)

$\overline{\text{INT}}$	Mode
Pull-down	Input.
Pull-up	Output.

10 Description of Demodulation Function

10.1 Clocks

10.1.1 PLL (LPF)

- The LC89058W-E incorporates a VCO (Voltage Controlled Oscillator) that can be stopped with PLLOPR and it synchronizes with sampling frequencies (fs) from 32kHz to 192kHz and with the data with transfer rate from 4MHz to 25MHz. PLL is locked at 512fs.
- LPF is a pin for PLL loop filter. Connect the following resistance and capacitance shown in the figure.

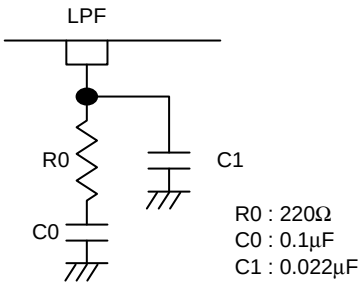


Figure 10.1 Loop Filter Configuration

10.1.2 Oscillation amplifiers (XIN, XOUT, XMCK)

- The LC89058W-E features a built-in oscillation amplifier. Connecting a quartz resonator, feedback resistor, and load capacitance to XIN and XOUT can configure an oscillation circuit. When connecting a quartz resonator, use one with a fundamental wave. Be aware that the load capacitance depends on the quartz resonator characteristics.
- If the built-in oscillation amplifier is not used and oscillation module is used as the clock source instead, connect the output of an external clock supply source to XIN. At this time, it is not necessary to connect a feedback resistor between XIN and XOUT.
- Always supply XIN with the 12.288MHz or 24.576MHz clock set with XINSEL. If supplying other frequencies to XIN, it is necessary to set that the result of change in sampling frequency fs of input data with FSERR is not reflected to an error flag. By this setting, the operation functions properly. Since it is not a recommended frequency, it cannot be used for input fs calculations.
- The setting of XINSEL must be completed prior to S/PDIF input.
- Supply XIN with clocks all the time to be used in the following applications.

  (1) Detection of presence or absence of S/PDIF input
  (2) Clock source while PLL is unlocked
  (3) Calculation of input data sampling frequency
  (4) Time definition when switching input data
  (5) External source of supply clock (clock for an AD converter, etc.) in XIN source mode.
  (6) Polling processing performed when setting the general-purpose I/O input function

- The oscillation amplifier runs even when the PLL is locked. Therefore, data detection and calculation of input sampling frequency become possible while the PLL is locked. In that case, both the oscillation amplifier clock and the PLL clock signals coexist, and then user must pay attention and make sure sound quality is not adversely affected.
- If adverse effects on the sound quality are recognized, it is possible to set with the AMPOPR [1:0] that the oscillation amplifier automatically stop operation while the PLL is locked. Therefore, setting of the AMPOPR [1:0] must be completed either prior to S/PDIF input or while PLL is unlocked.
- The oscillation amplifier can be stopped if it is unnecessary. However, when the normal operation is resumed, it must wait for 10ms or longer until the resonator oscillation gets stable.
- XMCK outputs the XIN clock. The XMCK output is set with XMSEL [1:0]. The XIN clock can be set to 1/1, 1/2, 1/4, or muted output.
- If you use only the oscillation amplifier, input the quartz resonator to XIN and XOUT or an external clock to XIN, and fix the electric potential of digital data input pins of RX0 to RX6, or set with RISEL [2:0] that all the inputs are deselected.

10.1.3 Switching between master clock and clock source

- The RMCK, RBCK, and RLRCK (hereunder, R system), and the SBCK and SLRCK (hereunder, S system) clock sources can be selected between the following two master clocks.
  (1) PLL source (512fs)
  (2) XIN source (12.288MHz or 24.576MHz)

- Clock source switching is to set with the R and S systems interlocked. This setting is carried out with OCKSEL.
- The clock source is automatically switched to the PLL or XIN clock by locking/unlocking the PLL. The clock source can be switched to XIN with OCKSEL, regardless of the PLL status.

Table 10.1: Relationship between Clock Source Switch Commands and Clock Sources when PLL Locked/Unlocked

OCKSEL	R System Clock Source		S System Clock Source	
	Locked	Unlocked	Locked	Unlocked
0	PLL	XIN	PLL	XIN
1	XIN	XIN	XIN	XIN

- The PLL status can be always monitored with RERR even after switching to the XIN source. Moreover, the processed information can be read with the microcontroller interface regardless of the PLL status.

10.1.4 Points to notice about switching clock source while PLL is locked

- It is necessary to set the oscillation amplifier to the continuous operation mode at the same time with AMPOPR [1:0] to do the clock switch to the XIN source with OCKSEL when the oscillation amplifier has stopped in the state where the PLL is locked. The clock is not output when switching to the XIN clock source without executing this setting.
- In the state where the PLL is locked, if the clock is switched to XIN source with OCKSEL while the oscillator amplifier is stopped, RERR is temporarily outputs an error (high level) indication. When switched to XIN source, the oscillator amplifier is switched to the operating state at the same time.
  RERR is temporality outputs an error (H level) indication when the oscillation amplifier switches from the stop condition to the continuous mode. Consequently the input fs calculation restarts. At this time, the previous fs calculation value is reset and compared with the newly calculated fs value. Then those two values are found not identical, that’s why the error is temporarily issued.

10.1.5 Master clock block diagram (XIN, XOUT, RMCK, XMCK)

- The relationships between the two types of PLL and XIN source master clocks, switching, and the frequency division function are described below.
- The contents in the quotation marks "*** " by the switch and function blocks correspond to the write command names.
- Lock/Unlock is automatically switched by PLL locking/unlocking.

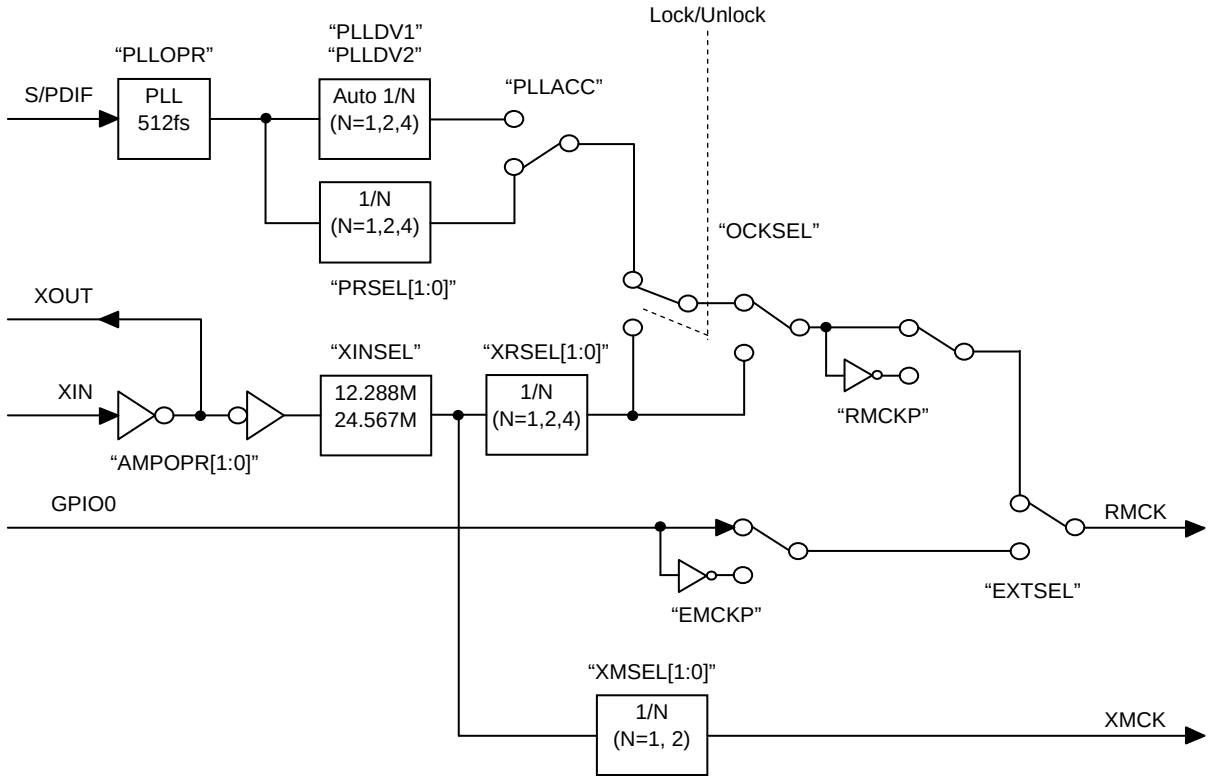


Figure 10.2 Master Clock Block Diagram

10.1.6 PLL clock output

- The PLL clock output is controlled by the PLLACC, PLLDV1, PLLDV2, or PRSEL[1:0].
- PLLACC can be used to generate a PLL lock frequency for each S/PDIF input sampling frequency band.

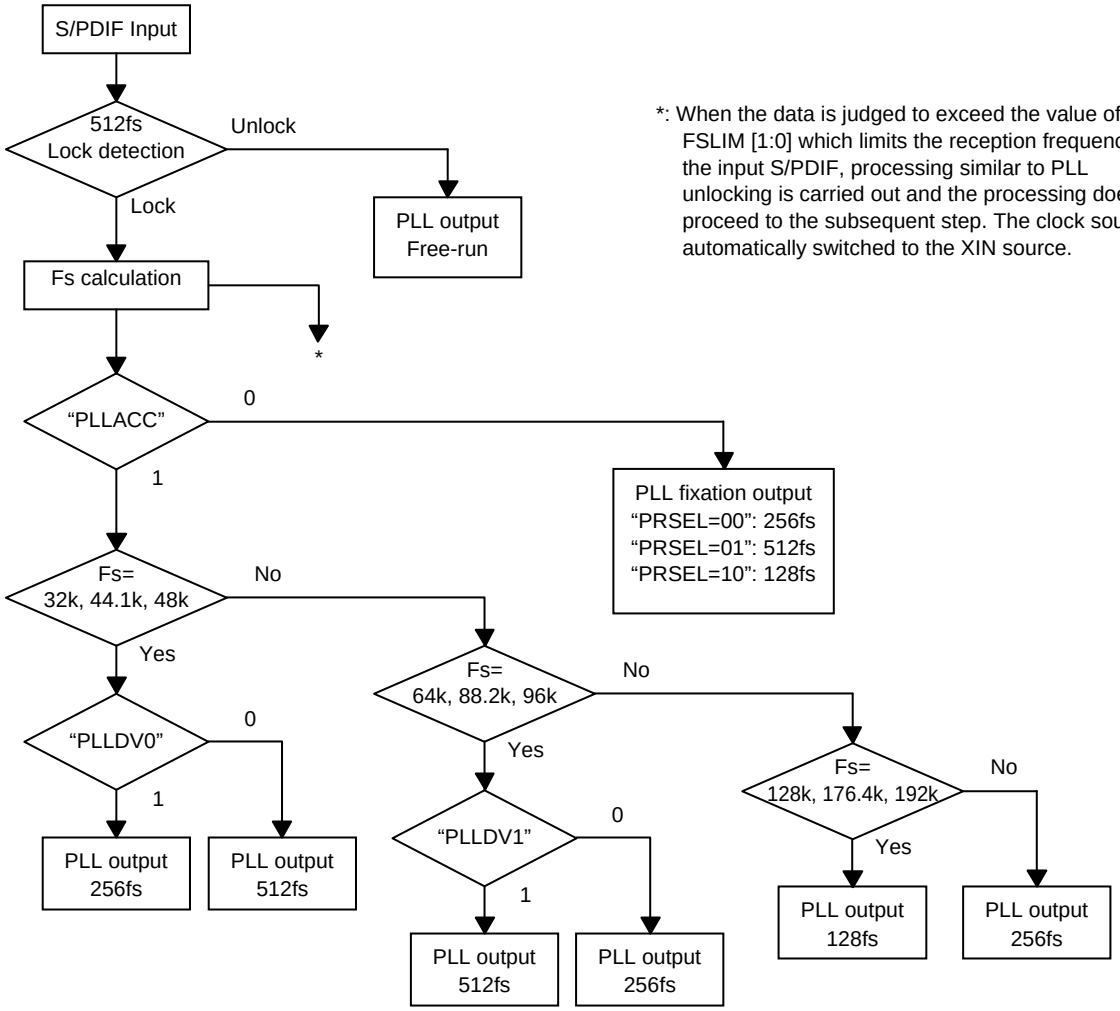


Figure 10.3 PLL Clock Output Control

Table 10.2: PLL Clock Output Frequencies (Bold settings are recommended values.)

S/PDIF fs	PLL Output						
	PLLACC=0 (Fixed multiple outputs of input fs)			PLLACC=1 (Fixed multiple outputs for each input fs band)			
	PRSEL=00 (256fs)	PRSEL=01 (512fs)	PRSEL=10 (128fs)	**PLLDV0=0 PLLDV1=0**	PLLDV0=1 PLLDV1=0	PLLDV0=0 PLLDV1=1	PLLDV0=1 PLLDV1=1
32kHz	8.19MHz	16.38MHz	4.09MHz	**16.38MHz**	8.19MHz	16.38MHz	8.19MHz
44.1kHz	11.28MHz	22.57MHz	5.64MHz	**22.57MHz**	11.28MHz	22.57MHz	11.28MHz
48kHz	12.28MHz	24.57MHz	6.14MHz	**24.57MHz**	12.28MHz	24.57MHz	12.28MHz
64kHz	16.38MHz	32.76MHz	8.19MHz	**16.38MHz**	16.38MHz	32.76MHz	32.76MHz
88.2kHz	22.57MHz	45.15MHz	11.28MHz	**22.57MHz**	22.57MHz	45.15MHz	45.15MHz
96kHz	24.57MHz	49.15MHz	12.28MHz	**24.57MHz**	24.57MHz	49.15MHz	49.15MHz
128kHz	32.76MHz	65.53MHz	16.38MHz	**16.38MHz**	16.38MHz	16.38MHz	16.38MHz
176.4kHz	45.15MHz	90.31MHz	22.57MHz	**22.57MHz**	22.57MHz	22.57MHz	22.57MHz
192kHz	49.15MHz	98.30MHz	24.57MHz	**24.57MHz**	24.57MHz	24.57MHz	24.57MHz

- If 128kHz, 176.4kHz or 192kHz input is received when the PLLACC is set to 0 and the PRSEL [1:0] to 01, the DC characteristics of output directly sent to the RMCK pin cannot be guaranteed. In such a case, set the frequency to one half or quarter of the PLL clock frequency (PRSEL [1:0]=00 or 10).

10.1.7 Output clocks (RMCK, RBCK, RLRCK, SBCK, SLRCK)

- The LC89058W-E features two clock systems (R and S systems) in order to supply the various needed clocks to peripheral devices such as A/D converter and DSP.
- The clock output settings for the R and S systems are done with PLLACC, PLLDV1, PLLVD2, PRSEL[1:0], XRSEL[1:0], XRBCK[1:0], XRLRCK[1:0], PSBCK[1:0], PSLRCK[1:0], XSBCK[1:0], and XSLRCK[1:0].
- Setting range for each clock output pin when the PLL is used as source
  (1) RMCK: Selection from 1/1, 1/2, and 1/4 of PLLACC, PLLDV0, PLLDV1, or 512fs
  (2) RBCK: 64fs output
  (3) RLRCK: fs output
  (4) SBCK: Selection from 128fs, 64fs, 32fs, and 16fs
  (5)SLRCK: Selection from 2fs, fs, 1/2fs, and 1/4fs
- Setting range for each clock output pins when the XIN is used as source
  (1) RMCK: Selection from 1/1, 1/2, and 1/4 of 12.288MHz or 24.576MHz
  (2) RBCK: Selection from 12.288MHz, 6.144MHz, and 3.072MHz
  (3) SBCK: Selection from 12.288MHz, 6.144MHz, and 3.072MHz
  (4) RLRCK: Selection from 192kHz, 96kHz, and 48kHz
  (5) SLRCK: Selection from 192kHz, 96kHz, and 48kHz
- The polarity of RMCK can be reversed with RMCKP.
- The polarity of RBCK, RLRCK, SBCK, and SLRCK can be reversed with RBCKP, RLRCKP, SBCKP, and SLRCKP.

Table 10.3 List of Output Clock Frequencies (Bold Items = Initial Settings)

Output Pin Name	PLL Source (Internal VCO CK)	XIN Source (XIN input CK)	
	512fs	12.288MHz	24.576MHz
RMCK	512fs **256fs** 128fs	**12.288MHz** 6.144MHz	24.576MHz 12.288MHz 6.144MHz
RBCK	**64fs**	12.288MHz (RMCK=24.576MHz) 6.144MHz (RMCK≥12.288MHz) **3.072MHz** (RMCK≥6.144MHz)	
RLRCK	**fs**	192kHz 96kHz **48kHz**	
SBCK	128fs **64fs** 32fs 16fs	12.288MHz (RMCK=24.576MHz) 6.144MHz (RMCK≥12.288MHz) **3.072MHz** (RMCK≥6.144MHz)	
SLRCK	2fs **fs** fs/2 fs/4	192kHz 96kHz **48kHz**	

Notes:

- RBCK and SBCK output clock must not quicken more than RMCK output clock frequency. Also, RBCK and SBCK output clock are set to become 1/2 or less of RMCK output clock at XIN source. If it doesn't follow these conditions, RBCK and SBCK clocks are not output.

10.1.8 Output clocks block diagram (RMCK, RBCK, RLRCK, SBCK, SLRCK, XMCK)

- The relationships between the output clock and switch function are shown below.
- PLL in the figure indicates the PLL source and XIN the XIN source.
- The contents in the quotation marks "***" by the switch function blocks correspond to the write command names.
- The broken lines connecting the switches indicate coordinated switching.
- Lock/Unlock is switched automatically by PLL locking/unlocking.

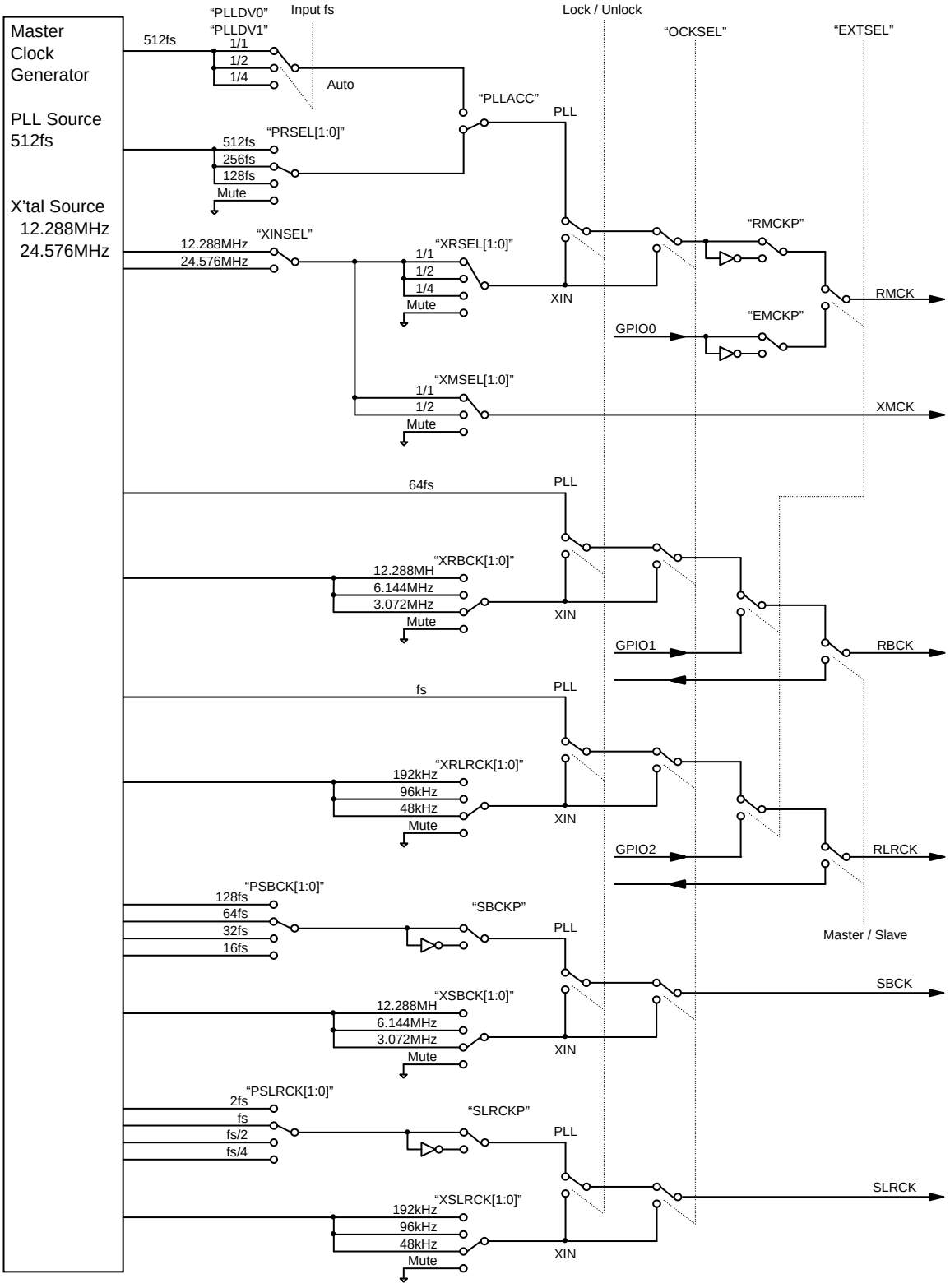
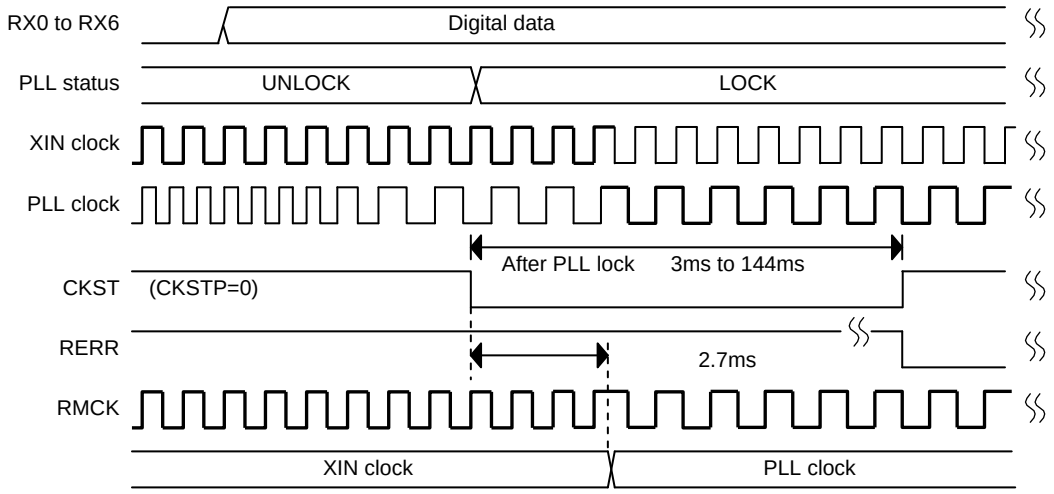


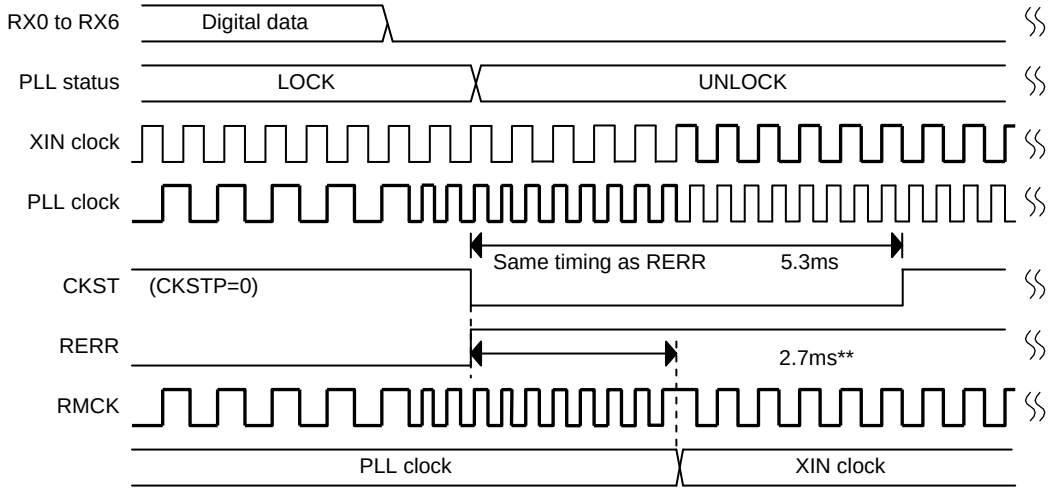
Figure 10.4 Clock Output Block Diagram

10.1.9 Output of clock switch transition signal (CKST)

- CKST outputs pulse when the output clock changes by PLL lock/unlock.
- The polarity of the CKST pulse output can be reversed with CKSTP. Subsequently, CKSTP is assumed to be 0.
- In the lock-in stage, the CKST falls at the word clock generated from the XIN clock after PLL is locked following detection of input data, and rises at the same timing as RERR after a designated period.
- In the unlock stage, the CKST falls at the same timing as RERR, PLL lock detection signal, and rises after word clocks generated from the XIN clock are counted for a designated period.
- Change of the PLL lock status and timing of the clock change can be seen by detecting the rising and falling edges and pulses of CKST.
- The clock is switched after the PLL lock condition is tested and identified. The timing of this clock switching is determined by setting the PTOXW [1:0]. The initial value is such that the clock is switched in 2.7ms after the falling edge of CKST. The value, however, assumes that the oscillation amplifier is set to permanent operation mode. If the oscillation amplifier is set to be stopped after PLL locking, the startup time before the oscillation amplifier stabilizes after PLL unlocking, is added.
- A free-running clock is output from the clock output pin immediately after PLL unlocking.



(a): Lock-in stage



**: When set to PTOXW[1:0]=00 (max.)

(b): Unlock stage

Figure 10.5 Clock Switch Timing

10.1.10 Output clocks generated when input S/PDIF reception is limited

- The same processing performed when the PLL is unlocked is carried out if an S/PDIF input exceeding the reception range limit (which can be defined by FSLIM[1:0]) is supplied. The clock source is then switched to the XIN clock and clocks are output from respective clock pins.

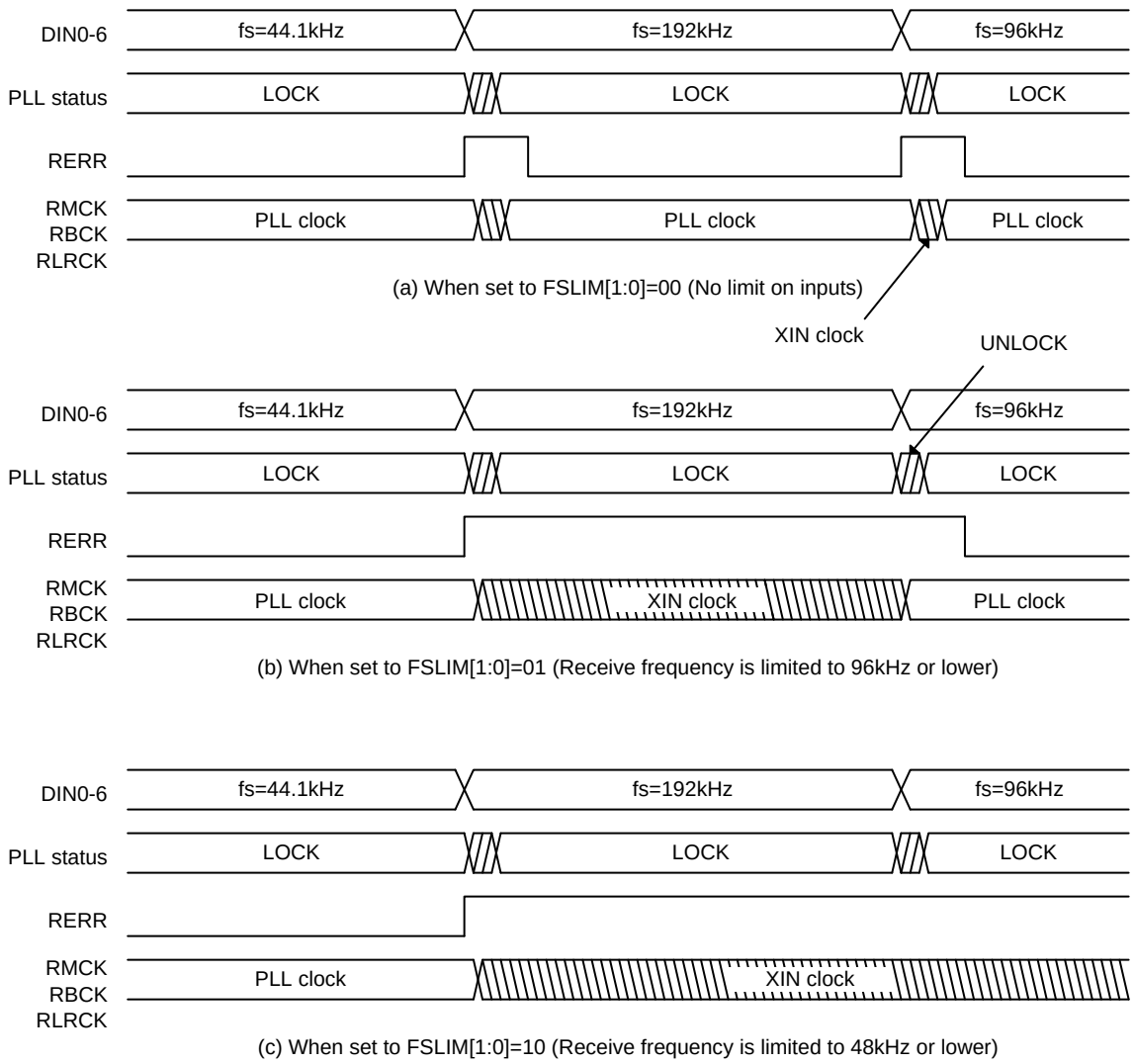


Figure 10.6 Output Clocks Generated When Input Data Reception Is Limited

10.2 S/PDIF I/O

10.2.1 Reception range of S/PDIF input

- The guaranteed reception range of input data is shown below.

Table 10.4: S/PDIF Reception Range (FSLIM [1:0]=00)

PLL Output Clock Setting	Input Data Reception Range
512fs	30kHz to 192kHz

Note:
(1) Reception range of RX1 is 32kHz to 96kHz.
(2) PLL output clock is frequency-divided with PLLACC, PLLDIV and PRSEL [1:0] and is output from RMCK.

- The fs reception range for input data can be limited within the set range of PLL output clocks stated above. This setting is carried out with FSLIM [1:0]. When this function is adopted, input data exceeding the set range is considered as an error, the clock source is automatically switched to the XIN source, and RDATA output data is subject to the RDTSEL setting.

10.2.2 S/PDIF I/O pins (RX0 to RX6, RXOUT1, RXOUT2)

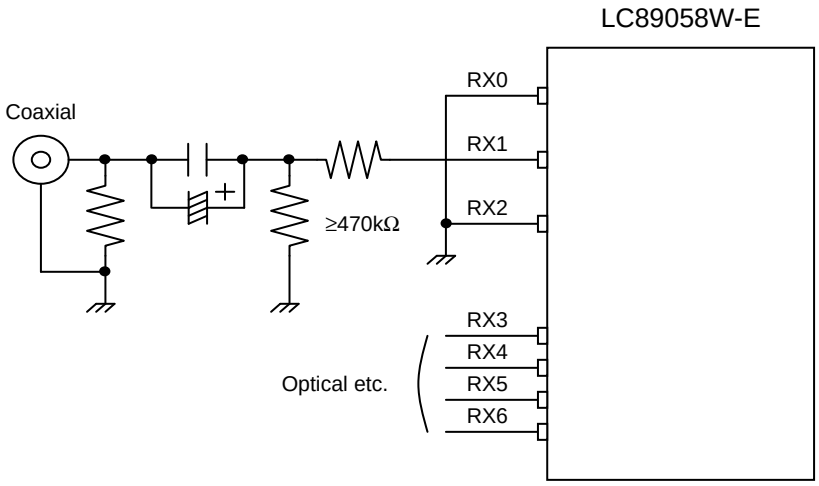
- S/PDIF input pins are 7 inputs at maximum.
  (1) RX1 is a coaxial-compatible input pin. When using RX1, connect RX0 and RX2 to GND.
  (2) RX0, RX2, RX3, RX4, RX5, and RX6 are TTL input level pins with 5V-tolerance voltage.
  (3) Make sure that the selected pins are not input-open. For points to notice on RX1, see the following subsection.
  (4) The unselected pins are pulled down with their internal resistors.

- The demodulation input and S/PDIF through-output pins RXOUT1 and RXOUT2 data can be selected independently.
  (1) The demodulation data is selected with RISEL[2:0].
  (2) The RXOUT1 output data is selected with ROSEL[2:0].
  (3) The RXOUT2 output data is selected with RXSEL[2:0].

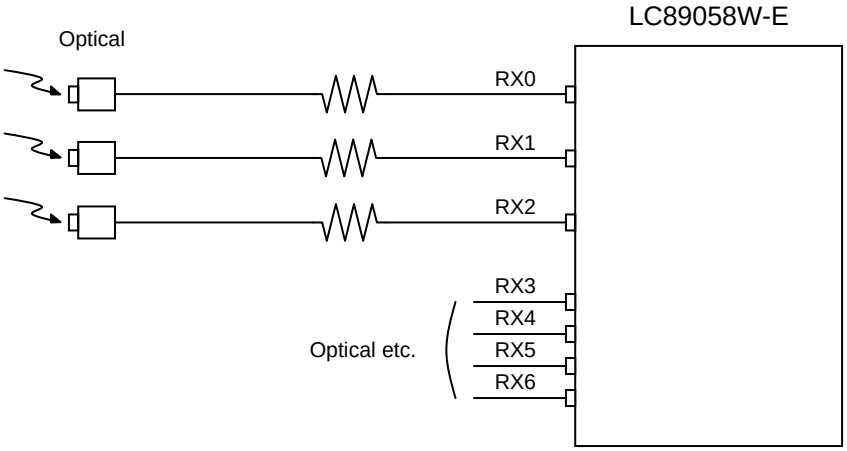
- It is possible to deselect all of RX0 to RX6 with RISEL[2:0] (RISEL[2:0]=111).
- RXOUT1 and RXOUT2 can be muted with RXOSEL[2:0] and RXSEL[2:0], respectively. Muting is recommended to reduce jitter when RXOUT1 and RXOUT2 are not used.
- The data input state can be monitored with the RXMON setting. The status of each data input pin is stored in CCB address 0xEA and output registers DO0 to DO7. Moreover, the latest information can be read with the microcontroller by setting the interrupt processing command INDET. For details, see Chapter 12, Microcontroller Interface.
- The frequencies of input data that can be monitored with this setting is from 32kHz to 192kHz. The data detection function applies to IEC60958 compatible S/PDIF data. The frequency of the clock supplied to XIN when RXMON is set is limited to 24.576MHz. LC89058W-E does not run at any clock frequency other than 24.576MHz. Moreover, since this function uses the XIN clock, the oscillation amplifier must be set in the continuous operation mode when RXMON is set.
- When the data input monitoring is specified, the input pins, except RX1pin and those which are selected for demodulation, are pulled down. This is to preclude input-open when detecting no connection input pins. For the peripheral circuit of the RX1 pin, see the following page.

10.2.3 S/PDIF input circuits (RX0 to RX6)

- RX0, RX2, RX3, RX4, RX5, and RX6 can be received the data of 32kHz to 192kHz.
- RX1 can be received up to 96kHz data.
- If RX1 with a built-in amplifier is used as a coaxial input pin, malfunction may occur due to the influence from the adjacent RX0 and RX2 input pins. To avoid the influences from those pins, fix RX0 and RX2 to "L". In addition, the pull-down resistor is inserted after the coupling capacitor for the noise measures, when the signal is not connected with RX1 is selected.
- When RX1 is selected and the input signal to RX1 is always fixed to either "H" or "L" (Toslink etc), RX0 and RX2 processes are not required.
- RX0, RX2, RX3, RX4, RX5, and RX6 are TTL input level compatible S/PDIF input pins with 5V-tolerance voltage.



(a) Coaxial input circuit



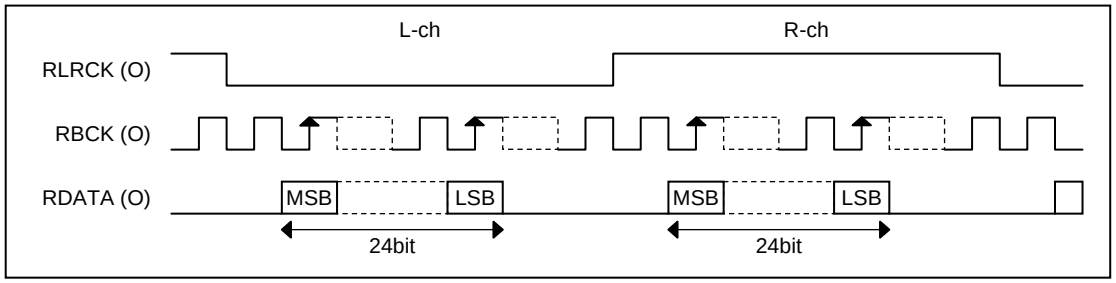
(b) Optical input circuit

Figure 10.7 S/PDIF Input Circuits

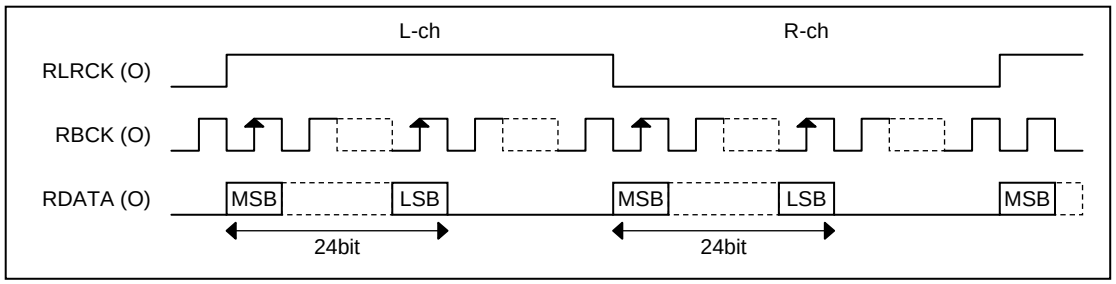
10.3 Serial Audio Data I/O

10.3.1 Output data format (RDATA)

• The output format is set with OFDSEL.
• The initial value of output format is I^2S.
• Output data is output synchronized with the RLRCK edge immediately after the RERR output becomes "L".



(0): I^2S data output

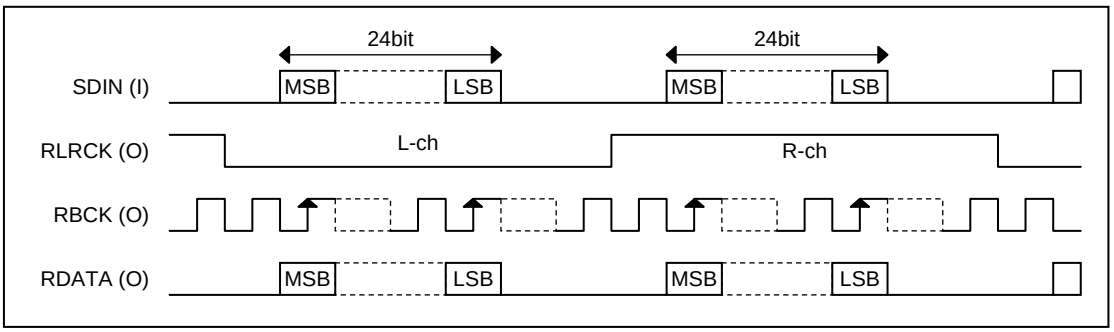


(1): MSB-first front-loading data output

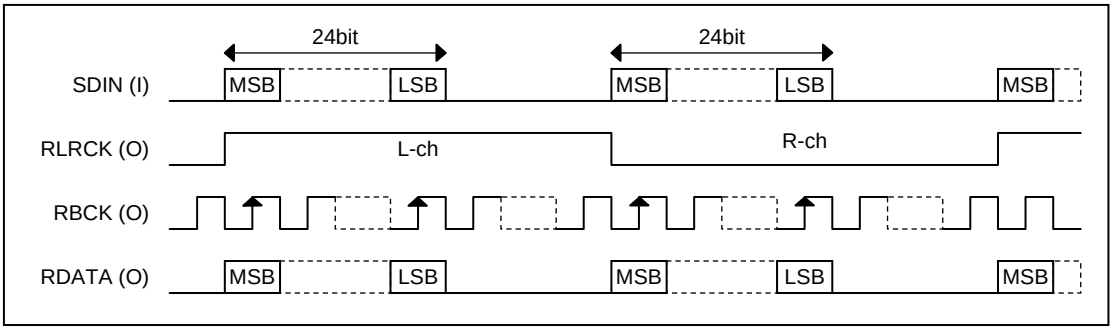
Figure 10.8 Data Output Timing

10.3.2 Serial audio data input format (SDIN)

- LC89058W-E is provided with a serial data input pin of SDIN.
- The format of the serial audio data input to SDIN and the demodulation data output format must be identical.
- The initial value of modulation data output format is I^2S.
- The SDIN data to be input must be in synchronization with the RBCK and RLRCK clocks.
- The data input from the SDIN pin is through-output to the RDATA pin.
- The SDIN pin must be connected to GND when it is not used.



(0): I^2S data output



(1): MSB-first front-loading data input

Figure 10.9 Serial Audio Data Input Timing

10.3.3 Output data switching (SDIN, RDATA)

- RDATA outputs demodulation data when the PLL is locked, and outputs SDIN input data when the PLL is unlocked. This output is automatically switched according to the PLL locked/unlocked status. For details, see the timing charts below.
- When SDIN input data is selected, switch to a clock source synchronized to the SDIN data.
- With the RDTSTA setting, the SDIN input data is output to RDATA regardless of the locked/unlocked status of the PLL.
- With the RDTMUT setting, the RDATA output data can be also muted forcibly.
- Even when the clock source is set to XIN with OCKSEL and RCKSEL, the PLL continues operating as long as the PLL is not stopped with PLLOPR. At this time, the PLL status is continuously output from RERR unless error output is forcibly set with RESTA. Moreover, the processed information can be read with the microcontroller interface regardless of the PLL status.

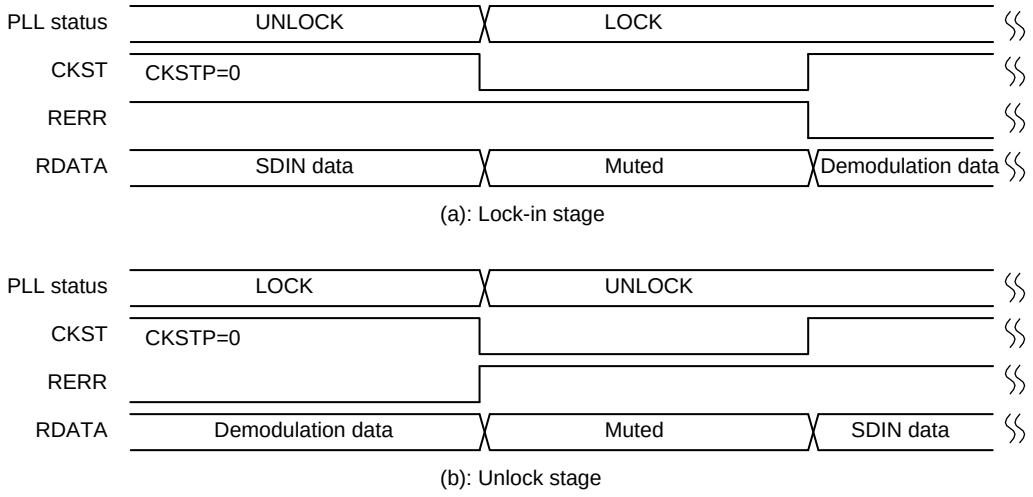


Figure 10.10 Timing Chart of RDATA Output Data Switching

10.3.4 Data block diagram (RX0 to RX6, RXOUT1, RXOUT2, RDATA, SDIN)

- Select the demodulated data and the SDIN input data with RDTSEL and RDTSTA, and mute processing can be performed with RDTMUT.
- Moreover, GPIO0 input data can be selected with EXTSEL. Also, GPIO0 can be subject to mute processing with EDTMUT. See Chapter 11 for the selector function for the general-purpose I/O pins (GPIO0 to GP1O3).

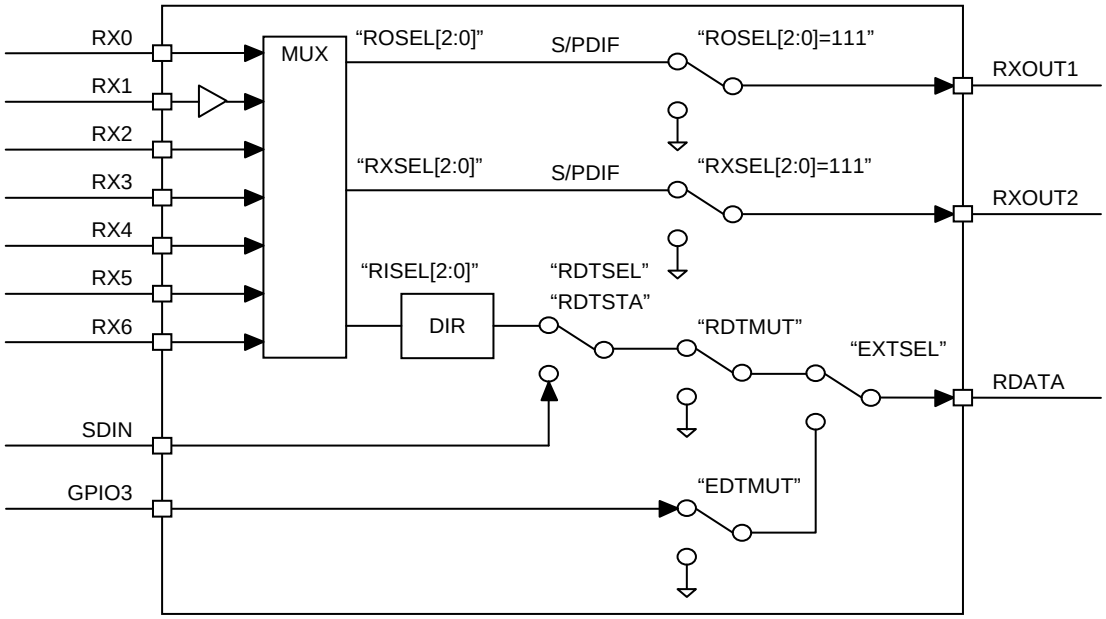


Figure 10.11 Data System Diagram

10.3.5 Calculation of input data sampling frequency (MOUT)

- The input data sampling frequency is calculated using the XIN clock.
- In the mode where the oscillation amplifier automatically stops according to the lock status of the PLL, the input data sampling frequency is calculated during the RERR error period and completed when the oscillation amplifier stops with holding the value. Therefore, the value remains unchanged until the PLL becomes unlocked.
- If the oscillation amplifier is in a continuous operation mode, calculation is repeated constantly. Even if sampling changes within the PLL capture range for input data whose channel status sampling information does not change, the calculation results that follow the input data can be read.
- The calculation results can be readout via MOUT pin or with the microcontroller interface. Since the MOUT pin is also used to generate the emphasis information, set the contents of the MOUT pin output by MOSEL. The fs calculation output to the MOUT pin is limited. The FSSEL[1:0] sets the contents of the MOUT pin output.

Table 10.5: MOUT Pin Output Mode Settings

FSSEL1	FSSEL0	MOUT Pin H Output Conditions
0	0	When calculating 32kHz, 44.1kHz or 48kHz
0	1	When calculating 88.2kHz or 96kHz
1	0	When calculating 176.4kHz or 192kHz
1	1	When calculating 88.2kHz, 96kHz or higher

10.4 Error Output Processing

10.4.1 Lock error and data error output (RERR)

- RERR outputs an error flag when a PLL lock error or a data error occurs.
- It is possible to treat non-PCM data reception as an error by the RESEL setting.
- The RERR output conditions are set with RESTA. Since the PLL status can be output at all times, the PLL status can be always monitored, even when the clock source is XIN.

10.4.2 PLL lock error

- The PLL gets unlocked for input data that lost bi-phase modulation regularity, or input data for which preambles B, M, and W cannot be detected. However, even if preambles B, M, and W are detected if the timing does not conform to the IEC60958, the PLL get unlocked and processed. For example, period of preamble B is not every192 frames.
- RERR turns to “H” when the PLL lock error occurs and returns to “L” when the data demodulation returns normal and “H” is held for somewhere between 3ms to 144ms. This holding time is determined with the ERWT[1:0] setting.
- The rising and falling edges of RERR are synchronized with RLRCK.

10.4.3 Input data parity error

- Odd number of errors among parity bits in input data and input parity errors are detected.
- If an input parity error occurs 9 or more times in succession, RERR turns to "H" indicating that the PLL is locked, and after holding "H" for somewhere between 3ms and 144ms, it returns to "L".
- The error flag output format can be selected with REDER, when an input parity error is output less than 8 times in succession.

10.4.4 Other errors

- Even if RERR turns to "L", the channel status bits of 24 to 27 (sampling frequency) are always fetched and the data of the previous block is compared with the current data. Moreover, the input data sampling frequency is calculated from the fs clock extracted from the input data, and the fs calculated value is compared in a same way as described above. If any difference is detected in these data, RERR is instantly made "H" and the same processing as for PLL lock errors is carried out.
- The PLL causes a lock error when the fs changes as described above. However, in order to support sources with a variable fs (for example a CD player with a variable pitch function), it is possible to set with FSERR not to output an error flag unless fs changes exceeding the PLL capture range.

  In the FSERR setting, when the PLL is locked, RERR is turned to “L” without reflecting the fs calculation result to the error flag concerning input data within reception range by FSLIM [1:0].

  Moreover, the data comparison at the channel status bits of 24 to 27 as described above is not performed.
- If a setting which regard non-PCM data input as an error is made with RESEL, RERR turns to “H” when non-PCM data input is detected. At this time, the PLL locked status and various output clocks are subject to the input data, but the output data is muted.

10.4.5 Data processing upon occurrence of errors (lock error, parity error)

- The data processing upon occurrence of an error is described below. If 8 or fewer input parity errors occur in succession and transfer data is PCM audio data, the data is replaced by the one saved each in L-ch and R-ch in the previous frame. However, if the transfer data is non-PCM data, the error data is output as it is.
- Non-PCM data is the data of when bit 1 (audio sample word) of the channel status turns to "H" based on the data detected prior to the occurrence of the input parity error.
- Output data is muted when a PLL lock error occurs or a parity error occurs 9 or more times in succession.
- As for the channel status output, the data of the previous block is held in 1-bit units when a parity error occur 8 or fewer times in succession.

Table 10.6 Data Processing upon Error Occurrence

Data	PLL Lock Error	Input Parity Error (a)	Input Parity Error (b)	Input Parity Error (c)
Demodulation data	“L”	“L”	Previous value data	Output
fs calculation result	“L”	Output	Output	Output
Channel status	“L”	“L”	Previous value data	Previous value data

* Input parity error (a): If occurs 9 or more times in succession
* Input parity error (b): If occurs 8 or fewer times in succession, in case of audio data
* Input parity error (c): If occurs 8 or fewer times in succession, in case of non-PCM burst data

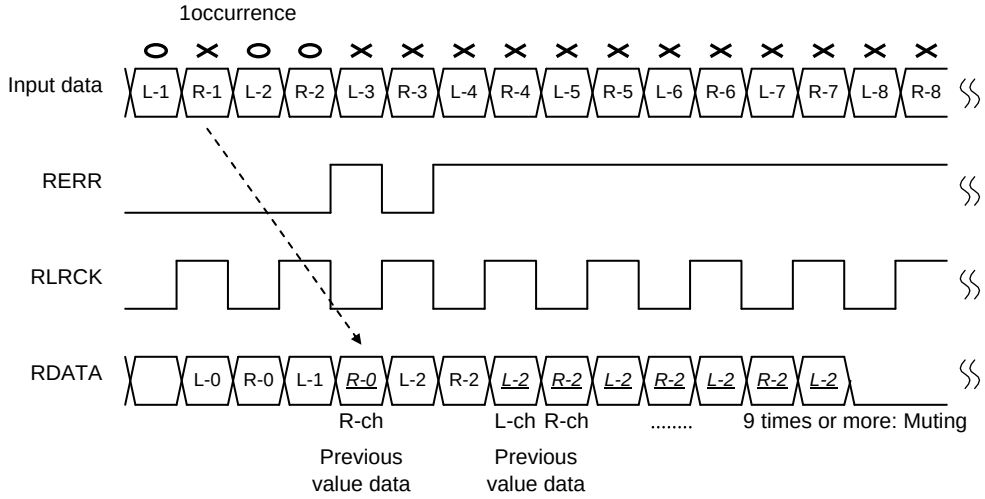


Figure 10.12 Example of Data Processing upon Parity Error Occurrence

10.4.6 Processing during error recovery

- When preambles B, M, and W are detected, PLL becomes locked and data demodulation begins.
- Demodulation data is output from the RLRCK edge after RERR turns to "L".

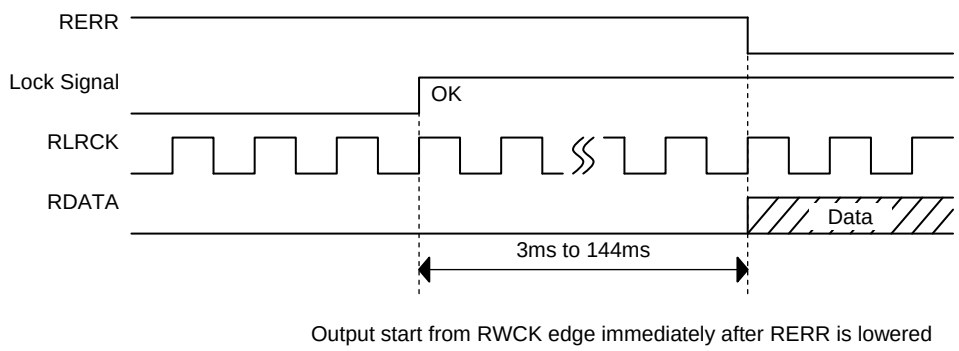


Figure 10.13 Data Processing When Data Demodulation Starts

10.5 Data Delimiter Bit 1 Output ($\overline{\text{AUDIO}}$)

- $\overline{\text{AUDIO}}$ outputs the channel status data delimiter bit 1 information.
- Outputs bit 1 of the channel status that indicates whether the input bi-phase data is PCM audio data. $\overline{\text{AUDIO}}$ is immediately output upon detection of RERR even during "H" output period.
- OR-output with IEC61937 or with the DTS-CD/LD detection flag is also possible with AOSEL.

Table 10.7 $\overline{\text{AUDIO}}$ Output

$\overline{\text{AUDIO}}$	Output Conditions
L	PCM audio data (CS bit 1 = "L")
H	Non-audio data (CS bit 1 = "H")

10.6 Emphasis Information Output (EMPHA)

- MOUT can output whether there is 50/15μs emphasis parameter for consumer by switching the contents of MOUT output by MOSEL.
- MOUT is immediately output upon detection of RERR even during "H" output.

Table 10.8 MOUT Output

MOUT	Output Conditions
L	No pre-emphasis
H	50/15μs pre-emphasis

10.7 IEC61937, DTS-CD/LD Detection Flag Output

- A function to output IEC61937 and DTS-CD/LD detection flag for non-PCM data is provided.
- DTS-CD/LD is compatible with "14-bit format."
- When bit 1 of channel status is non-PCM data, the IEC61937 sync signal is detected and detection flag is output. If bit 1 is PCM data, detection flag is not output.
- The DTS-CD/LD sync signal detection is done based on the sync pattern and the base frequency. The sync pattern is checked every 4096th frame, and the detection status is held until the sync pattern is no longer verified.
- The IEC61937 and DTS-CD/LD detection flags can be readout with the microcontroller interface in addition to output to the $\overline{\text{AUDIO}}$ pin by AOSEL. When the UNPCM non-PCM signal output setting is selected through the $\overline{\text{INT}}$ output contents setting, an interrupt signal is output from $\overline{\text{INT}}$ detecting an IEC61937 or DTS-CD/LD sync signal. Reading output register from this information can see details of Non-PCM signal. This information is used to read out the output register and identify the details of the non-PCM signal
- The detection flags are cleared when fs is changed or when a PLL lock error or data error occurs.

11 Description of General-purpose I/O Function (GPIO0, GPIO1, GPIO2, GPIO3)

11.1 Initial Settings

- When setting general-purpose I/Os for input, pull down $\overline{\text{INT}}$ with a 10kΩ resistors. When settings general-purpose I/Os for output, pull up $\overline{\text{INT}}$ with a 10kΩ resistor. See Chapter 9 for $\overline{\text{INT}}$ pin settings.
- If general-purpose I/Os are set to the output pin, the serial data input from the microcontroller interface is converted to parallel data and output from of GPIO0, GPIO1, GPIO2, and GPIO3.
- If general-purpose I/Os are set to the input pin, select one of the functions listed below with GPIOS.

(1) Store the parallel data input from the GPIO0, GPIO1, GPIO2, and GPIO3 in the internal register and readout the contents of that register through the microcontroller interface (GPIOS=0).
(2) Configure a 2-to-1 (4 bits wide) selector that selects either the audio format data and clock that are input to the GPIO0, GPIO1, GPIO2, and GPIO3 pins, or data and clock demodulated by the DIR block.
RMCK, RBCK, RLRCK, and RDATA are the outputs from the selector (GPIOS=1).

11.2 Output Function

- The data output directed to the GPIO0, GPIO1, GPIO2, and GPIO3 are stored at CCB address 0xE8, command address 10, input register bits DI12 to DI15, or register PI[3:0].
- The data stored in PI[3:0] are transmitted out of the GPIO0, GPIO1, GPIO2, and GPIO3 pins.

11.3 Input Function

11.3.1 GPIOS=0

- The data input to the GPIO0, GPIO1, GPIO2, and GPIO3 are taken into CCB address 0xEB, output register bits DO0 to DO3, or register PO[3:0].
- The data must be readout by setting the interrupt source GPIO to $\overline{\text{INT}}$ or at an arbitrary timing. The way in which the data is taken into the register depends on how it is readout.

11.3.1.1 GPIO=1 (using $\overline{\text{INT}}$)

(1) XIN must always be given the specified clock and set in continuous operating mode (default).
(2) The data inputs to the GPIO0, GPIO1, GPIO2, and GPIO3 are taken into the register on a 24kHz clock.
(3) When the state of one of the data inputs changes, $\overline{\text{INT}}$ turns to “L” and suspends the data transfer to the register.
(4) The interrupt sources for CCB address 0xEA, output register DO14, and register OGPIO must be verified.
(5) $\overline{\text{INT}}$ turns “H” and the data is held in the register immediately when address 0xEA is readout.
(6) The read data from the PO[3:0] is transferred to the microcontroller. At the same time, the data in the register is cleared.
(7) The contents of the register are updated if $\overline{\text{INT}}$ turns to “L” before P0[3:0] is readout.

11.3.1.2 GPIO=0 (not using $\overline{\text{INT}}$)

(1) The data inputs to the GPIO0, GPIO1, GPIO2, and GPIO3 pins are taken in when the CCB address 0xEB is set.
(2) The data read from the PO[3:0] is transferred to the microcontroller. At the same time, the data in the register is cleared.

11.3.2 GPIOS=1

- The figure below shows the relationship between GPIO0, GPIO1, GPIO2, GPIO3 which are input to the selector and the DIR block signal, and RMCK, RBCK, RLRCK, RDATA which are output from the selector and the control signal.

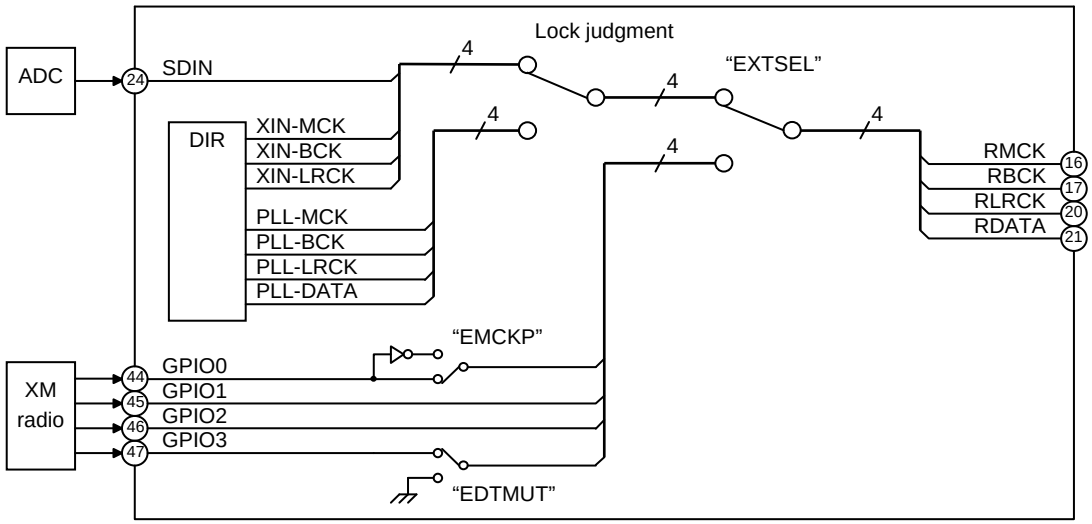


Figure 11.1 Selector Configuration Diagram

Table 11.1 Selector I/O Signals

Input Pin or Input Signal			Output pin
EXTSEL=1	EXTSEL=0		
	PLL Lock State	PLL Unlock State	
GPIO0 (pin 44)	PLL-MCK	XIN-MCK	RMCK (pin 16)
GPIO1 (pin 45)	PLL-BCK	XIN-BCK	RBCK (pin 17)
GPIO2 (pin 46)	PLL-LRCK	XIN-LRCK	RLRCK (pin 20)
GPIO3 (pin 47)	PLL-DATA	SDIN	RDATA (pin 21)

Note: The selector output generated when the PLL is locked can be changed to the XIN clock system by setting the OCKSEL and RCSEL.

- EXTSEL is enabled by setting GPIOS=1. When GPIOS=0 is set, the state of EXTSEL=0 is output from each pin.
- The clock input to GPIO0 can be inverted by EMCKP and sent to RMCK.
- The data to be input to GPIO3 must conform to the PLL-DATA or SDIN audio format.
- The data input to GPIO3 can be muted by EDTMUT.
- EMCKP and EDTMUT are enabled when GPIOS=1 is set.
- The above settings are valid only when the master mode is set and must not be set when the slave mode is set.

12. Microcontroller Interface ($\overline{\text{INT}}$, CL, CE, DI, DO)

12.1 Description of Microcontroller Interface

12.1.1 Interrupt output ($\overline{\text{INT}}$)

- Interrupts is output when a change has occurred in the PLL lock status or output data information.
- Interrupt output consists of the register for selecting the interrupt source, the $\overline{\text{INT}}$ pin that outputs that state transition, and the registers that store the interrupt source data.
- Normally $\overline{\text{INT}}$ is held “H” and output “L” upon occurrence of an interrupt. Following “L” output, it is cleared and returns to “H” immediately when the interrupt source output register is readout.
- The interrupt sources can be selected among the following items. Multiple sources can be selected at the same time with the contents of CCB address 0xE8 and command address 8. $\overline{\text{INT}}$ outputs OR calculation result of the selected interrupt sources.

$\overline{\text{INT}}$ output = (selected source 1) + (selected source 2) + ··· + (selected source n)

Table 12.1 Interrupt Source Setting Contents

No.	Command Name	Description
1	ERROR	Output when RERR pin status has changed
2	INDET	Output when input data pin status has changed (subject to oscillation amplifier operation condition)
3	FSCHG	Output when input fs calculation result has changed. (subject to oscillation amplifier condition)
4	CSRNW	Output when channel status data of first 48 bits have updated
5	UNPCM	Output when $\overline{\text{AUDIO}}$ pin status has changed
6	PCRNW	Output when burst preamble Pc has been updated
7	GPIO	Output when the state of input data changes when the general-purpose I/O parallel input is set.
8	EMPF	Output when emphasis information has changed

- The contents of set interrupt source are saved in output registers DO8 to DO15 of CCB address 0xEA, when the source occurs. However, for the read registers for source items 1 and 5, the each status of the RERR and $\overline{\text{AUDIO}}$ pins are output at the time of reading. Other data except for source items 1 and 5 are saved in the registers upon occurrence of an interrupt source.
- Concerning source items 2 and 3, the oscillation amplifier clock is used. Therefore, if the status is monitored even while the PLL is locked, the oscillation amplifier must be set to the continuous operation mode.
- Clearing $\overline{\text{INT}}$ at the same time of readout of an output register is carried out immediately after the output register 0xEA is set. However, $\overline{\text{INT}}$ is not cleared other than the 0xEA setting.

12.1.2 CCB interface

- The CCB interface is a Our original serial bus format based on LSB-first communication, but three-state is employed instead of open-drain for the data output format of LC89058W-E.
- Data input/output is performed following CCB address input. The same CCB address cannot be used for both read and write operation.

Table 12.2 Relationship between Register I/O Contents and CCB Addresses

Register I/O contents	R/W	CCB address	B0	B1	B2	B3	A0	A1	A2	A3
Function setting data input	Write	0xE8	0	0	0	1	0	1	1	1
Input detection, interrupt output	Read	0xEA	0	1	0	1	0	1	1	1
fs data output	Read	0xEB	1	1	0	1	0	1	1	1
CS data output	Read	0xEC	0	0	1	1	0	1	1	1
Pc data output	Read	0xED	1	0	1	1	0	1	1	1

12.1.3 Data write procedure

- Input is performed in the following sequence: CCB addresses of A0 to A3 and B0 to B3, chip addresses of DI0 and DI1, command addresses of DI4 to DI7, and data of DI8 to DI15. DI2 and DI3 are reserved for the system. So, DI2 and DI3 input must be doing "0".
- For the chip addresses, DI0 corresponds to CAL (low-order), and DI1 to CAU (high-order). For details, see section 9.2.

12.1.4 Data read procedure

- Read data is output from DO. DO is in the high impedance state when CE is "L", and begins outputting from the rising edge of CE after output setting is established at the CCB address. DO then returns to the high impedance state at the falling edge of CE.
- If DO outputs are shared using multiple LC89058W-E units, it is possible to set the DO outputs of the LC89058W-E units of which data is not to be read to be always in the high impedance state with DOEN. With this setting, only the targeted outputs can be read.

12.1.5 Points to notices when normal H clock is used

- The CCB interface uses CL of a normal L clock, and it is also possible to use CL of a normal H clock. However, input the clock based on CCB microcontroller interface AC characteristics.
- CL is lowered before CE is raised when data reads.

12.1.6 I/O timing

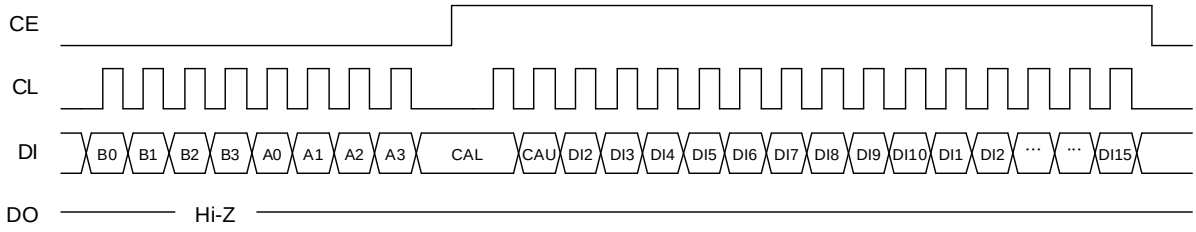


Figure 12.1 Input Timing Chart (Normal L clock)

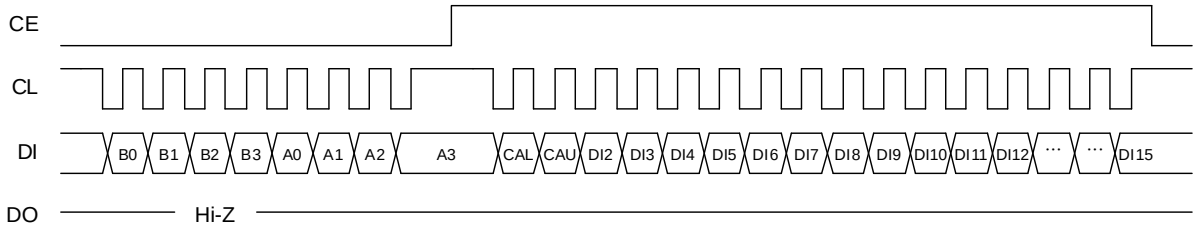


Figure 12.2 Input Timing Chart (Normal H clock)
(CL need not be lowered before CE is raised.)

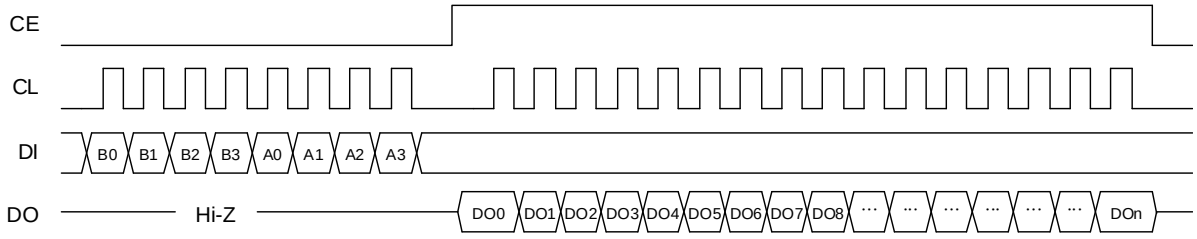


Figure 12.3 Output Timing Chart (Normal L clock)

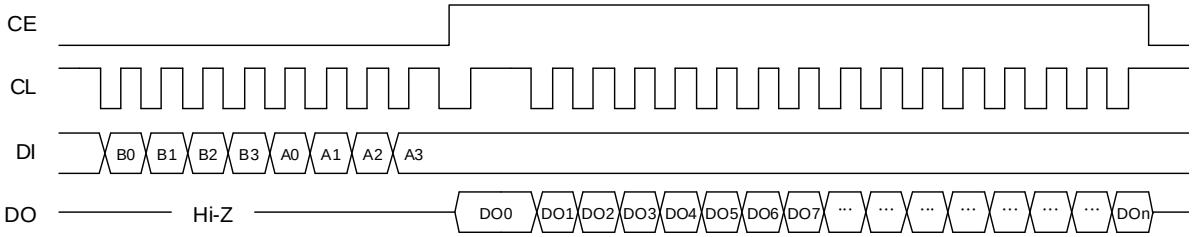


Figure 12.4 Output Timing Chart (Normal H clock)
(CL is lowered before CE is raised, and DO0 need be read with port)

12.2 Write Data

12.2.1 List of write commands

• A list of the write commands is shown below.
• To write the commands shown in the following table, set the CCB address to 0xE8.

Table 12.3 Write Register Map

Add.	Setting Items	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	System setting 1	TESTM	0	0	0	0	0	DOEN	SYSRST
1	System setting 2	0	0	FSLIM1	FSLIM0	RXMON	AOSEL	0	MOSEL
2	Master clock	AMPOPR1	AMPOPR0	0	PLLOPR	XMSEL1	XMSEL0	XINSEL	0
3	R system output clock	XRLRCK1	XRLRCK0	XRBCK1	XRBCK0	XRSEL1	XRSEL0	PRSEL1	PRSEL0
4	S system output clock	XSLRCK1	XSLRCK0	XSBCK1	XSBCK0	PSLRCK1	PSLRCK0	PSBCK1	PSBCK0
5	Source switch	0	RDTMUT	RDTSTA	RDTSEL	0	0	OCKSEL	0
6	Data I/O 1	0	ROSEL2	ROSEL1	ROSEL0	0	RISEL2	RISEL1	RISEL0
7	Output format	SLRCKP	SBCKP	RLRCKP	RBCKP	0	0	0	OFDSEL
8	$\overline{\text{INT}}$source selection	EMPF	GPIO	PCRNW	UNPCM	CSRNW	FSCHG	INDET	ERROR
9	RERR condition setting	ERWT1	ERWT0	FSERR	RESTA	0	0	REDER	RESEL
10	General-purpose I/O	PI3	PI2	PI1	PI0	0	0	0	0
11	TEST	0	0	0	0	0	0	0	0
12	System setting 3	0	0	CKSTP	RMCKP	0	PLLDV1	PLLDV0	PLLACC
13	Data I/O 2	0	RXSEL2	RXSEL1	RXSEL0	EDTMUT	EMCKP	EXTSEL	GPIOS
14	PLL clock	FSSEL1	FSSEL0	0	0	PTOXW1	PTOXW0	0	0
15	TEST	0	0	0	0	0	0	0	0

Addr: Command address

• The shaded parts of DI8 to DI15 in the command area are reserved bits. Input must be doing "0".
• Command addresses 11 and 15 are reserved for testing purposes. Writing to these addresses is prohibited.

12.2.2 Details of write commands

CCB address: 0xE8; Command address: 0; System setting 1

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	0	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
TESTM	0	0	0	0	0	DOEN	SYSRST

SYSRST System reset
- 0: Don't reset (initial value)
- 1: Reset circuits other than command registers

DOEN DO pin output setting
- 0: Output (initial value)
- 1: Always high impedance state (read disabled)

TESTM Test mode setting
- 0: Normal operation (initial value)
- 1: Enter test mode

• When reset by SYSRST is performed, RBCK outputs “L” and BLRCK outputs “H.”

CCB address: 0xE8; Command address: 1; System setting 2

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	0	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	0	FSLIM1	FSLIM0	RXMON	AOSEL	0	MOSEL

MOSEL MOUT output contents setting
- 0: Output channel status emphasis information (initial value)
- 1: Output input data fs calculation results (output conditions are given by FSSEL[1:0].)

AOSEL $\overline{\text{AUDIO}}$ output mode
- 0: Only output channel status bit 1 (initial value)
- 1: Output channel status bit 1, IEC61937 or DTS-CD/LD detection flag

RXMON Setting digital audio data (S/PDIF) input status monitoring
- 0: Don’t monitor S/PDIF input status (initial value).
- 1: Monitor S/PDIF input status

FSLIM[1:0] Setting of sampling frequency reception range for input digital signal
- 00: No limit (initial value)
- 01: fs≤96kHz (when exceeded, data is muted and clock is set to XIN system output)
- 10: fs≤48kHz (when exceeded, data is muted and clock is set to XIN system output)
- 11: Reserved

CCB address: 0xE8; Command address: 2; Master clock setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	1	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
AMPOPR1	AMPOPR0	0	PLLOPR	XMSEL1	XMSEL0	XINSEL	0

XINSEL XIN input frequency setting
- 0: 12.288MHz (initial value)
- 1: 24.576MHz

XMSEL [1:0] XMCK output frequency setting
- 00: 1/1 of XIN input frequency (initial value)
- 01: 1/2 of XIN input frequency
- 10: 1/4 of XIN input frequency
- 11: Muted

PLLOPR PLL (VCO) operation setting
- 0: Operate (initial value)
- 1: Stop

AMPOPR [1:0] Oscillation amplifier operation setting
- 00: Permanent continuous operation (initial value)
- 01: Reserved
- 10: Automatic stopping of oscillation amplifier while PLL is locked
- 11: Stop

- In order to replace LC89057W-VF4A-E, setting contents of the AMPOPR[1:0] are different from those of LC89057W-VF4A-E.

CCB address: 0xE8; Command address: 3; R system output clock setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	1	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
XRLRCK1	XRLRCK0	XRBCK1	XRBCK0	XRSEL1	XRSEL0	PRSEL1	PRSEL0

PRSEL [1:0] Setting of RMCK output frequency while PLL is locked
(enabled when PLLACC is set to “0”)
00: 512fs×1/2 (256fs) (initial value)
01: 512fs×1/1 (512fs)
10: 512fs×1/4 (128fs)
11: Muted

XRSEL [1:0] Setting of RMCK output frequency during XIN source
00: 1/1 of XIN input frequency (initial value)
01: 1/2 of XIN input frequency
10: 1/4 of XIN input frequency
11: Muted

XRBCK [1:0] Setting of RBCK output frequency during XIN source
00: 3.072MHz output (RMCK≥6.144MHz) (initial value)
01: 6.144MHz output (RMCK≥12.288MHz)
10: 12.288MHz output (RMCK=24.576MHz)
11: Muted

XRLRCK [1:0] Setting of RLRCK output frequency during XIN source
00: 48kHz output (initial value)
01: 96kHz output
10: 192kHz output
11: Muted

- Don’t do the setting to which RMCK=3.072MHz is output by XRSEL [1:0]=10(1/4 output) setting when XIN=12.288MHz is input because it doesn't satisfy the output setting condition of RBCK and SBCK.
- Setting of XRBCK [1:0] relate to setting of RMCK output clock. RBCK output clock is set to become 1/2 or less of RMCK output clock at XIN source.

CCB address: 0xE8; Command address: 4; S system output clock setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	1	0	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
XSLRCK1	XSLRCK0	XSBCK1	XSBCK0	PSLRCK1	PSLRCK0	PSBCK1	PSBCK0

PSBCK [1:0] Setting of SBCK frequency while PLL is locked
- 00: 64fs output (initial value)
- 01: 128fs output
- 10: 32fs output
- 11: 16fs output

PSLRCK [1:0] Setting of SLRCK frequency while PLL is locked
- 00: fs output (initial value)
- 01: 2fs output
- 10: fs/2 output
- 11: fs/4 output

XSBCK [1:0] Setting of SBCK frequency during XIN source
- 00: 3.072MHz output (RMCK≥6.144MHz) (initial value)
- 01: 6.144MHz output (RMCK≥12.288MHz)
- 10: 12.288MHz output (RMCK=24.576MHz)
- 11: Muted

XSLRCK [1:0] SLRCK output frequency setting during XIN source
- 00: 48kHz output (initial value)
- 01: 96kHz output
- 10: 192kHz output
- 11: Muted

- Setting of XSBCK [1:0] relate to setting of RMCK output clock. SBCK output clock is set to become 1/2 or less of RMCK output clock at XIN source.

CCB address: 0xE8; Command address: 5; Clock source switching; RDATA output setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	1	0	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	RDTMUT	RDTSTA	RDTSEL	0	0	OCKSEL	0

OCKSEL Clock source setting
- 0: Use XIN clock as source while PLL is unlocked (initial value)
- 1: Use XIN clock as source regardless of PLL status

RDTSEL RDATA output setting while PLL is unlocked
- 0: Output SDIN data while PLL is unlocked (initial value)
- 1: Mute while PLL is unlocked

RDTSTA RDATA output setting
- 0: According to RDTSEL (initial value)
- 1: Output SDIN input data regardless of PLL status

RDTMUT RDATA mute setting
- 0: Output data selected with RDTSEL (initial value)
- 1: Muted

- When the oscillation amplifier is set to the permanent continuous operation mode with AMPOPR [1:0] or fs changes are set not to be reflected to the error flag with FSERR, OCKSEL can switch the clock source while maintaining the RERR status.
- The phase of R system clock and S system clock synchronize.
- To input data to SDIN, select a clock synchronized with the SDIN input data.
- The XIN source can be switched while maintaining the PLL locked status. However, since switching between clock and data output can be set independently; it is recommended to select mute or SDIN data for the output data when XIN source is switched.
- If the oscillation amplifier is set to stop automatically when the PLL gets locked, XIN source switching from the PLL locked status disables the clock output. Be sure to set the oscillation amplifier to the continuous operation mode when switching the clock source to the XIN source.

CCB address: 0xE8; Command address: 6; Data I/O setting 1

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	1	1	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	ROSEL2	ROSEL1	ROSEL0	0	RISEL2	RISEL1	RISEL0

RISEL [2:0] Data demodulation input pin setting

000: RX0 selection (initial value)
001: RX1 selection
010: RX2 selection
011: RX3 selection
100: RX4 selection
101: RX5 selection
110: RX6 selection
111: None are selected (all inputs are connected to GND through pull-down resistors.)

ROSEL [2:0] RXOUT1 output data setting

000: RX0 input data (initial value)
001: RX1 input data
010: RX2 input data
011: RX3 input data
100: RX4 input data
101: RX5 input data
110: RX6 input data
111: “L” fixed output

CCB address; 0xE8; Command address: 7; Data output format setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	1	1	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
SLRCKP	SBCKP	RLRCKP	RBCKP	0	0	0	OFDSEL

OFSEL Audio data output format setting
- 0: I^2S data output (initial value)
- 1: 24 bits, MSB first, left-justification output

RBCKP RBCK output polarity setting
- 0: Falling RDATA data change (initial value)
- 1: Rising RDATA data change

RLRCKP RLRCK output polarity setting
- 0: "L" period: L-channel data; "H" period: R-channel data (initial value)
- 1: "L" period: R-channel data; "H" period: L-channel data

SBCKP SBCK output polarity setting
- 0: Falling RDATA data change (initial value)
- 1: Rising RDATA data change

SLRCKP SLRCK output polarity setting
- 0: "L" period: L-channel data; "H" period: R-channel data (initial value)
- 1: "L" period: R-channel data; "H" period: L-channel data

CCB address: 0xE8; Command address: 8; $\overline{INT}$ output contents setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	0	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
EMPF	GPIO	PCRNW	UNPCM	CSRNW	FSCHG	INDET	ERROR

ERROR RERR signal output setting
- 0: Don't output (initial value)
- 1: Output RERR pin status change

INDET Input data detection output setting
- 0: Don't output (initial value)
- 1: Output input data pin status change

FSCHG Setting of updated flag output of PLL lock frequency calculation result
- 0: Don't output (initial value)
- 1: Output updated flag of PLL lock frequency calculation result

CSRNW Output setting for updated flag of first 48-bit channel status data
- 0: Don't output (initial value)
- 1: Output update flag of first 48-bit channel status data

UNPCM Output setting for change flag of non-PCM data detection
- 0: Don't output (initial value)
- 1: Output $\overline{AUDIO}$ pin status change

PCRNW Output setting for updated flag of burst preamble Pc
- 0: Don't output (initial value)
- 1: Output updated flag of burst preamble Pc

GPIO Input data updated flag output setting when general-purpose I/O parallel input is set (GPIOS=0)
- 0: Don't output (initial value)
- 1: Output input data updated flag

EMPF Output setting of emphasis detection flag
- 0: Don't output (initial value)
- 1: Output emphasis detection flag

- The input data detection output setting functions when INDET=1 is set with the clock of 24.576MHz is supplied to the terminal XIN (XINSEL=1) and digital data input state monitoring function (RXMON=1) made effective.
- The channel status update flag compares the first 48 bits of data of the previous block with those of the current block. If these data are identical, it outputs a flag, considering the data has been updated.
- The burst preamble Pc update flag also compares the 16 bits of data of the previous block with those of the current data. If they are identical, an update flag is output.
- The 4-bit input data updated flag when the general-purpose I/O parallel input is set, is output only when a change has occurred in the sampling data with a clock of 24kHz.

CCB address: 0xE8, Command address: 9; RERR output setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	0	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
ERWT1	ERWT0	FSERR	RESTA	0	0	REDER	RESEL

RESEL RERR output contents setting
- 0: PLL lock error or data error (initial value)
- 1: PLL lock error or data error or non-PCM data

REDER Setting of parity error flag output within 8 times in a row
- 0: Output only when non-PCM data is recognized (initial value)
- 1: Output only during sub-frame for which error was generated

RESTA RERR output condition setting
- 0: Output PLL status all the time (Output PLL status even during XIN source) (initial status)
- 1: Forcibly output error (Set "H" to RERR forcibly)

FSERR Setting of error flag output condition according to fs change
- 0: Reflect fs changes to error flag (initial value)
- 1: Don't reflect fs changes to error flag

ERWT [1:0] Setting of RERR wait time after PLL is locked
- 00: Cancel error after preamble B is counted 3 (initial value)
- 01: Cancel error after preamble B is counted 24
- 10: Cancel error after preamble B is counted 12
- 11: Cancel error after preamble B is counted 6

- Non-PCM data is identical to the detection data output to $\overline{\text{AUDIO}}$.
- Output data is muted if an error occurs due to non-PCM data with RESEL.
- The RESTA setting is not reflected to the output pins of data and clock.
- For FSERR, the fs calculation result obtained while the oscillation amplifier is stopped is not reflected. In this case, fs changes consist of only channel status fs information.
- ERWT[1:0] defines the interval of time for RERR to output error cancellation ("L") after PLL is locked. Since demodulated audio data is output after RERR cancels an error, you need to change this setting if the situation that the head of data is missing is a problem.

CCB address: 0xE8; Command address: 10; General-purpose I/O function

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	1	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
PI3	PI2	PI1	PI0	0	0	0	0

PI0 Contents of data output to the GPIO0 pin when the general-purpose I/O parallel output is set
0: L (initial value)
1: H

PI1 Contents of data output to the GPIO1 pin when the general-purpose I/O parallel output is set
0: L (initial value)
1: H

PI2 Contents of data output to the GPIO2 pin when the general-purpose I/O parallel output is set
0: L (initial value)
1: H

PI3 Contents of data output to the GPIO3 pin when the general-purpose I/O parallel output is set
0: L (initial value)
1: H

CCB address: 0xE8; Command address: 11; System settings 3

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	1	0	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	0	CKSTP	RMCKP	0	PLLDV1	PLLDV0	PLLACC

PLLACC PLL clock lock frequency setting
- 0: Manual setting (initial value)
- 1: Automatic control (see 10.1.6.)

PLLDV0 Set the PLL clock generated when 32kHz, 44.1kHz or 48kHz is received with PLLACC=1
- 0: 512fs output (initial value)
- 1: 256fs output

PLLDV1 Set the PLL clock generated when 88.2kHz or 96kHz is received with PLLAC=1
- 0: 256fs output (initial value)
- 1: 512fs output

RMCKP DIR block RMCK output setting
- 0: Normal output (initial value)
- 1: Inverted output

CKSTP CKST output polarity setting
- 0: Normal high output (initial value)
- 1: Normal low output

CCB address: 0xE8; Command address: 12; Data I/O setting 2

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	1	0	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	RXSEL2	RXSEL1	RXSEL0	EDTMUT	EMCKP	EXTSEL	GPIOS

GPIOS Setting of pins 44 to 47 input function (when $\overline{\text{INT}}$ pull-down is set)
- 0: General-purpose I/O parallel input (initial value)
- I: Selector input

EXTSEL RMCK, RBCK, RLRCK, and RDATA output setting
- 0: Output data and clock of DIR function (initial value).
- 1: Output input signals to GPIO0, GPIO1, GPIO2, GPIO3 (GPIOS=1)

EMCKP GPIO0 output polarity setting (GPIOS=1)
- 0: Normal output (Initial value)
- 1: Inverted output

EDTMUT GPIO3 mute setting (GPIOS=1)
- 0: Normal output (initial value)
- 1: Muted

RXSEL[2:0] RXOUT2 output data setting
- 000: "L" fixed output (initial value)
- 001: RX0 input data
- 010: RX1 input data
- 011: RX2 input data
- 100: RX3 input data
- 101: RX4 input data
- 110: RX5 input data
- 111: RX6 input data

- GPIOS setting is needed when RMCK, RBCK, RLRCK, and RDATA output are changed with EXTSEL.
- RMCK, RBCK, RLRCK, and RDATA output don't change even if it sets to EXTSEL=1 in the state of GPIOS=0.

CCB address: 0xE8; Command address: 13; PLL clock

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	1	1	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
FSSEL1	FSSEL0	0	0	PTOXW1	PTOXW0	0	0

PTOXW[1:0] Setting of clock switch wait time

00: Clock switching after 2.67ms from when the PLL lock status is identified (initial value)
01: Clock switching after 1.33ms from when the PLL lock status is identified
10: Clock switching after 0.67ms from when the PLL lock status is identified
11: Clock switching after when the PLL lock status is identified

FSSEL[1:0] MOUT output contents setting (output “L” when PLL unlock status or when a value other than those listed below is calculated)

00: Output “H” when 32kHz/44.1kHz/48kHz is calculated (Initial value)
01: Output “H” when 64kHz/88.2kHz/96kHz is calculated
10: Output “H” when 128kHz/176.4kHz/192kHz is calculated
11: Output “H”when 64kHz/88.2kHz/96kHz or higher is calculated

12.3 Read Data

12.3.1 List of read commands

• It is possible to read the following items.
  – Interrupt data output
  – Monitor output of digital data input status
  – Input data output when general-purpose I/O parallel input mode is set
  – Output of fs calculation result
  – Output of first 48 bits of channel status
  – Output of burst preamble Pc data

Table 12.4 Read Register Map

	0xEA	0xEB	0xEC	0xED
DO0	RXDET0	PO0	CS bit0	Pc bit0
DO1	RXDET1	PO1	CS bit1	Pc bit1
DO2	RXDET2	PO2	CS bit2	Pc bit2
DO3	RXDET3	PO3	CS bit3	Pc bit3
DO4	RXDET4	FSC0	CS bit4	Pc bit4
DO5	RXDET5	FSC1	CS bit5	Pc bit5
DO6	RXDET6	FSC2	CS bit6	Pc bit6
DO7	0	FSC3	CS bit7	Pc bit7
DO8	OERROR	-	CS bit8	Pc bit8
DO9	OINDET	-	CS bit9	Pc bit9
DO10	OFSCHG	-	CS bit10	Pc bit10
DO11	OCSRNW	-	CS bit11	Pc bit11
DO12	OUNPCM	-	CS bit12	Pc bit12
DO13	OPCRNW	-	CS bit13	Pc bit13
DO14	OGPIO	-	CS bit14	Pc bit14
DO15	OEMPF	-	CS bit15	Pc bit15
DO16	CSBIT1	-	CS bit16	-
DO17	IEC1937	-	CS bit17	-
DO18	DTS51	-	CS bit18	-
DO19	DTSES	-	CS bit19	-
DO20	0	-	CS bit20	-
DO21	0	-	CS bit21	-
DO22	0	-	CS bit22	-
DO23	0	-	CS bit23	-
DO24	-	-	CS bit24	-
DO25	-	-	CS bit25	-
DO26	-	-	CS bit26	-
…	…	…	…	…
…	…	…	…	…
DO45	-	-	CS bit45	-
DO46	-	-	CS bit46	-
DO47	-	-	CS bit47	-

12.3.2 Read register 0xEA (S/PDIF input detection, interrupt flag) output

CCB address: 0xEA, Contents of read register output 1

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
0	RXDET6	RXDET5	RXDET4	RXDET3	RXDET2	RXDET1	RXDET0

RXDET0 RX0 input detection
- 0: No input data in RX0
- 1: Input data exist in RX0

RXDET1 RX1 input detection
- 0: No input data in RX1
- 1: Input data exist in RX1

RXDET2 RX2 input detection
- 0: No input data in RX2
- 1: Input data exist in RX2

RXDET3 RX3 input detection
- 0: No input data in RX3
- 1: Input data exist in RX3

RXDET4 RX4 input detection
- 0: No input data in RX4
- 1: Input data exist in RX4

RXDET5 RX5 input detection
- 0: No input data in RX5
- 1: Input data exist in RX5

RXDET6 RX6 input detection
- 0: No input data in RX6
- 1: Input data exist in RX6

• For readout of RXDET[10:0], RXMON must be set to "1" beforehand.

CCB address; 0xEA; Contents of read register output 2

DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8
OEMPF	OGPIO	OPCRNW	OUNPCM	OCSRNW	OFSCHG	OINDET	OERROR

OERROR RERR output (Output status during readout)
- 0: No transfer error while PLL is locked
- 1: Transfer error exists or PLL is unlocked

OINDET Status change of data input pin (clear after readout)
- 0: No change in status of data input pin
- 1: Change exists in status of data input pin

OFSCHG Result of updating input fs calculation (clear after readout)
- 0: No update of input fs calculation
- 1: Input fs calculation is updated

OCSRNW Update result of first 48 bits channel status (clear after readout)
- 0: Not updated
- 1: Updated

OUNPCM $\overline{\text{AUDIO}}$ output (output of status during readout)
- 0: Non-PCM signal not detected
- 1: Non-PCM signal detected

OPCRNW Update result of burst preamble Pc (clear after readout)
- 0: Not updated
- 1: Updated

OGPIO Update result of input date when the general-purpose I/O parallel input mode is set (GPIOS=0) (clear after readout)
- 0: Not updated
- 1: Updated

OEMPF Channel status emphasis detection (output of status during readout)
- 0: No pre-emphasis
- 1: 50/15μs pre-emphasis exists

• Concerning OERROR and OUNPCM, the status of RERR and $\overline{\text{AUDIO}}$ that are subject to RESEL setting are read regardless of the $\overline{\text{INT}}$output setting.

CCB address: 0xEA; Contents of read register output 3

DO23	DO22	DO21	DO20	DO19	DO18	DO17	DO16
0	0	0	0	DTSES	DTS51	IEC1937	CSBIT1

CSBIT1 Channel status bit 1 detection
- 0: PCM
- 1: Non-PCM

IEC1937 IEC61937 burst preamble detection
- 0: Pa, Pb not detected
- 1: Pa, Pb detected

DTS51 DTS-CD/LD 5.1 channel sync signal detection
- 0: DTS-CD/LD sync signal not detected
- 1: DTS-CD/LD sync signal detected

DTSES DTS ES-CD/LD 6.1 channel sync signal detection
- 0: DTS ES-CD/LD sync signal not detected
- 1: DTS ES-CD/LD sync signal detected

12.3.3 Read register 0xEB (General-purpose I/O parallel input contents, fs calculation results) output

CCB address: 0xEB, Contents of read register output

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
FSC3	FSC2	FSC1	FSC0	PO3	PO2	PO1	PO0

PO0 Contents input to the GPIO0 pin when the general-purpose I/O parallel input mode is set (GPIOS=0).
0: L
1: H

PO1 Contents input to the GPIO1 pin when the general-purpose I/O parallel input mode is set (GPIOS=0).
0: L
1: H

PO2 Contents input to the GPIO2 pin when the general-purpose I/O parallel input mode is set (GPIOS=0).
0: L
1: H

PO3 Contents input to the GPIO3 pin when the general-purpose I/O parallel input mode is set (GPIOS=0).
0: L
1: H

FSC [3:0] Input data fs calculation result
"xxxx": See code table.

Table 12.5 Code Table of Input fs Calculation Result (Ta = 25°C, AV_{DD} = DV_{DD} = 3.3 V)

FSC3	FSC2	FSC1	FSC0	Target Frequency
0	0	0	0	Out of range
0	0	0	1	-
0	0	1	0	-
0	0	1	1	-
0	1	0	0	-
0	1	0	1	-
0	1	1	0	-
0	1	1	1	32kHz
1	0	0	0	44.1kHz
1	0	0	1	48kHz
1	0	1	0	64kHz
1	0	1	1	88.2kHz
1	1	0	0	96kHz
1	1	0	1	128kHz
1	1	1	0	176.4kHz
1	1	1	1	192kHz

12.3.4 Read register 0xEC (Readout of first 48 bits of channel status) output

- The first 48bits of channel status can be read.
- The readout channel status data is output with LSB first.
- For readout, set the CCB address to 0xEC.
- The channel status data cannot be updated after the CCB address is set.
- The relation between the read registers and the channel status data is shown below.

Table 12.6 Read Registers of First 48 bits of Channel Status

Register	Bit No.	Contents
DO0	Bit 0	Application
DO1	Bit 1	Control
DO2	Bit 2	
DO3	Bit 3	
DO4	Bit 4	
DO5	Bit 5	
DO6	Bit 6	Not defined
DO7	Bit 7	
DO8	Bit 8	Category code
DO9	Bit 9	
DO10	Bit 10	
DO11	Bit 11	
DO12	Bit 12	
DO13	Bit 13	
DO14	Bit 14	
DO15	Bit 15	
DO16	Bit 16	Source number
DO17	Bit 17	
DO18	Bit 18	
DO19	Bit 19	
DO20	Bit 20	Channel number
DO21	Bit 21	
DO22	Bit 22	
DO23	Bit 23	

Register	Bit No.	Contents
DO24	Bit 24	Sampling frequency
DO25	Bit 25	
DO26	Bit 26	
DO27	Bit 27	
DO28	Bit 28	Clock accuracy
DO29	Bit 29	
DO30	Bit 30	Not defined
DO31	Bit 31	
DO32	Bit 32	Word length
DO33	Bit 33	
DO34	Bit 34	
DO35	Bit 35	
DO36	Bit 36	Not defined
DO37	Bit 37	
DO38	Bit 38	
DO39	Bit 39	
DO40	Bit 40	
DO41	Bit 41	
DO42	Bit 42	
DO43	Bit 43	
DO44	Bit 44	
DO45	Bit 45	
DO46	Bit 46	
DO47	Bit 47	

12.3.5 Read register 0xED (Burst preamble Pc data) output

- The burst preamble Pc data can be read with the demodulation function.
- The 16 bit-data of burst preamble Pc are output with LSB first.
- For readout, set the CCB address to OxED.
- The relation between the read register and burst preamble Pc data is shown below.

Table 12.7 Burst Preamble Pc Read Registers

Register	Bit No.	Contents
DO0	Bit 0	Data type
DO1	Bit 1	
DO2	Bit 2	
DO3	Bit 3	
DO4	Bit 4	
DO5	Bit 5	Reserved
DO6	Bit 6	
DO7	Bit 7	Error
DO8	Bit 8	Data type dependent
DO9	Bit 9	Information
DO10	Bit 10	
DO11	Bit 11	
DO12	Bit 12	
DO13	Bit 13	Bit stream number
DO14	Bit 14	
DO15	Bit 15	

12.3.6 Burst Preamble Pc Field

• The burst preamble Pc field is shown below.
• For the latest information, refer to official specifications.

Table 12.8 Burst Preamble Pc Field

Register	Value	Contents
DO4 to 0	0	NULL data
	1	Dolby AC-3 data
	2	Reserved
	3	Pause
	4	MPEG-1, layer 1 data
	5	MPEG-1, layer 2, 3 data, or non-extended MPEG-2
	6	Extended MPEG-2 data
	7	Reserved
	8	MPEG-2, layer 1, low sampling rate
	9	MPEG-2, layer 2, 3, low sampling rate
	10	Reserved
	11	DTS type1
	12	DTS type2
	13	DTS type3
	14	ATRAC
	15	ATRACK2/3
	16 to 26	Reserved
	27	Reserved (MPEG-4, AAC data)
	28	MPEG-2, AAC data
	29 to 31	Reserved
DO6, 5	0	Reserved (set to "0")
DO7	0	Error flag indicating effective burst payload
	1	Error flag indicating burst payload error
DO12 to 8		Data type dependent information
DO15 to 13	0	Bit stream number. (set to "0")

13 Application Example

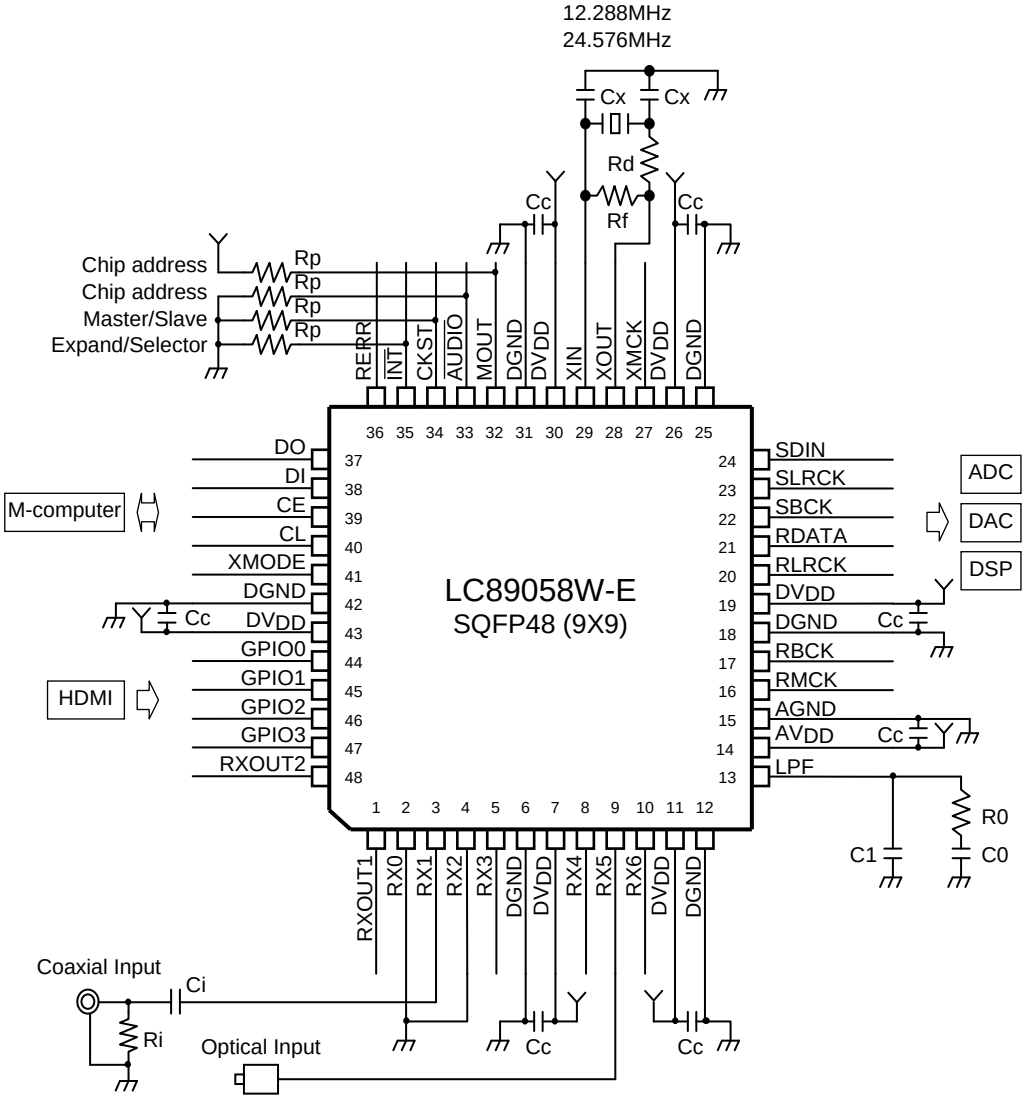


Table 13.1 Application Example

Element Symbol	Recommended Parameter	Application	Remarks
Cc	0.1μF	Power supply de-coupling	Ceramic capacitor
Rp	10kΩ	Function setting	Pull-down/pull-up resistor
Cx	1pF to 33pF	Quarts resonator load	Ceramic capacitor with NP0 characteristics
Rf	1MΩ	Oscillation amplifier feedback	
Rd	150Ω to 330Ω	Oscillation amplifier current limit	
Ci	0.1μF to 0.01μF	Coaxial input DC cut	Ceramic capacitor
Ri	75Ω	Coaxial input termination	
C0	**	PLL loop filter	(**: See Section 10.1.1)
C1	**	PLL loop filter	(**: See Section 10.1.1)
R0	**	PLL loop filter	(**: See Section 10.1.1)