BLOCK DIAGRAMS

Application 1

Stepper 3ch-ex.1 & using Crystal oscillator (or Ceramic oscillator)

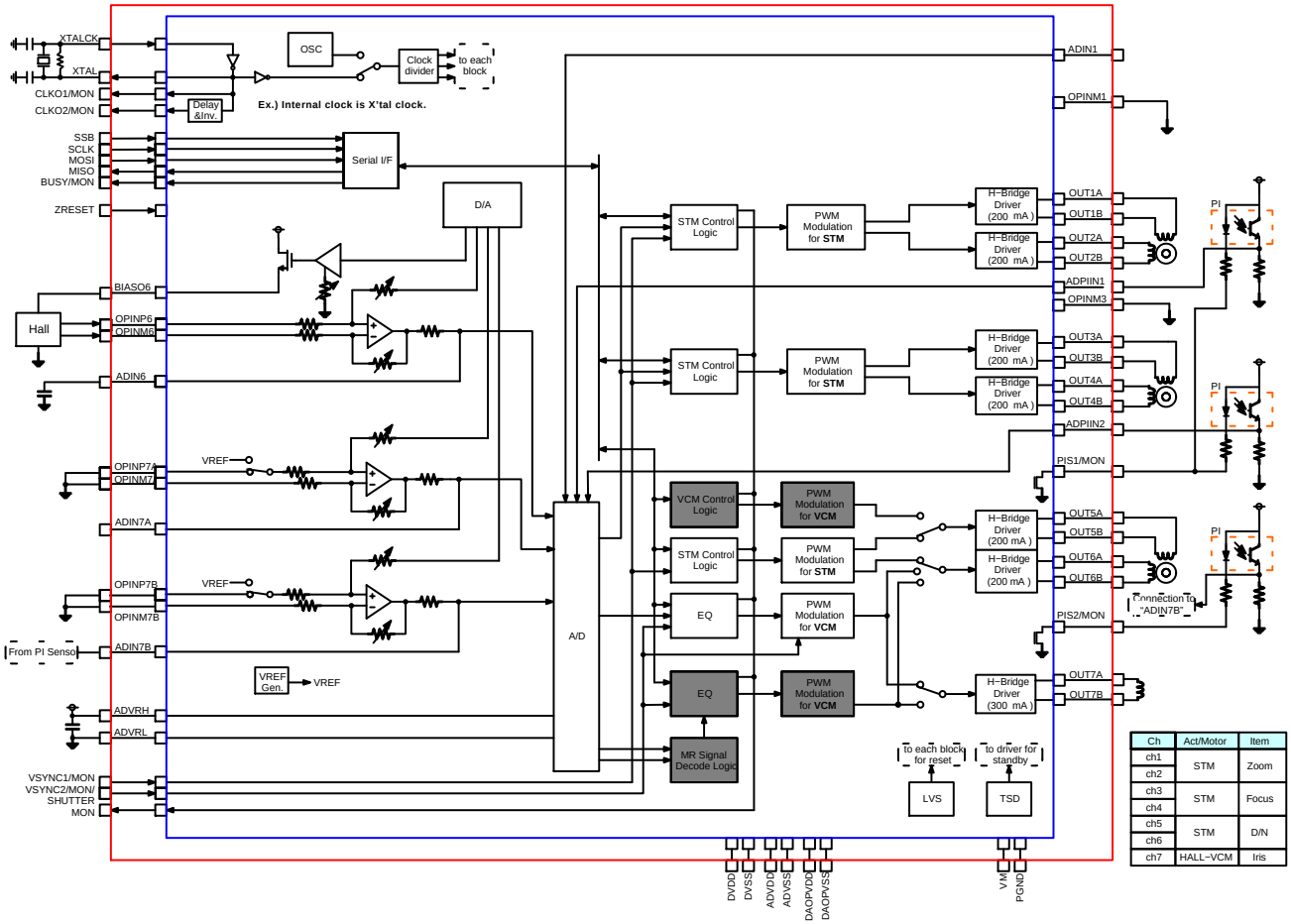


Figure 1. Application 1

Application 2

Stepper 3ch-ex.2 & using internal OSC

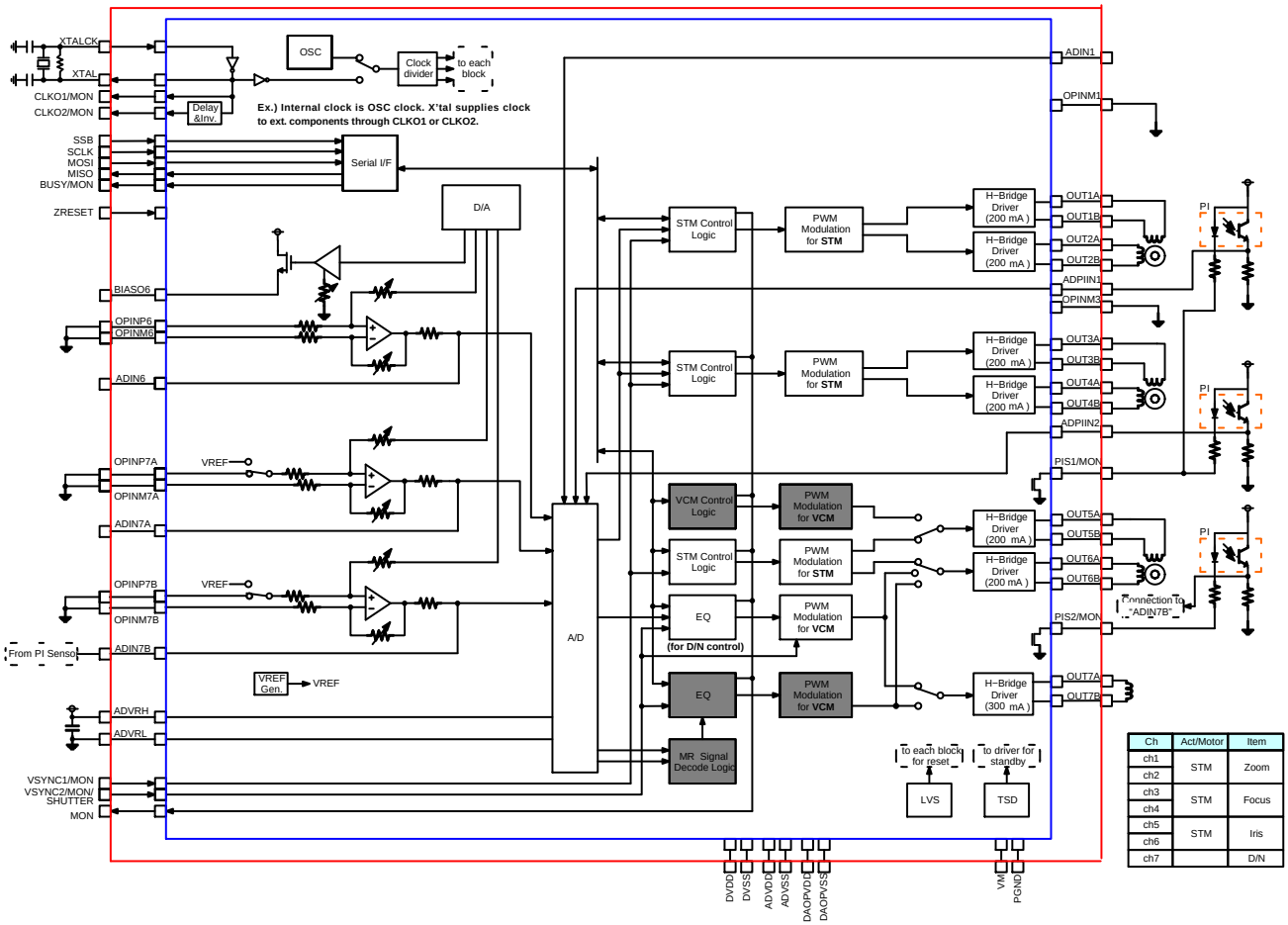


Figure 2. Application 2

Application−3

Stepper 2ch & using internal OSC

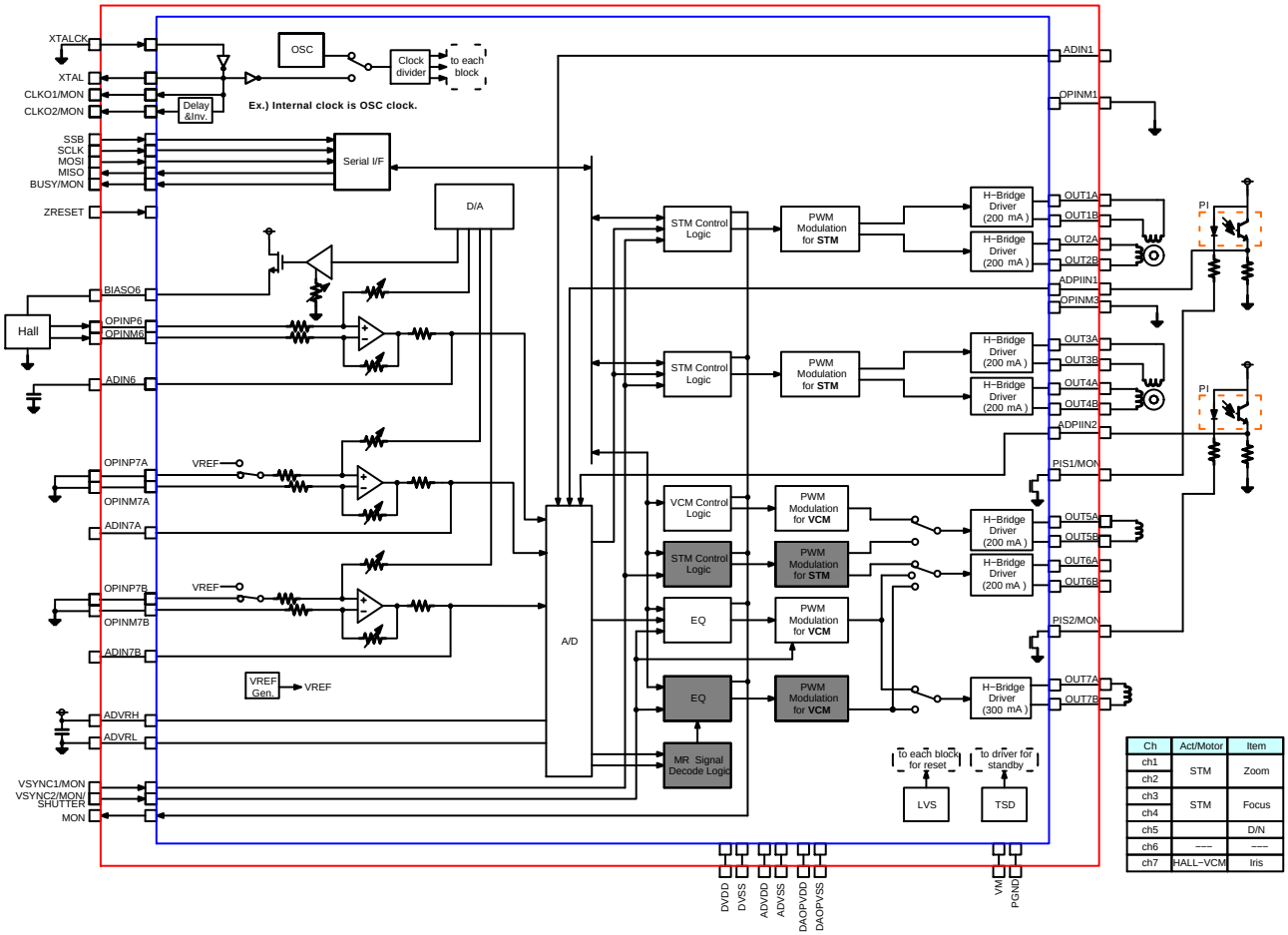


Figure 3. Application 3

Application−4

MR−VCM & using internal OSC

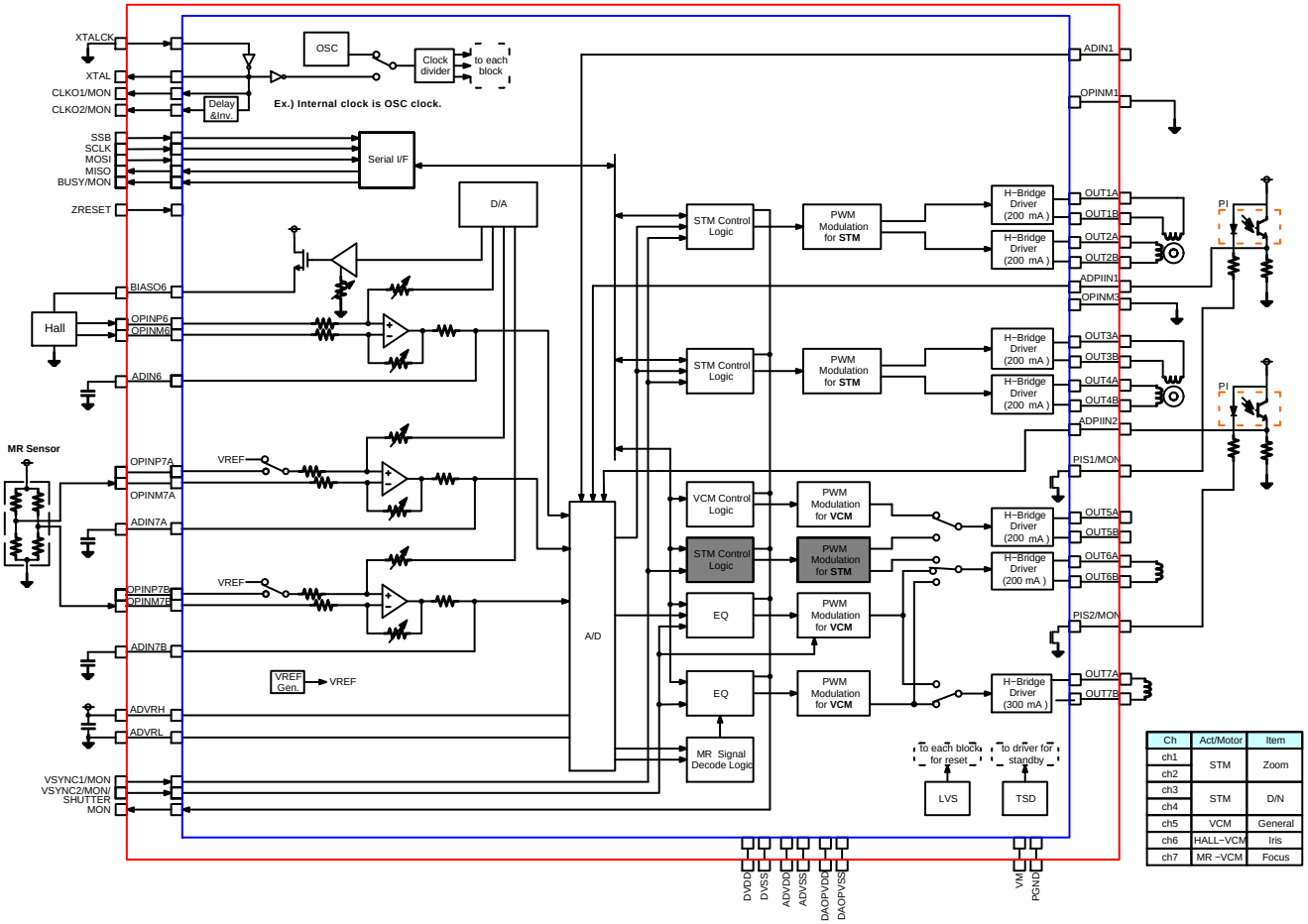


Figure 4. Application 4

PIN DESCRIPTION

Table 1. PIN DESCRIPTION

TYPE					
I	INPUT	P	Power, GND	NC	NOT CONNECT
O	OUTPUT				
B(I)	BIDIRECTION: INPUT at Reset				
B(O)	BIDIRECTION: OUTPUT at Reset				

SPI INTERFACE (SLAVE)		
SSB	I	Chip select
SCLK	I	Clock
MOSI	I	Received data
MISO	B(O)	Transmit data
BUSY/MON	B(O)	Transfer busy / Monitor output
PI SENSOR DRIVE SIGNAL OUTPUT		
PIS1/MON	B(O)	PI sensor drive signal output 1 / Monitor output
PIS2/MON	B(O)	PI sensor drive signal output 2 / Monitor output
VIDEO SYNCHRONIZING SIGNAL INPUT		
VSYNC1/MON	B(I)	Video synchronizing signal input / Monitor output (with pull-down resistance)
VSYNC2/MON /SHUTTER	B(I)	Video synchronizing signal input / Monitor output / Shutter input (with pull-down resistance)
MONITOR OUTPUT		
MON	B(O)	Monitor output
CLOCK OUTPUT		
XTALCK	I	Oscillation amplifier input
XTAL	O	Oscillation amplifier output
CLKO1/MON	B(O)	Clock output 1 / Monitor output
CLKO2/MON	B(O)	Clock output 2 / Monitor output
RESET		
ZRESET	I	Reset signal input (Low active)
BIAS CURRENT PIN		
BIASO6	O	CH6 Bias current output
OP AMP PIN		
OPINP6	I	CH6 OP Amp input (+)
OPINM6	I	CH6 OP Amp input (−)
OPINP7A	I	CH7−A OP Amp input (+)
OPINM7A	I	CH7−A OP Amp input (−)
OPINP7B	I	CH7−B OP Amp input (+)
OPINM7B	I	CH7−B OP Amp input (−)
A/D INPUT PIN		
ADIN1	B	General A/D input
ADIN6	B	CH6 A/D input (CH6 OP Amp output)
ADIN7A	B	CH7−A A/D input (CH7 OP Amp output)

A/D INPUT PIN		
ADIN7B	B	CH7−B A/D input (CH7 OP Amp output)
ADPIIN1	I	CH1/2 PI sensor signal A/D input
ADPIIN2	I	CH3/4 PI sensor signal A/D input
ADVRH	I	A/D conversion range standard voltage
ADVRL	I	A/D conversion range standard voltage
H−BRIDGE		
OUT1A	O	CH1 H−Bridge output
OUT1B	O	CH1 H−Bridge output
OUT2A	O	CH2 H−Bridge output
OUT2B	O	CH2 H−Bridge output
OUT3A	O	CH3 H−Bridge output
OUT3B	O	CH3 H−Bridge output
OUT4A	O	CH4 H−Bridge output
OUT4B	O	CH4 H−Bridge output
OUT5A	O	CH5 H−Bridge output
OUT5B	O	CH5 H−Bridge output
OUT6A	O	CH6 H−Bridge output
OUT6B	O	CH6 H−Bridge output
OUT7A	O	CH7 H−Bridge output
OUT7B	O	CH7 H−Bridge output
MISCELLANEOUS		
OPINM1	I	Connect to GND (DAOPVSS)
OPINM3	I	Connect to GND (DAOPVSS)
POWER PIN		
DVDD	P	Digital VDD
DVSS	P	Digital GND
DAOPVDD	P	D/A, OP Amp VDD
DAOPVSS	P	D/A, OP Amp GND
ADVDD	P	A/D VDD
ADVSS	P	A/D GND
VM	P	H−Bridge VDD
PGND	P	H−Bridge GND

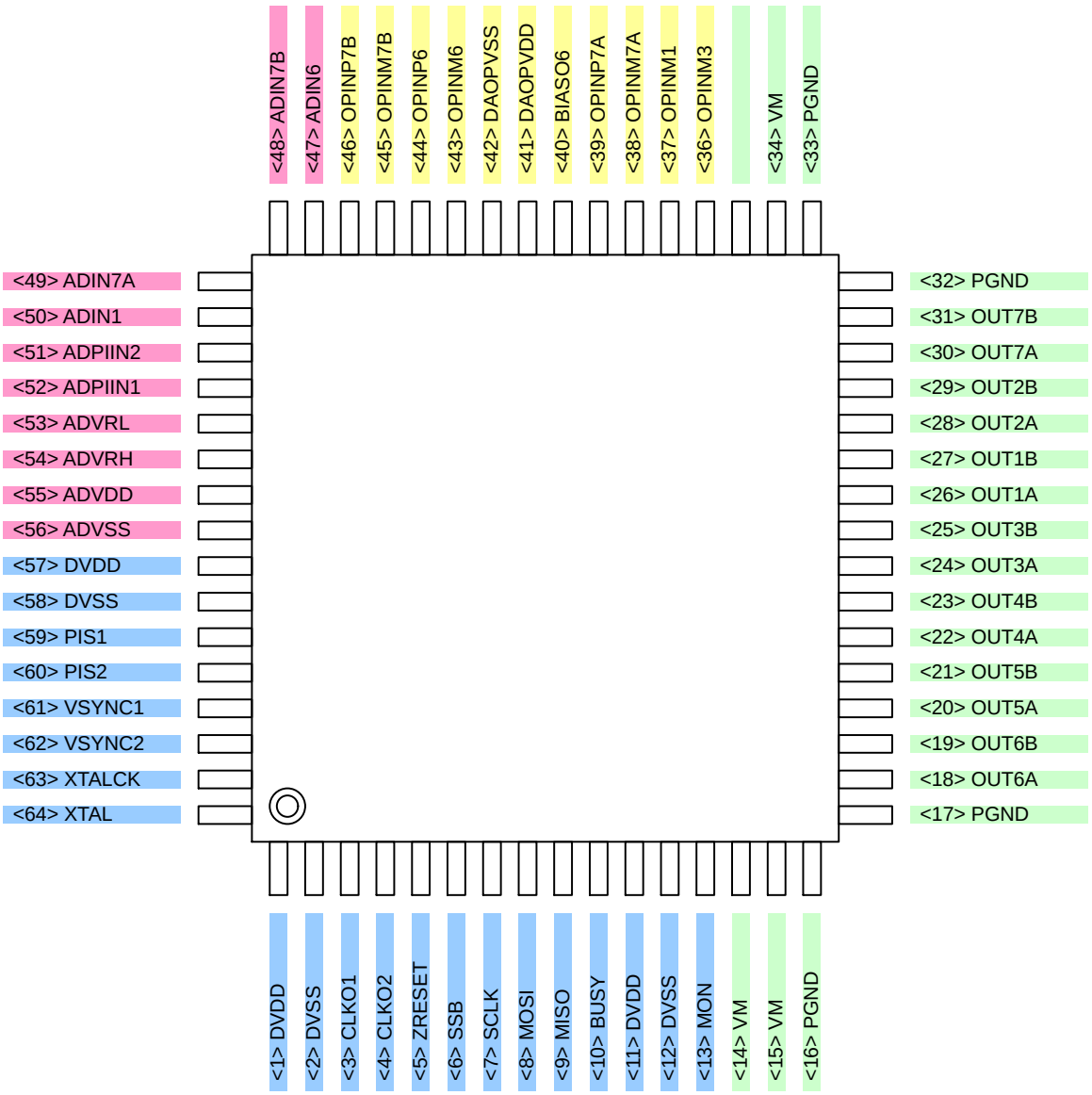
Process when pins are not used

- PIN TYPE “O” − The pin must be left open
- PIN TYPE “I” − The pin must not be left open. Please make sure to connect the pin to V_{DD} or V_{SS} even when it is not used. (Please check with us whether to connect to V_{DD} or V_{SS})
- PIN TYPE “B” − Please contact us if you are uncertain about a processing method in the pin description in the PIN layout table

A problem may occur if the processing method is used wrongly for any unused pin.

Please make sure to contact us.

PIN ASSIGNMENT − TQFP64



(TOP VIEW)

Figure 5. TQFP64 (7×7)

PIN ASSIGNMENT − FBGA64

	A	B	C	D	E	F	G	H	J	K
10	DVDD	VSYNC2	PIS2	DVSS	ADVSS	ADVDD	ADPI IN1	ADPI IN2	ADIN7A	ADIN7B
9	DVSS				ADVRL	ADVRH				ADIN6
8	CLKO1		XTALCK	VSYNC1	PIS1	DVDD	ADIN1	OPINM 7B		OPINP 7B
7	CLKO2		XTAL					OPINM6		OPINP6
6	SSB		ZRESET	SCLK			BIASO6	DAOP VSS		DAOP VDD
5	MISO		BUSY	MOSI			OPINM1	OPINP 7A		OPINM 7A
4	DVDD		DVSS					OPINM3		OUT7A
3	MON		OUT6A	OUT5A	OUT4A	OUT3A	OUT1A	OUT2A		OUT7B
2	VM	VM							VM	VM
1	PGND	PGND	OUT6B	OUT5B	OUT4B	OUT3B	OUT1B	OUT2B	PGND	PGND

(TOP VIEW)

Figure 6. FBGA64 (6.0×6.0)

PIN NUMBER

Table 2. PIN NUMBER

Pin No.		Type	Pin name
TQFP64	FBGA64		
1	A10	P	DVDD
2	A9	P	DVSS
3	A8	B(O)	CLKO1
4	A7	B(O)	CLKO2
5	C6	I	ZRESET
6	A6	I	SSB
7	D6	I	SCLK
8	D5	I	MOSI
9	A5	B(O)	MISO
10	C5	B(O)	BUSY
11	A4	P	DVDD
12	C4	P	DVSS
13	A3	B(O)	MON
14	B2	P	VM
15	A2	P	VM
16	B1	P	PGND
17	A1	P	PGND
18	C3	O	OUT6A
19	C1	O	OUT6B
20	D3	O	OUT5A
21	D1	O	OUT5B
22	E3	O	OUT4A
23	E1	O	OUT4B
24	F3	O	OUT3A
25	F1	O	OUT3B
26	G3	O	OUT1A
27	G1	O	OUT1B
28	H3	O	OUT2A
29	H1	O	OUT2B
30	K4	O	OUT7A
31	K3	O	OUT7B
32	K1	P	PGND
33	J1	P	PGND
34	J2	P	VM
35	K2	P	VM
36	H4	I	OPINM3
37	G5	I	OPINM1
38	K5	I	OPINM7A
39	H5	I	OPINP7A

Table 2. PIN NUMBER (continued)

Pin No.		Type	Pin name
TQFP64	FBGA64		
40	G6	O	BIASO6
41	K6	P	DAOPVDD
42	H6	P	DAOPVSS
43	H7	I	OPINM6
44	K7	I	OPINP6
45	H8	I	OPINM7B
46	K8	I	OPINP7B
47	K9	B	ADIN6
48	K10	B	ADIN7B
49	J10	B	ADIN7A
50	G8	B	ADIN1
51	H10	I	ADPIIN2
52	G10	I	ADPIIN1
53	E9	I	ADVRL
54	F9	I	ADVRH
55	F10	P	ADVDD
56	E10	P	ADVSS
57	F8	P	DVDD
58	D10	P	DVSS
59	E8	B(O)	PIS1
60	C10	B(O)	PIS2
61	D8	B(I)	VSYNC1
62	B10	B(I)	VSYNC2
63	C8	I	XTALCK
64	C7	O	XTAL

ELECTRICAL CHARACTERISTICS

Logic, Analog

Logic, Analog power: DVDD/DVSS, OPDAVDD/ OPDAVSS, ADVDD/ADVSS, these should be connected at the same voltage. They are shown DVDD/DVSS as follows.

ABSOLUTE MAXIMUM RATINGS (DVSS = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	DVDD max	$T_A \le 25°C$	–0.3 to 4.6	V
Input/Output Voltage	V_{IN}, V_{OUT}	$T_A \le 25°C$	–0.3 to DVDD+0.3	V
Storage Temperature	T_{stg}		–55 to 125	°C
Operating Temperature	T_{opr}		–20 to 85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ALLOWABLE OPERATING RANGES (T_A = −20 to 85°C, DVSS = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Applicable Pins
Power Supply Voltage	DVDD	2.7	3.3	3.6	V	
Input Voltage Range	V_{IN}	0	−	DVDD	V	Except for OPINM1, OPINM3
		0	−	VM	V	OPINM1, OPINM3

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS: INPUT/OUTPUT LEVEL (T_A = −20 to 85°C, DVSS = 0 V, DVDD = 2.7 to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable Pins
High-level Input Voltage	V_{IH}	CMOS	0.7 DVDD			V	(2)(3)
Low-level Input Voltage	V_{IL}				0.2 DVDD	V	
High-level Input Voltage	V_{IH}	CMOS Schmidt	0.75 DVDD			V	(1)
Low-level Input Voltage	V_{IL}				0.15 DVDD	V	
High-level Output Voltage	V_{OH}	I_{OH} = –4 mA	DVDD − 0.4			V	(2)(3)(4)
Low-level Output Voltage	V_{OL}	I_{OL} = 4 mA			0.4	V	(2)(3)
		I_{OL} = 30 mA			0.4	V	(4)
PullDown Resistance	Rdn		40	80	200	kΩ	(3)
Analog Input Voltage	V_{AI}		DVSS		DVDD	V	(5)
			PGND		VM	V	(6)
VGA Output Resistance	R_{out}			1		kΩ	(7)
Analog Output Current	I_{AO}	CMSDAC = 001b & WH_DAV4 = 00h		1		mA	(8)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Applicable Pins:
(1) ZRESET, SSB, SCLK, MOSI
(2) MISO, BUSY, MON, CLKO1, CLKO2
(3) VSYNC1, VSYNC2
(4) PIS1, PIS2
(5) OPINP6, OPINM6, OPINP7A, OPINM7A, OPINP7B, OPINM7B, ADPIIN1, ADPIIN2
(6) OPINM1, OPINM3
(7) ADIN1, ADIN6, ADIN7A, ADIN7B
(8) BIASO6

VM

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, PGND = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	VM_{max}		–0.3 to 7.0	V
Output Peak Current	I_{opeak1}	OUT1A/B to OUT6A/B t ≤ 10 ms, On-duty ≤ 20%	300	mA
	I_{opeak2}	OUT7A/B t ≤ 10 ms, On-duty ≤ 20%	450	mA
Output Continuous Current	I_{omax1}	OUT1A/B to OUT6A/B	200	mA
	I_{omax2}	OUT7A/B	300	mA
Storage Temperature	T_{stg}		–55 to 125	°C
Operating Temperature	T_{opr}		–20 to 85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ALLOWABLE OPERATING RANGES (T_A = 25°C, PGND = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	VM		2.7 to 5.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, PGND = 0 V, VM = 5 V)

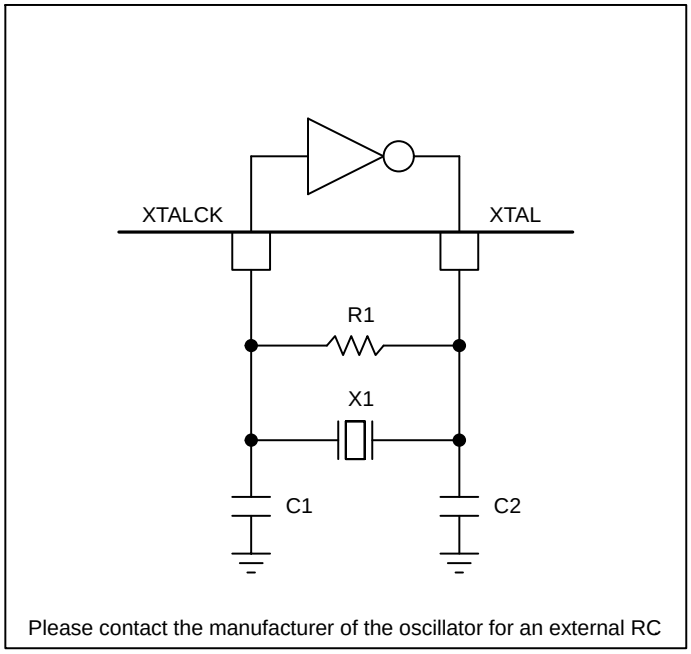
Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable Pins
Output ON Resistance	R_{onu}	I_O = 200 mA Pch		0.85		Ω	(9)
	R_{ond}	I_O = 200 mA Nch		0.45		Ω	
Output ON Resistance	R_{onu}	I_O = 300 mA Pch		0.85		Ω	(10)
	R_{ond}	I_O = 300 mA Nch		0.45		Ω	
Diode Forward Voltage	V_D	I_D = –200 mA		0.9		V	(9)
		I_D = –300 mA		0.9		V	(10)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Applicable Pins:
(9) OUT1A, OUT1B, OUT2A, OUT2B, OUT3A, OUT3B, OUT4A, OUT4B, OUT5A, OUT5B, OUT6A, OUT6B
(10) OUT7A, OUT7B

EXAMPLE OF EXTERNAL CIRCUIT

Connection example of oscillation circuit.



* In the case of X'tal, it takes about 50 ms for oscillation to stabilize (please check with the manufacturer for a precise time period).

Figure 7. Example of External Circuit

AC CHARACTERISTICS

1−a) Power Supply, Reset Pin

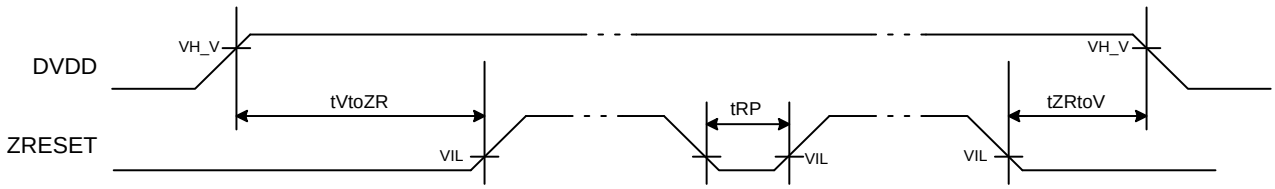


Figure 8.

1−b) Specification

DVDD: DVDD, OPDAVDD, ADVDD
VH_V: 2.7 V
VIL: 0.15 × DVDD

Parameter	Symbol	Min	Typ	Max	Unit
The time from the rise of DVDD to the rise of ZRESET	tVtoZR	1			ms
The time from the fall of DVDD to the fall of ZRESET	tZRtoV	500			μs
Low period of ZRESET	tRP	100			μs

VM can be turn on/off regardless above power supply AC timing.

2−a) Power Supply, Reset Pin

Upper: “H” active Use setting of 0250h−0253h−bit2 = 0
Lower: “L” active Use setting of the above bit = 1

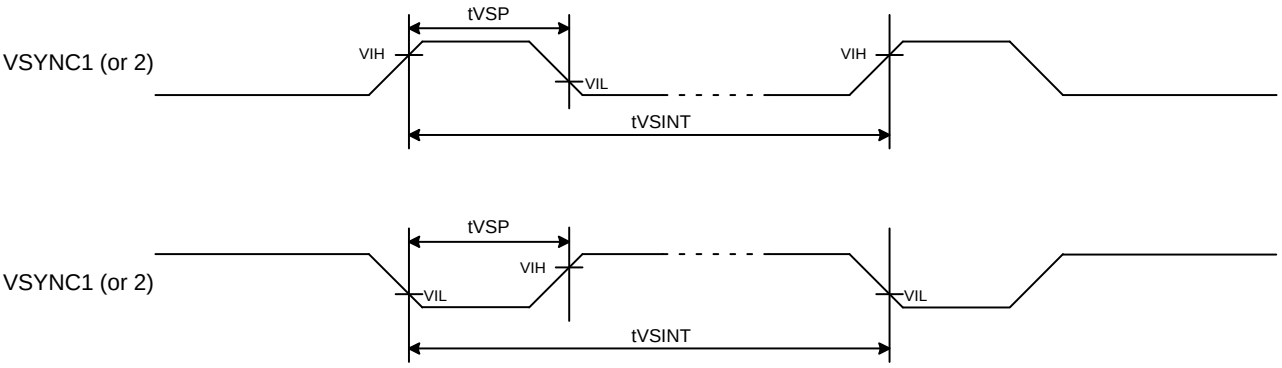


Figure 9.

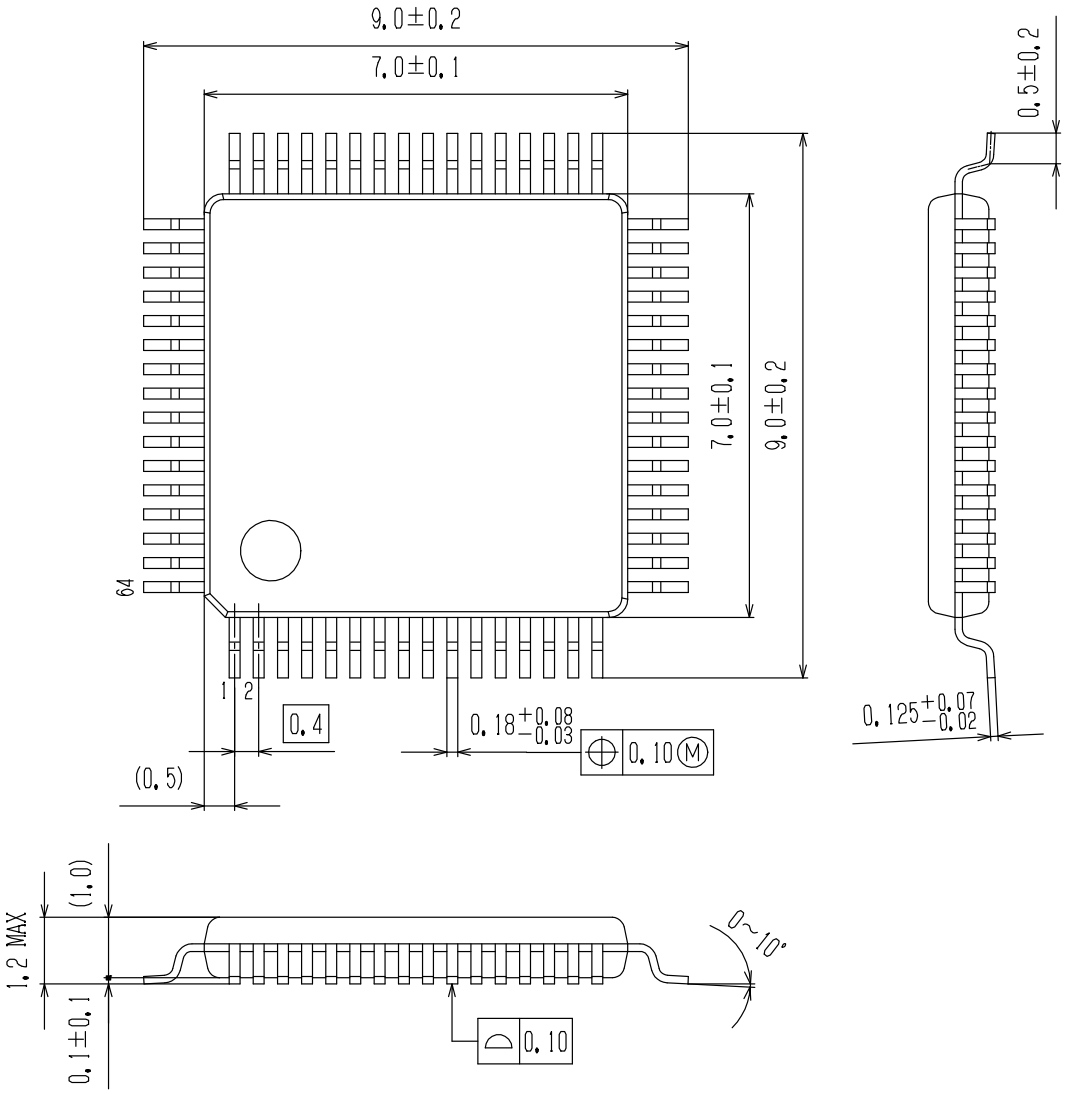
2−b) Specification

VIH: 0.7 × DVDD
VIL: 0.2 × DVDD

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Active period of VSYNC1(or 2)	tVSP	STMCLK = 12 MHz	100			ns
Interval time of VSYNC1(or 2)	tVSINT		2			ms

PACKAGE DIMENSIONS

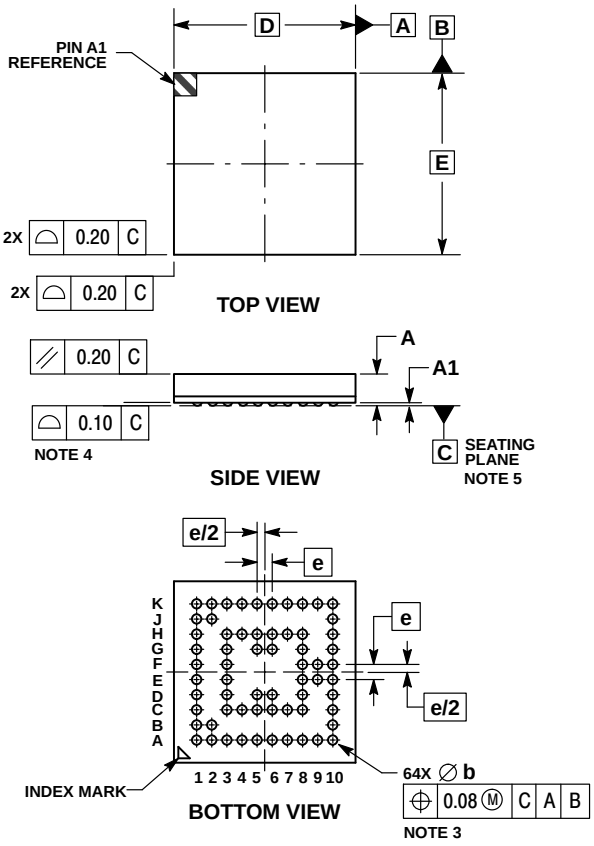
TQFP64 7x7 / TQFP64
CASE 932BC
ISSUE O



LC898201

PACKAGE DIMENSIONS

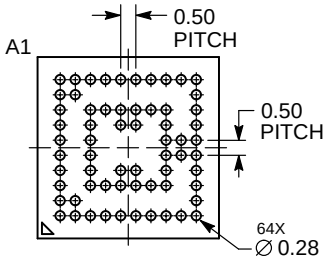
FBGA64 6x6
CASE 113BL
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.
5. DIMENSION C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	1.05
A1	0.05	0.15
b	0.24	0.34
D	6.00 BSC	
E	6.00 BSC	
e	0.50 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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