

FIG.1- 8/20us pulse waveform according to IEC 61000-4-5

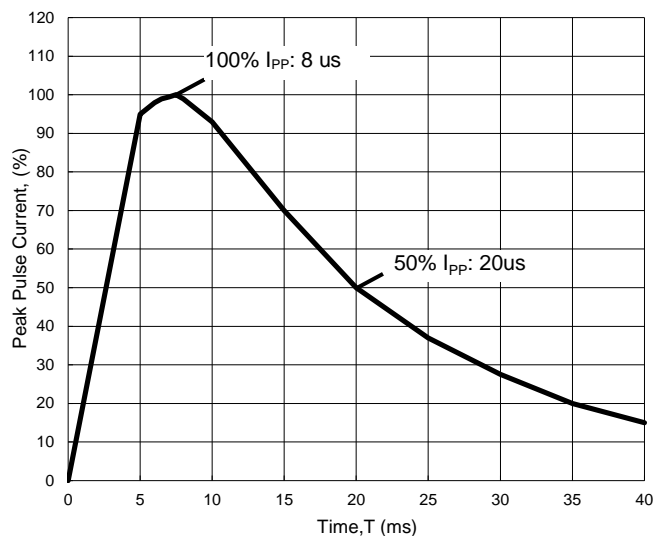


FIG .2- ESD pulse waveform according to IEC 61000-4-2

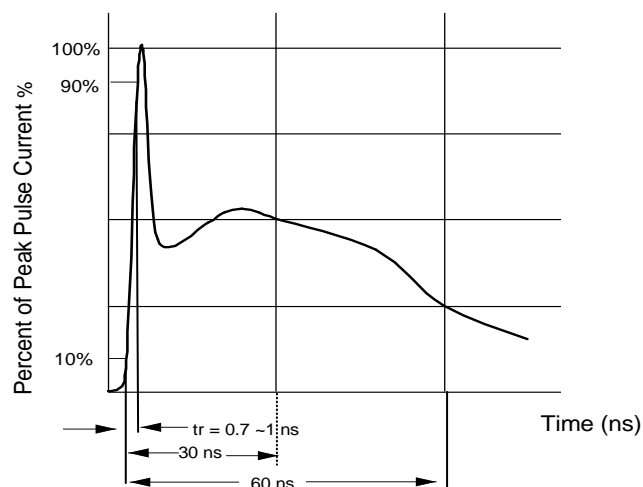


FIG.3- Power Dissipation Versus Pulse Time

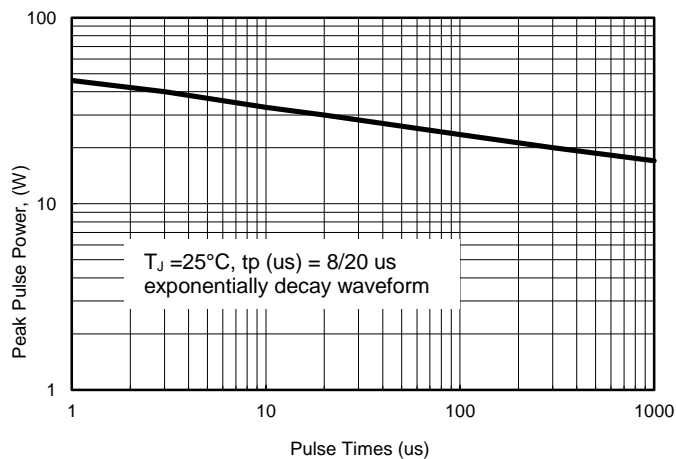


FIG.4- Peak Pulse Power Versus T_J

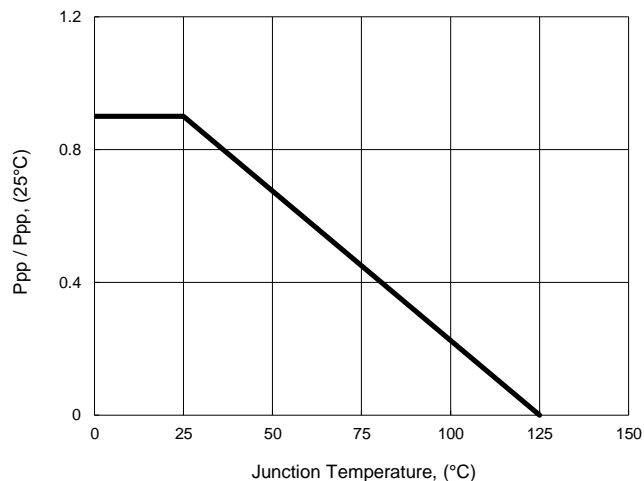


FIG.5- Typical Junction Capacitance

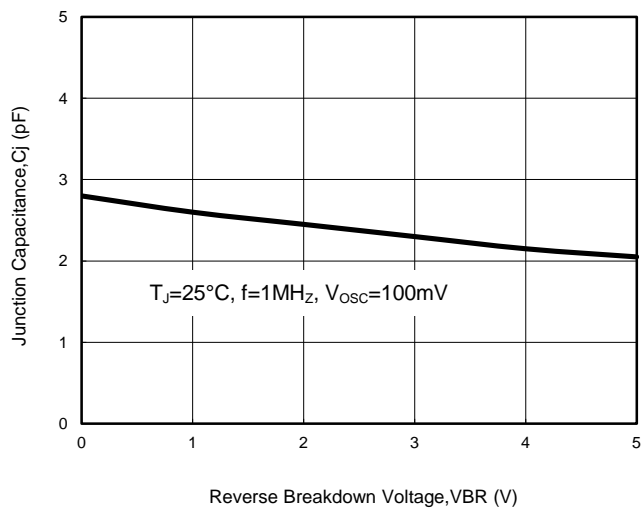
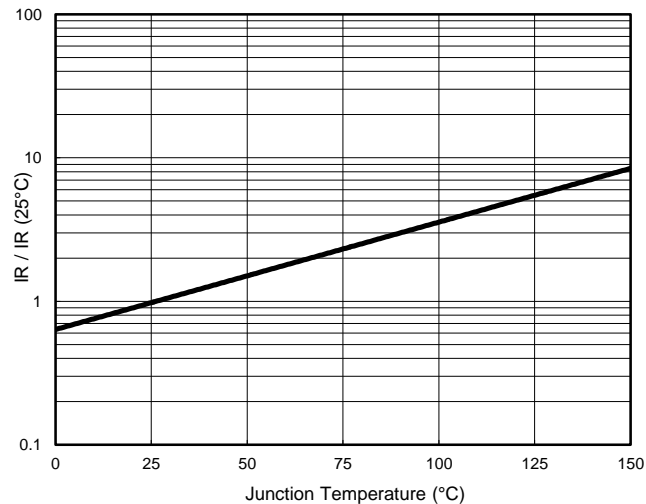


FIG.6- Reverse Leakage Current Versus T_J



RATING AND CHARACTERISTIC CURVES

L03ESDL5V0CE2

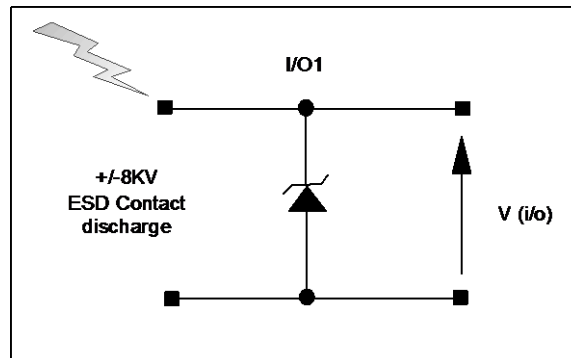


FIG.7- ESD Test Configuration

FIG.8- Clamped +8 kV ESD voltage waveform

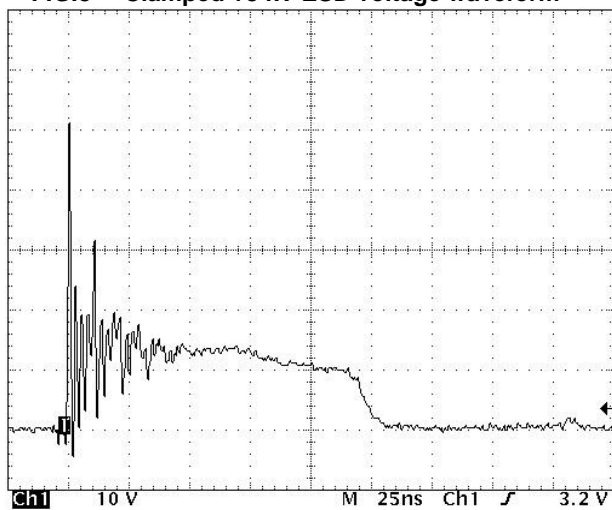
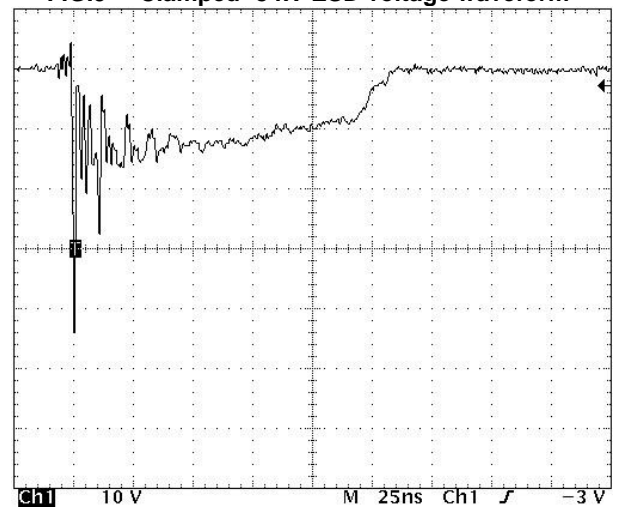
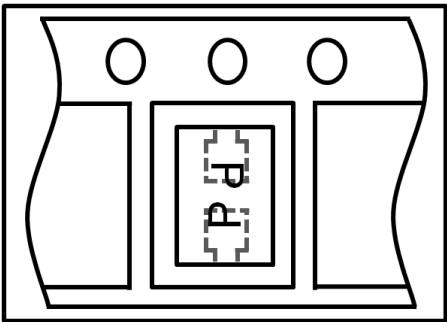


FIG.9- Clamped -8 kV ESD voltage waveform



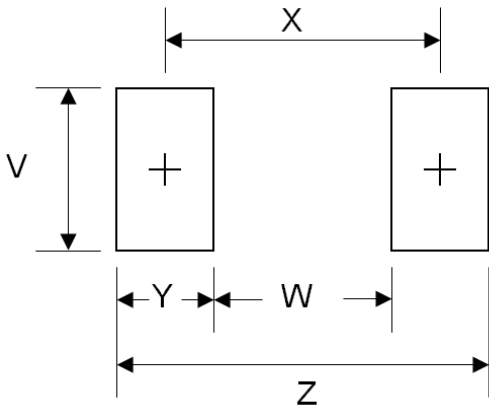
Marking & Orientation



Packaging Information

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L03ESDL5V0CE2	10K	7	150K	300K

SOD-882 Soldering Pad Layout



DIM.	MILLIMETERS	INCHES
Z	1.30	0.051
X	0.75	0.029
W	0.20	0.007
Y	0.55	0.021
V	0.80	0.031

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