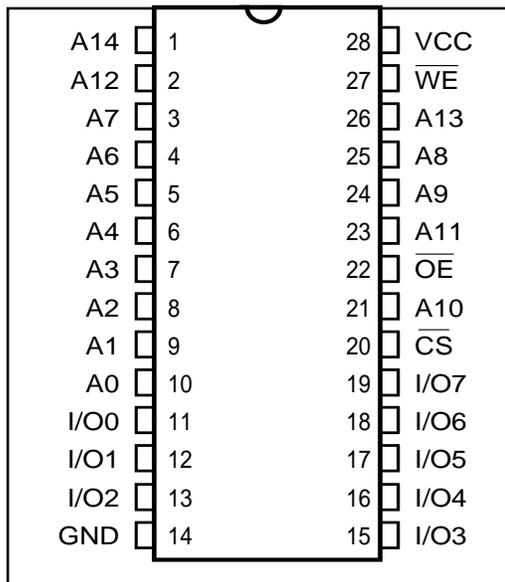


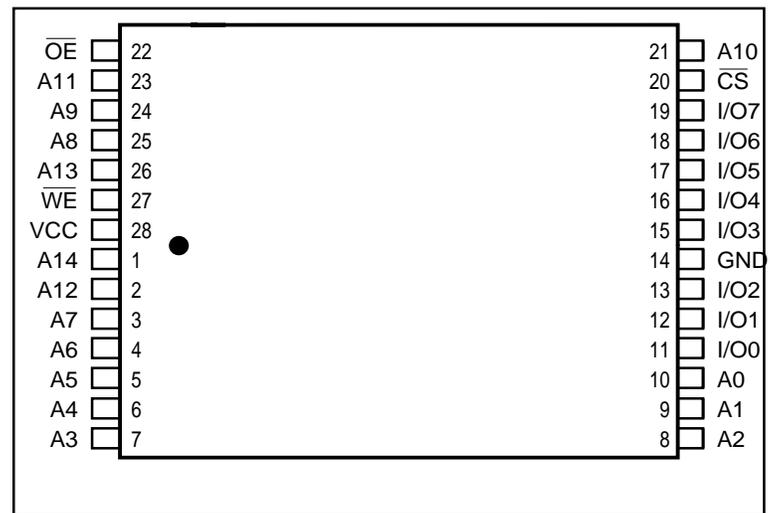
PIN CONFIGURATION

28-Pin SOP



PIN CONFIGURATION

28-Pin TSOP



PIN DESCRIPTIONS

A0-A14	Address Inputs
CS	Chip Select Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	WE	CS	OE	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	ISB1, ISB2
Output Disabled	H	L	H	High-Z	Icc1, Icc2
Read	H	L	L	DOUT	Icc1, Icc2
Write	L	L	X	DIN	Icc1, Icc2

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-65 to +150	°C
PT	Power Dissipation	0.5	W
IOUT	DC Output Current (LOW)	20	mA

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1.0 mA	2.4	—	V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA	—	0.4	V	
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.5	V	
V _{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V	
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{CC}	Com. Ind.	-2 10	2 10	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{CC} , Outputs Disabled	Com. Ind.	-2 -10	2 10	μA

Note:

1. V_{IL} = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-45 ns		-70 ns		Unit
				Min.	Max.	Min.	Max.	
I _{CC1}	V _{CC} Operating Supply Current	V _{CC} = Max., \overline{CS} = V _{IL} I _{OUT} = 0 mA, f = 0	Com.	—	60	—	60	mA
			Ind.	—	70	—	70	
I _{CC2}	V _{CC} Dynamic Operating Supply Current	V _{CC} = Max., \overline{CS} = V _{IL} I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	70	—	65	mA
			Ind.	—	80	—	75	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} \overline{CS} ≥ V _{IH} , f = 0	Com.	—	5	—	5	mA
			Ind.	—	10	—	10	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max., \overline{CS} ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com.	—	0.5	—	0.5	mA
			Ind.	—	1.0	—	1.0	

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	10	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V _{DR}	V _{CC} for retention of data		2.0	—	V
I _{DR1}	Data retention current	V _{DR} = 3.0V, T _A = 0°C to +25°C	—	200	μA
I _{DR2}	Data retention current	V _{DR} = 3.0V, T _A = 0°C to +70°C	—	200	μA

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-45 ns		-70 ns		Unit
		Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	45	—	70	—	ns
t _{AA}	Address Access Time	—	45	—	70	ns
t _{OH}	Output Hold Time	2	—	2	—	ns
t _{ACS}	$\overline{\text{CS}}$ Access Time	—	45	—	70	ns
t _{DOE}	$\overline{\text{OE}}$ Access Time	—	25	—	35	ns
t _{LZOE} ⁽²⁾	$\overline{\text{OE}}$ to Low-Z Output	0	—	0	—	ns
t _{HZOE} ⁽²⁾	$\overline{\text{OE}}$ to High-Z Output	0	20	0	25	ns
t _{LZCS} ⁽²⁾	$\overline{\text{CS}}$ to Low-Z Output	3	—	3	—	ns
t _{HZCS} ⁽²⁾	$\overline{\text{CS}}$ to High-Z Output	0	20	0	25	ns
t _{PU} ⁽³⁾	$\overline{\text{CS}}$ to Power-Up	0	—	0	—	ns
t _{PD} ⁽³⁾	$\overline{\text{CS}}$ to Power-Down	—	30	—	50	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

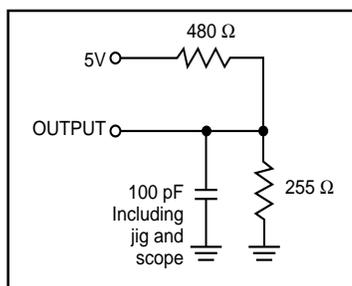


Figure 1.

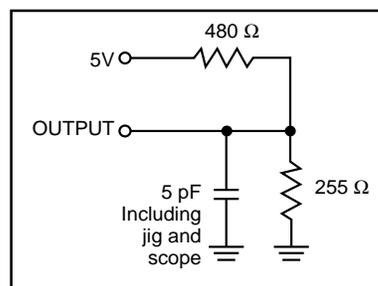
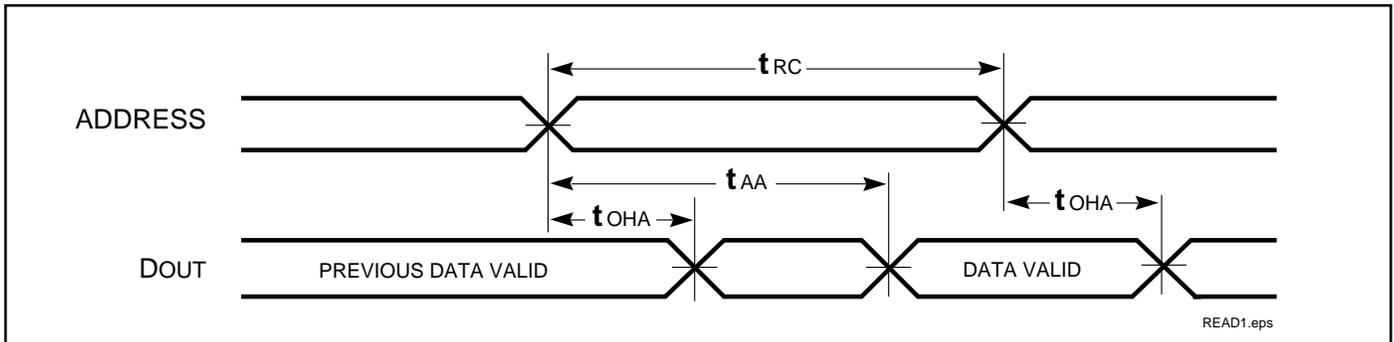
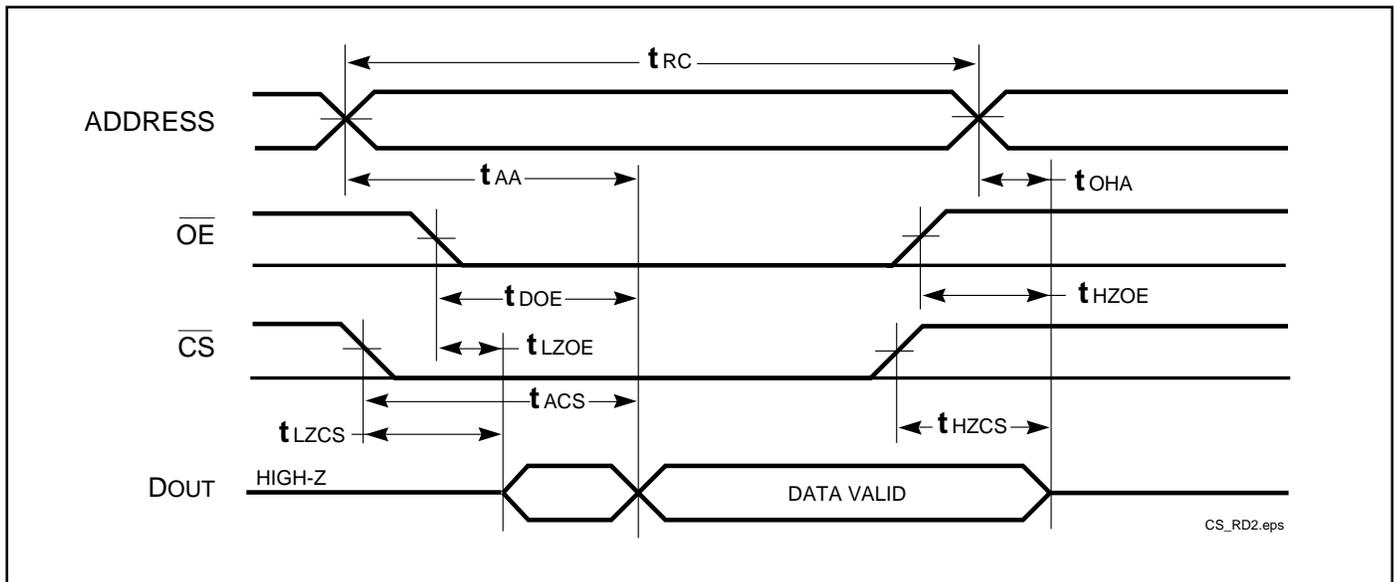


Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2)READ CYCLE NO. 2^(1,3)**Notes:**

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CS} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CS} LOW transitions.

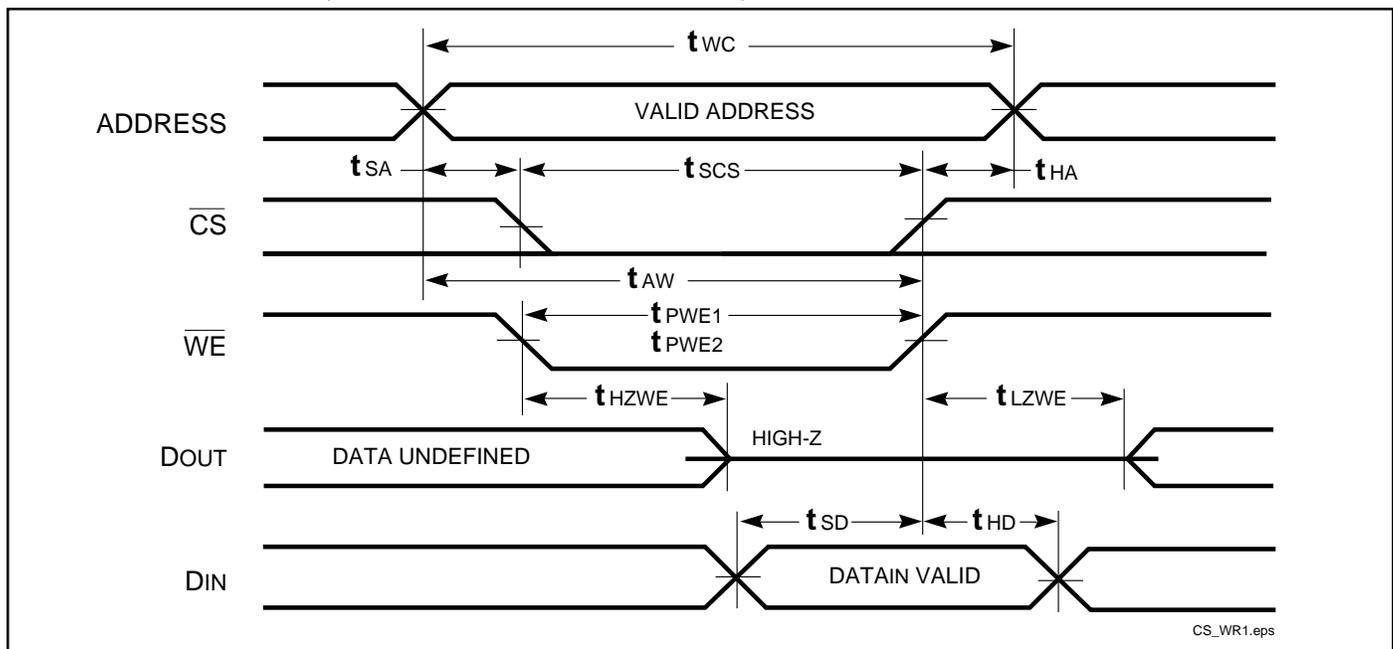
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

Symbol	Parameter	-45 ns		-70ns		Unit
		Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	45	—	70	—	ns
t _{SCS}	\overline{CS} to Write End	35	—	60	—	ns
t _{AW}	Address Setup Time to Write End	25	—	60	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	ns
t _{PWE⁽⁴⁾}	\overline{WE} Pulse Width	25	—	55	—	ns
t _{SD}	Data Setup to Write End	20	—	30	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CS} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. Tested with \overline{OE} HIGH.

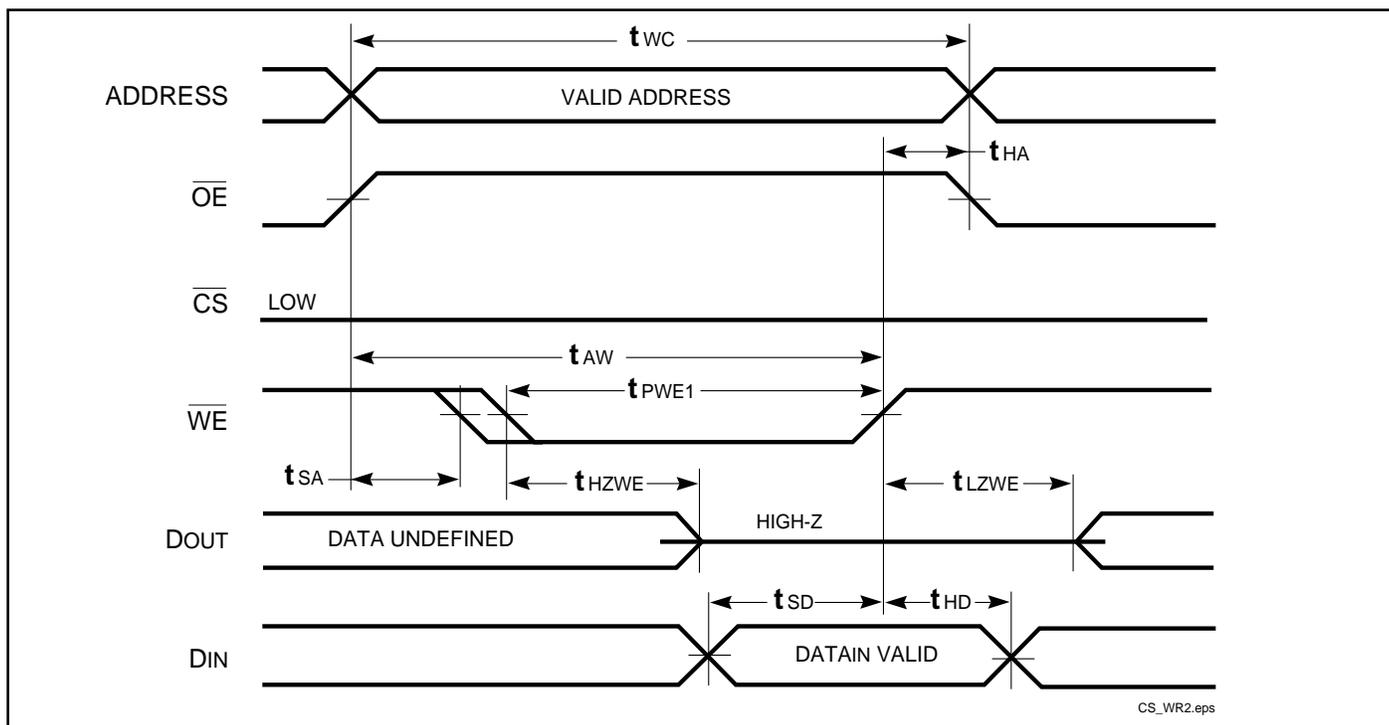
AC WAVEFORMS

WRITE CYCLE NO. 1 (\overline{CS} Controlled, \overline{OE} is HIGH or LOW) ⁽¹⁾

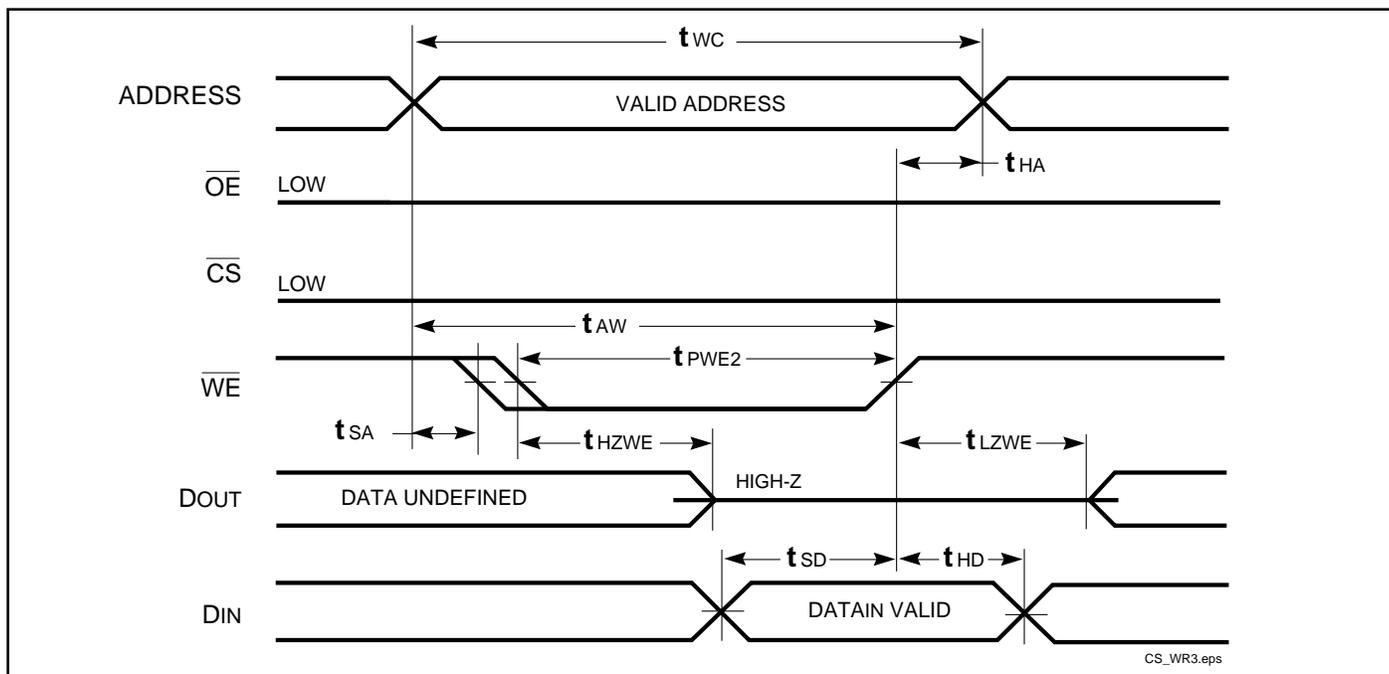
IS62C256

AC WAVEFORMS

WRITE CYCLE NO. 2 (\overline{OE} is HIGH During Write Cycle) ^(1,2)



WRITE CYCLE NO. 3 (\overline{OE} is LOW During Write Cycle) ⁽¹⁾



Notes:

1. The internal write time is defined by the overlap of \overline{CS} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
2. I/O will assume the High-Z state if $\overline{OE} = V_{IH}$.

ORDERING INFORMATION**Commerical Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
45	IS62C256-45T	TSOP
	IS62C256-45U	Plastic SOP
70	IS62C256-70T	TSOP
	IS62C256-70U	Plastic SOP

ORDERING INFORMATION**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
45	IS62C256-45TI	TSOP
	IS62C256-45UI	Plastic SOP
70	IS62C256-70TI	TSOP
	IS62C256-70UI	Plastic SOP

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