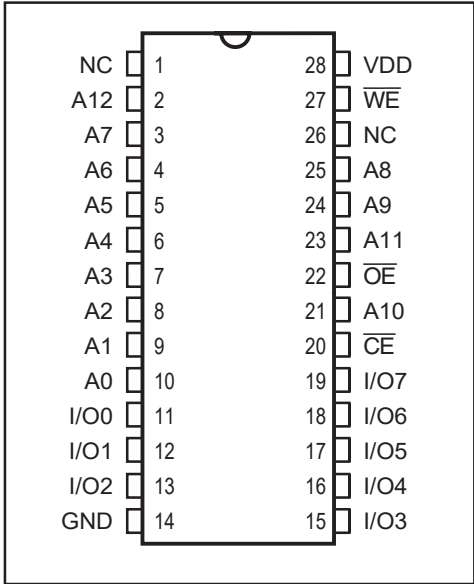


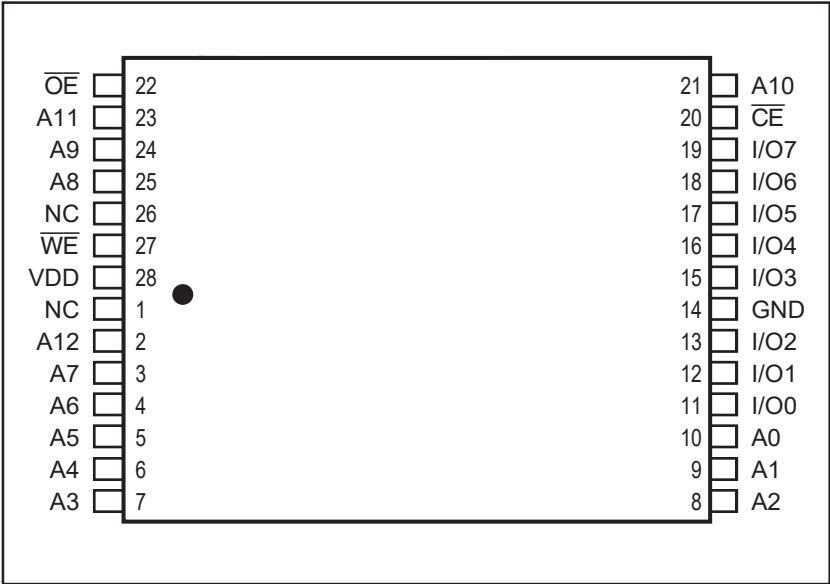
TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V <sub>DD</sub> Current
Not Selected (Power-down)	X	H	X	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	High-Z	I <sub>CC</sub>
Read	H	L	L	DOUT	I <sub>CC</sub>
Write	L	L	X	DIN	I <sub>CC</sub>

PIN CONFIGURATION  
28-Pin SOJ



PIN CONFIGURATION  
28-Pin TSOP (Type 1)



PIN DESCRIPTIONS

A0-A12	Address Inputs
$\overline{CE}$	Chip Enable 1 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connect
V <sub>DD</sub>	Power
GND	Ground

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T <sub>STG</sub>	Storage Temperature	−65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.5	W
I <sub>OUT</sub>	DC Output Current (LOW)	20	mA

**Notes:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING RANGE**

Range	Ambient Temperature	Speed	V <sub>DD</sub> <sup>(1)</sup>
Commercial	0°C to +70°C	-10	5V ± 5%
Industrial	−40°C to +85°C	-10	5V ± 5%

**Note:**

1. If operated at 12ns, V<sub>DD</sub> range is 5V ± 10%.

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = −4.0 mA	2.4	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 8.0 mA	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>DD</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>		−0.3	0.8	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	Com. Ind.	−1 2	1 2 μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled	Com. Ind.	−1 −2	1 2 μA

**Note:**

1. V<sub>IL</sub> = −3.0V for pulse width less than 10 ns.

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	Test Conditions		-10		-12		Unit
				Min.	Max.	Min.	Max.	
I <sub>CC1</sub>	V <sub>DD</sub> Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CE}$ = V <sub>IL</sub>	Com.	—	20	—	20	mA
		I <sub>OUT</sub> = 0 mA, f = 0	Ind.	—	25	—	25	
I <sub>CC2</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CE}$ = V <sub>IL</sub>	Com.	—	45	—	35	mA
		I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Ind.	—	50	—	45	
			typ. <sup>(2)</sup>		25		25	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max.,	Com.	—	1	—	1	mA
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CE} \geq V_{IH}$ , f = 0	Ind.	—	2	—	2	
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max.,	Com.	—	350	—	350	μA
		$\overline{CE} \geq V_{DD} - 0.2V$ ,	Ind.	—	450	—	450	
		V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	typ. <sup>(2)</sup>		200		200	

**Note:**

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V<sub>DD</sub> = 5V, T<sub>A</sub> = 25°C. Not 100% tested.

**CAPACITANCE<sup>(1,2)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 5.0V.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

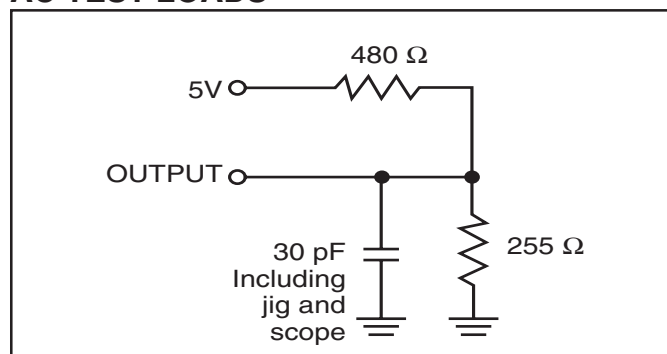
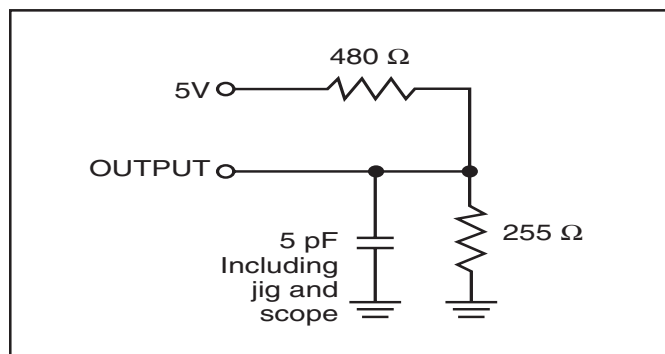
Symbol	Parameter	-10 ns		-12 ns		Unit
		Min.	Max	Min.	Max.	
$t_{RC}$	Read Cycle Time	10	—	12	—	ns
$t_{AA}$	Address Access Time	—	10	—	12	ns
$t_{OHA}$	Output Hold Time	2	—	2	—	ns
$t_{ACS}$	$\overline{CE}$ Access Time	—	10	—	12	ns
$t_{DOE}$	$\overline{OE}$ Access Time	—	6	—	6	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	—	5	—	6	ns
$t_{LZCS}^{(2)}$	$\overline{CE}$ to Low-Z Output	2	—	3	—	ns
$t_{HZCS}^{(2)}$	$\overline{CE}$ to High-Z Output	—	5	—	7	ns
$t_{PU}^{(3)}$	$\overline{CE}$ to Power-Up	0	—	0	—	ns
$t_{PD}^{(3)}$	$\overline{CE}$ to Power-Down	—	10	—	12	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

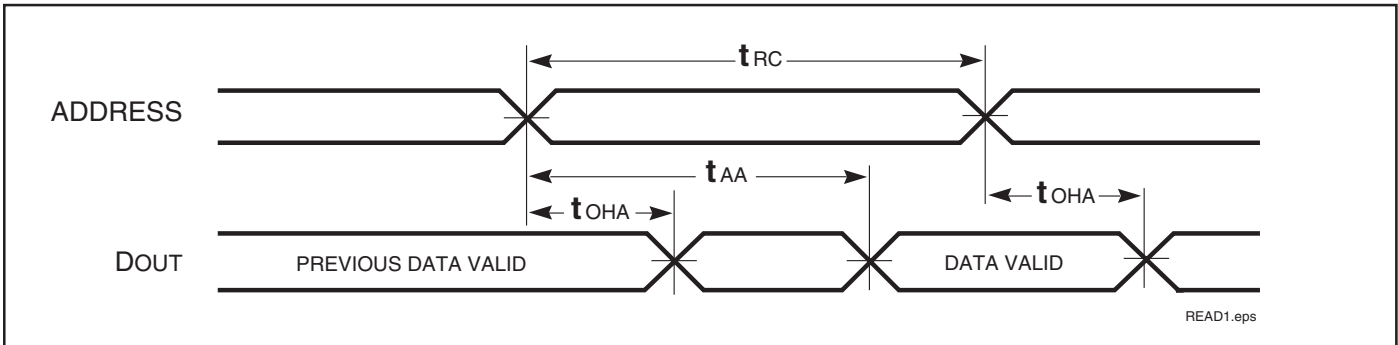
**AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

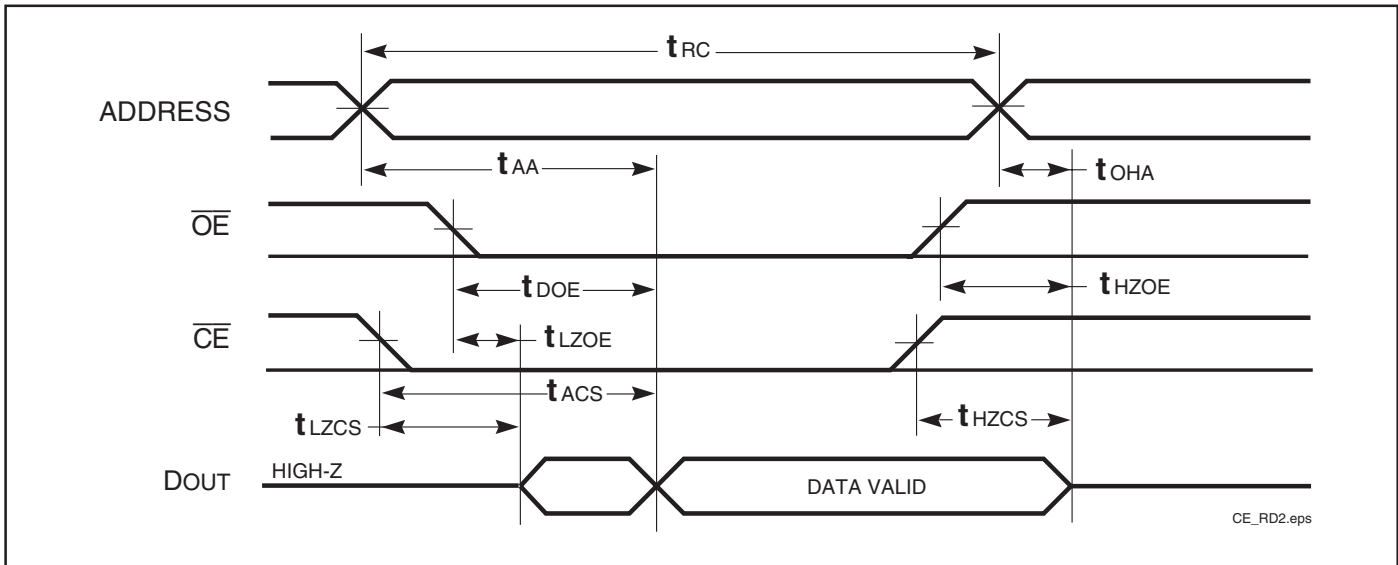
**AC TEST LOADS****Figure 1****Figure 2**

## AC WAVEFORMS

### READ CYCLE NO. 1<sup>(1,2)</sup>



### READ CYCLE NO. 2<sup>(1,3)</sup>



#### Notes:

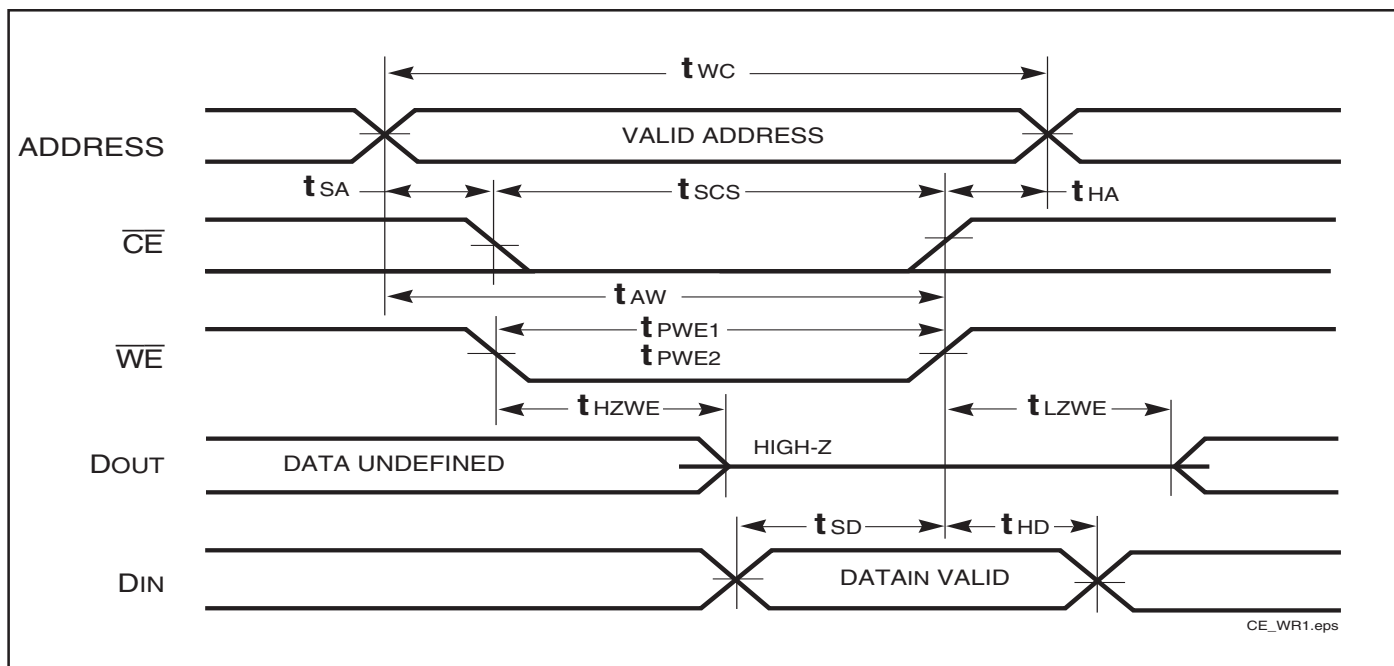
1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transitions.

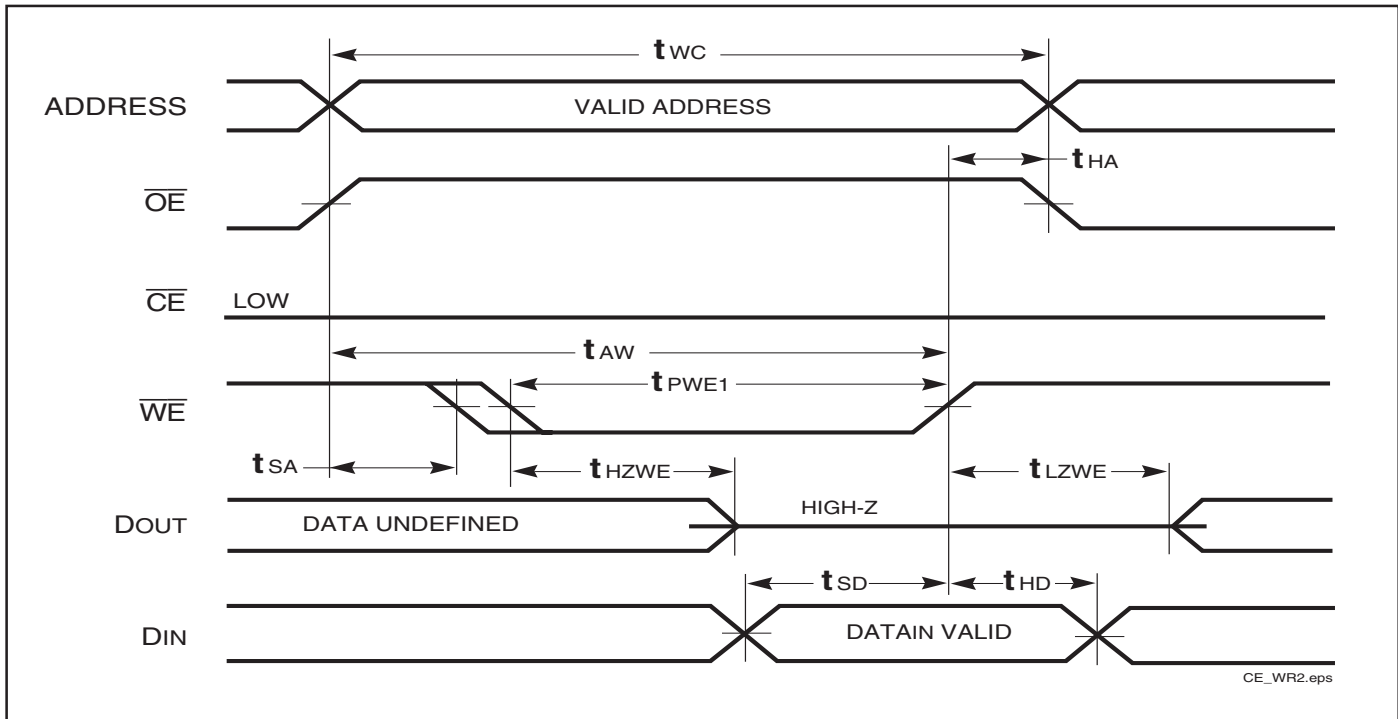
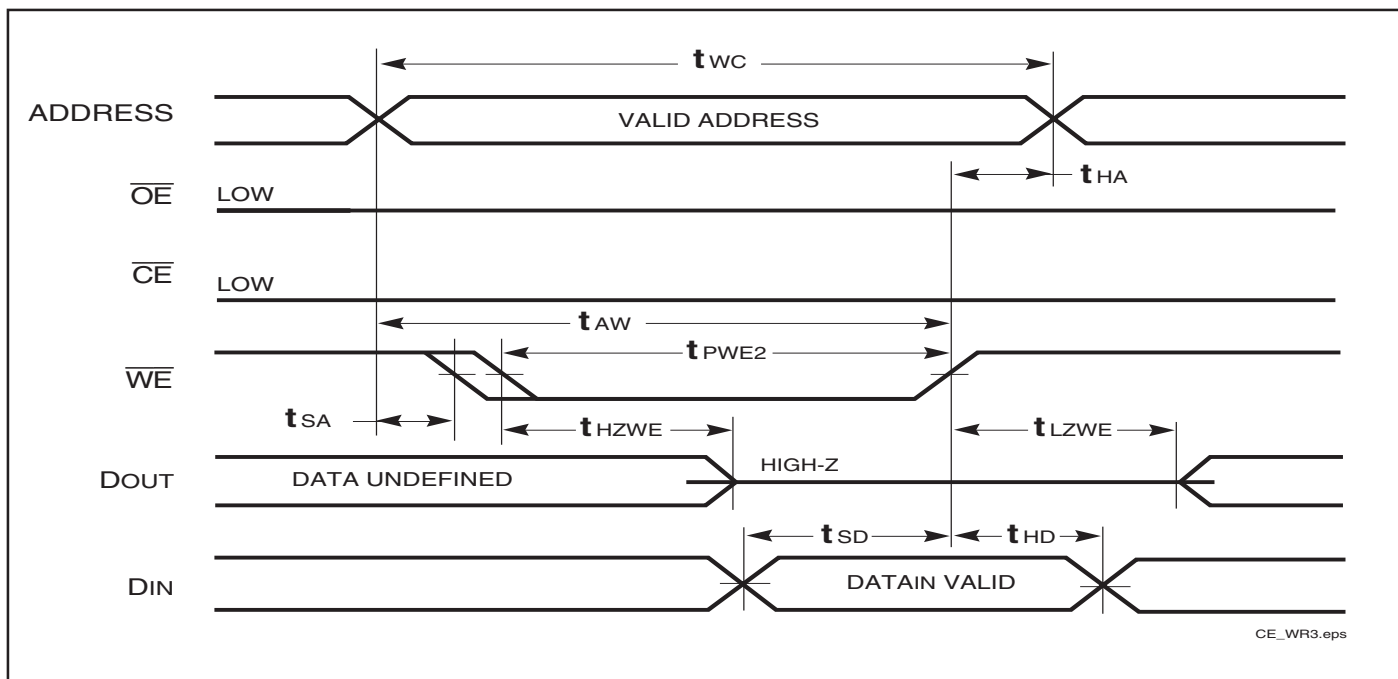
**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,3)</sup>** (Over Operating Range)

Symbol	Parameter	-10 ns		-12 ns		Unit
		Min.	Max	Min.	Max.	
$t_{WC}$	Write Cycle Time	10	—	12	—	ns
$t_{SCS}$	$\overline{CE}$ to Write End	9	—	10	—	ns
$t_{AW}$	Address Setup Time to Write End	9	—	10	—	ns
$t_{HA}$	Address Hold from Write End	0	—	0	—	ns
$t_{SA}$	Address Setup Time	0	—	0	—	ns
$t_{PWE1}$	$\overline{WE}$ Pulse Width ( $\overline{OE}$ LOW)	9	—	9	—	ns
$t_{PWE2}$	$\overline{WE}$ Pulse Width ( $\overline{OE}$ HIGH)	8	—	8	—	ns
$t_{SD}$	Data Setup to Write End	7	—	7	—	ns
$t_{HD}$	Data Hold from Write End	0	—	0	—	ns
$t_{HZWE}^{(2)}$	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	ns
$t_{LZWE}^{(2)}$	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

**AC WAVEFORMS****WRITE CYCLE NO. 1 ( $\overline{WE}$  Controlled)<sup>(1,2)</sup>**

**WRITE CYCLE NO. 2** ( $\overline{OE}$  is HIGH During Write Cycle) <sup>(1,2)</sup>**WRITE CYCLE NO. 3** ( $\overline{OE}$  is LOW During Write Cycle) <sup>(1)</sup>**Notes:**

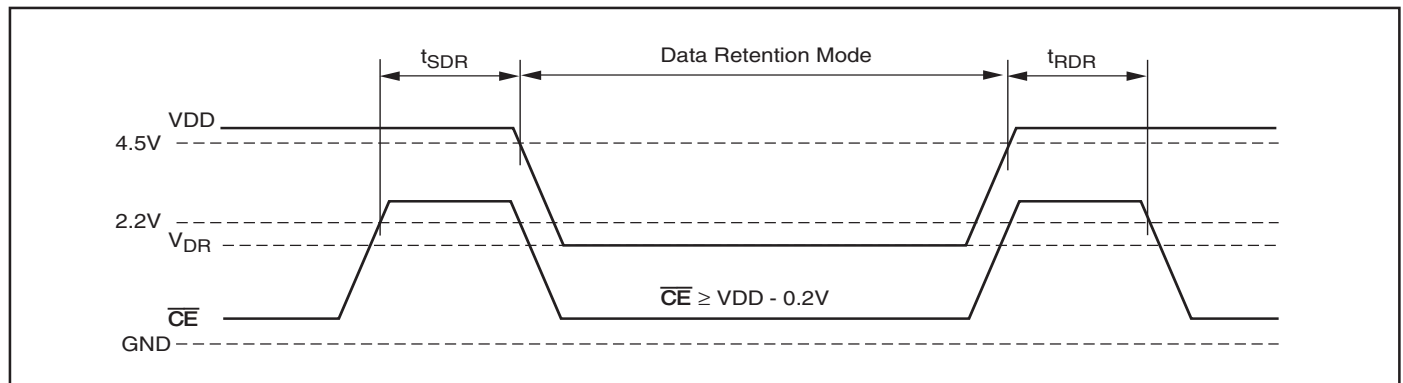
1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} \geq V_{IH}$ .

## DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{DR}$	$V_{DD}$ for Data Retention	See Data Retention Waveform	2.0		5.5	V
$I_{DR}$	Data Retention Current	$V_{DD} = 2.0V, \overline{CE} \geq V_{DD} - 0.2V$ $V_{IN} \geq V_{DD} - 0.2V$ , or $V_{IN} \leq V_{SS} + 0.2V$	—	50	90	$\mu A$
$t_{SDR}$	Data Retention Setup Time	See Data Retention Waveform	0		—	ns
$t_{RDR}$	Recovery Time	See Data Retention Waveform	$t_{RC}$		—	ns

**Note:**

1. Typical Values are measured at  $V_{DD} = 5V$ ,  $T_A = 25^\circ C$  and not 100% tested.

DATA RETENTION WAVEFORM ( $\overline{CE}$  Controlled)

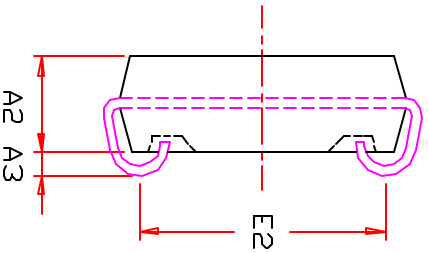
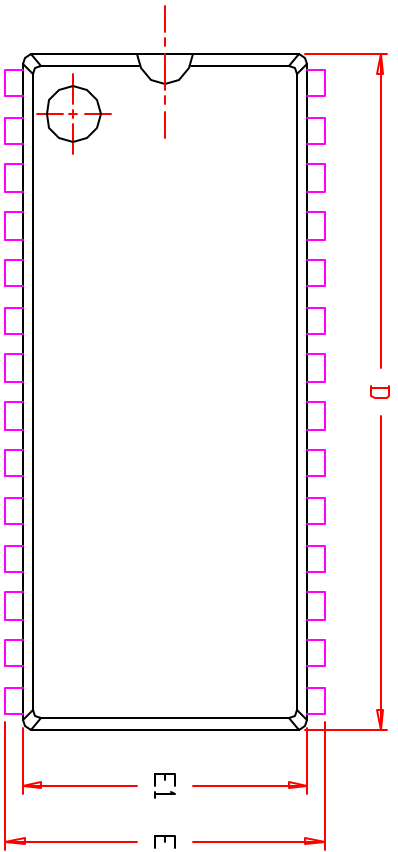




## ORDERING INFORMATION

Industrial Range: -40°C to +85°C

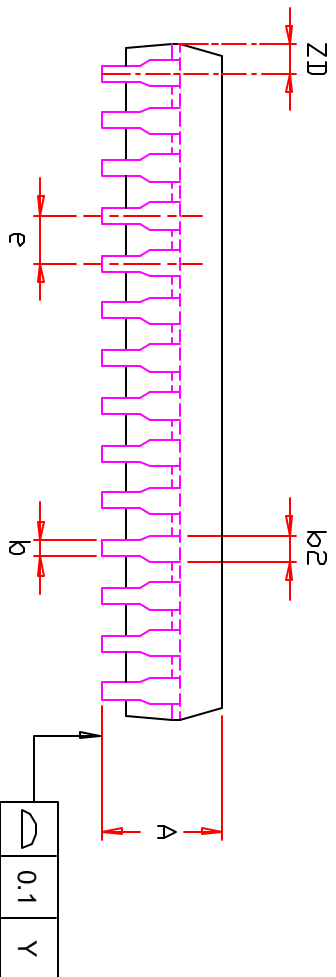
Speed (ns)	Order Part No.	Package
10	IS61C64AL-10JLI	300-mil Plastic SOJ, Lead-free
	IS61C64AL-10TLI	Plastic TSOP, Lead-free



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	3.05		3.76
A2	2.41	2.54	2.67
A3	0.64		1.09
k	0.36		0.56
k2	0.66		0.81
D	17.70		18.54
E	8.26	8.56	8.81
E1	7.42		7.75
E2	6.22		7.29
e	1.27 BSC		
ZD	0.95 REF.		
Y	0.1		

# **NOTE :**

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intursion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.



**ISSI**

**TITLE**

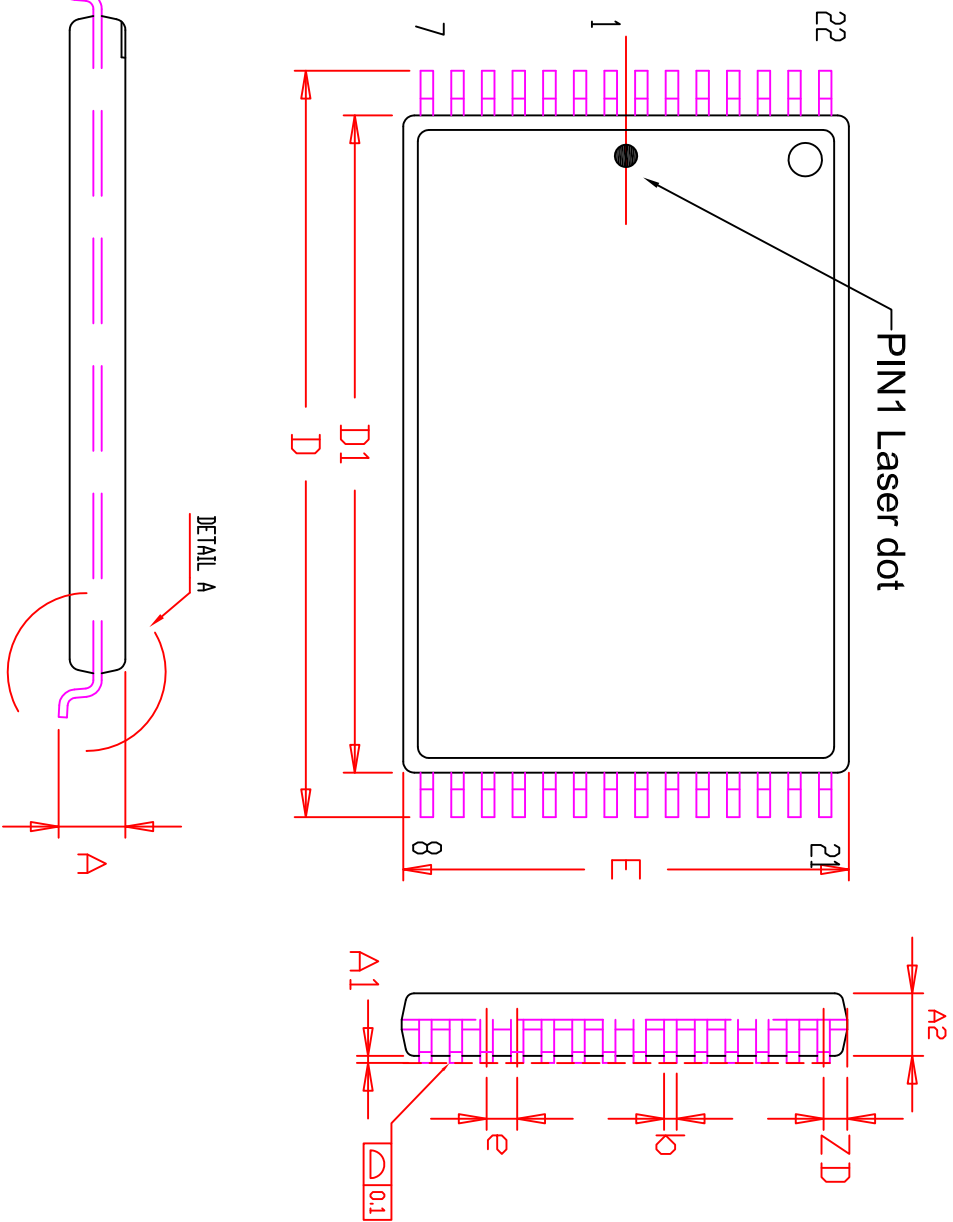
**28L 300mil SOJ**  
Package Outline

**REV.**

**C**

**DATE**

07/05/2006



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95		1.20	0.037		0.047
A1	0.05		0.20	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
D	13.20	13.40	13.60	0.520	0.528	0.535
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.55 BSC.			0.022 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.425 REF.			0.017 REF.		
Θ	0	3°	5°	0	3°	5°
C	0.12		0.21	0.12		0.21

# NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183

DETAIL A

DETAIL A



TITLE

28L 8x13.4mm TSOP-1  
Package Outline

REV.

G

DATE

10/28/2019