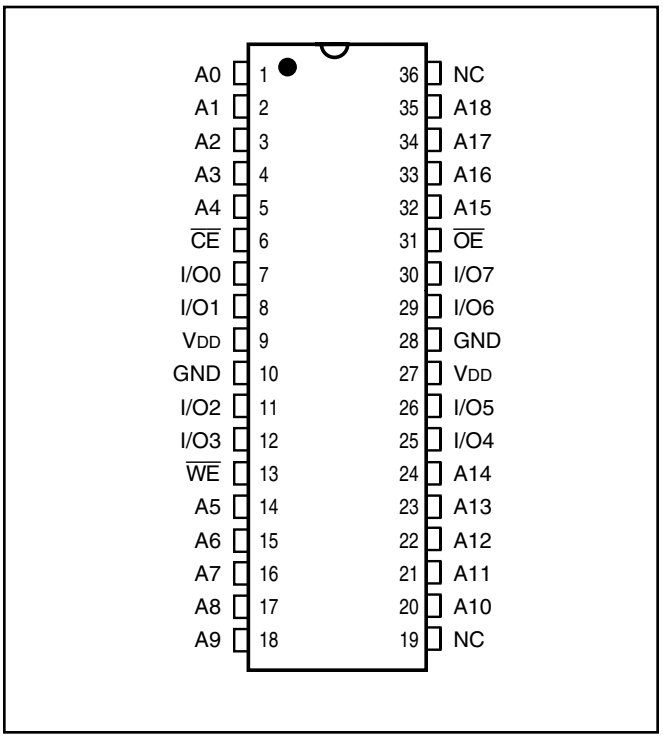
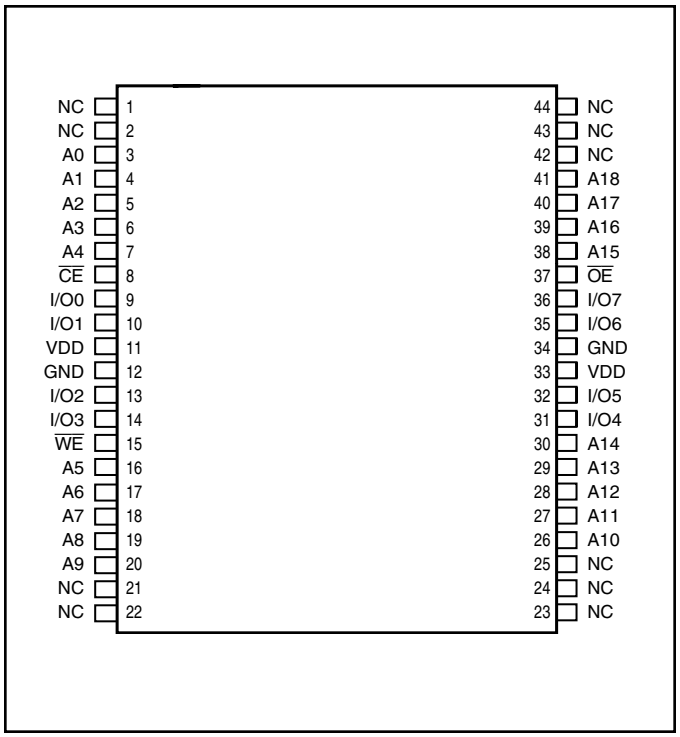
HIGH SPEED (IS61/64C5128AL) PIN CONFIGURATION

36-Pin SOJ (400-mil)



44-Pin TSOP (Type II)

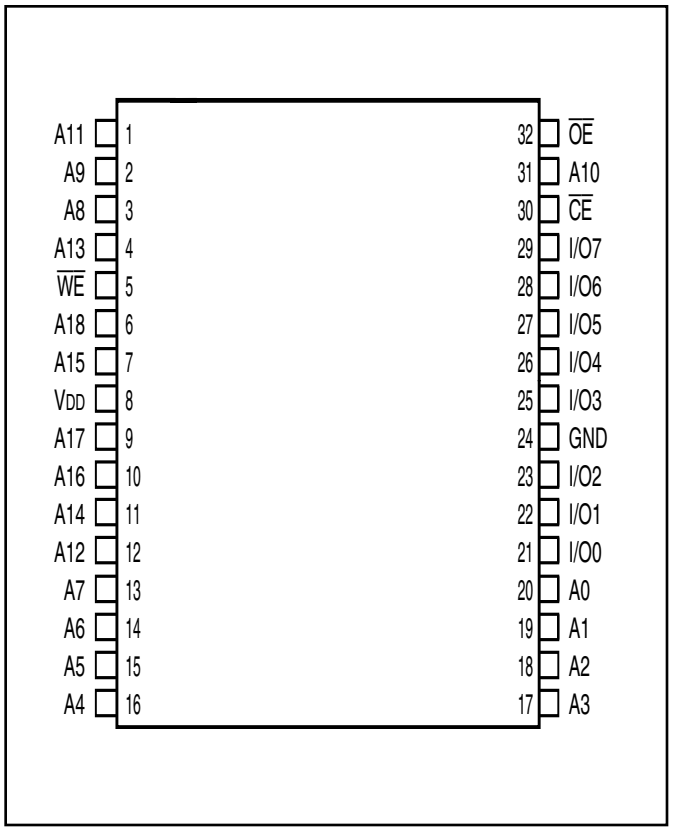


PIN DESCRIPTIONS

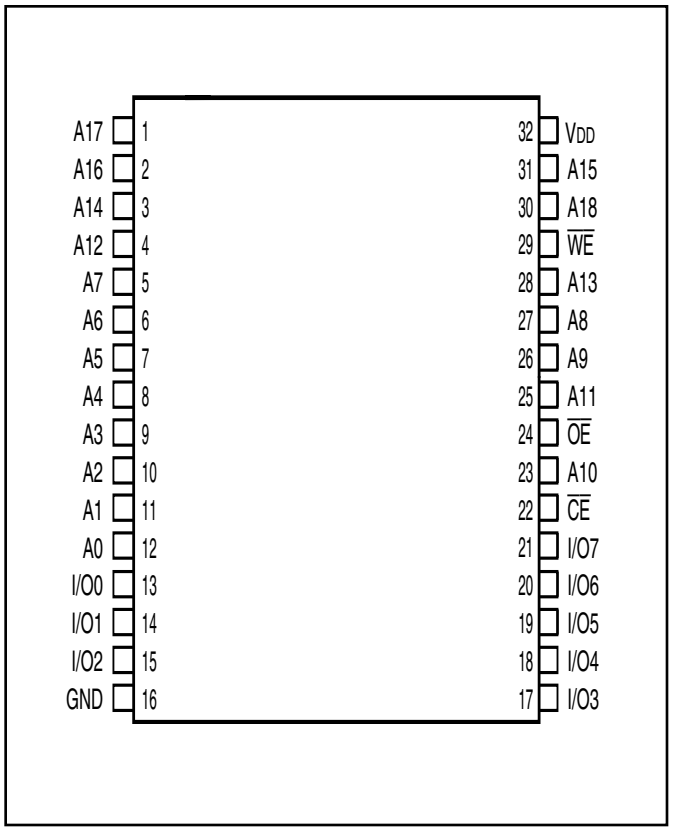
A0-A18	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Bidirectional Ports
V_{DD}	Power
GND	Ground
NC	No Connection

LOW POWER (IS61/64C5128AS) PIN CONFIGURATION

32-pin sTSOP (TYPE I)



32-pin SOP
32-pin TSOP (TYPE II)



PIN DESCRIPTIONS

A0-A18	Address Inputs
$\overline{CE}$	Chip Enable 1 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
VDD	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O PIN I/O0-I/O7	I/O PIN V_{DD} Current
Not Selected	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage(1)			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	Com.	–1	1	µA
			Ind.	–2	2	
			Auto.	–5	5	
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}	Com.	–1	1	µA
		Outputs Disabled	Ind.	–2	2	
			Auto.	–5	5	

Note: 1. V_{IL} = –3.0V for pulse width less than 10 ns.

OPERATING RANGE: HIGH SPEED OPTION (IS61/64C5128AL)

Range	Ambient Temperature	V_{DD}	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	10
Industrial	-40°C to +85°C	5V ± 10%	10
Automotive	-40°C to +125°C	5V ± 10%	12

OPERATING RANGE: LOW POWER OPTION (IS61/64C5128AS)

Range	Ambient Temperature	V_{DD}	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	25
Industrial	-40°C to +85°C	5V ± 10%	25
Automotive	-40°C to +125°C	5V ± 10%	25

HIGH SPEED OPTION (IS61/64C5128AL)

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	Unit
I_{CC1}	V_{DD} Operating Supply Current	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} = V_{IL}$, I_{OUT} = 0 mA, f = 0	Com.	—	45	—	45	mA
			Ind.	—	50	—	50	
			Auto.	—	55	—	55	
I_{CC2}	V_{DD} Dynamic Operating Supply Current	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} = V_{IL}$, I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	50	—	45	mA
			Ind.	—	55	—	50	
			Auto.	—	70	—	60	
			typ.[2]		30		25	
I_{SB1}	TTL Standby Current (TTL Inputs)	$V_{DD} = V_{DD\ MAX.}$, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	15	—	15	mA
			Ind.	—	20	—	20	
			Auto.	—	30	—	30	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} \leq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com.	—	8	—	8	mA
			Ind.	—	12	—	12	
			Auto.	—	20	—	20	
			typ.[2]		2			

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25% and not 100% tested.

LOW POWER OPTION (IS61/64C5128AS)

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-25 ns Min.	-25 ns Max.	Unit
I_{CC}	Average operating Current	$\overline{CE} = V_{IL}$, V_{DD} = Max., I_{OUT}= 0 mA, f= 0	Com.	—	10	mA
			Ind.	—	15	
			Auto.	—	20	
I_{CC1}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., $\overline{CE} = V_{IL}$, I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	25	mA
			Ind.	—	30	
			Auto.	—	40	
			typ.[2]		15	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	1	mA
			Ind.	—	1.5	
			Auto.	—	2	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$, f = 0	Com.	—	0.8	mA
			Ind.	—	0.9	
			Auto.	—	2	
			typ.		0.2	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25% and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-25 Min.	-25 Max.	Unit
t_{RC}	Read Cycle Time	10	—	12	—	25	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	25	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	10	—	12	—	25	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	6	—	15	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	5	0	6	0	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	2	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	5	0	6	0	8	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	2	—	2	—	2	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

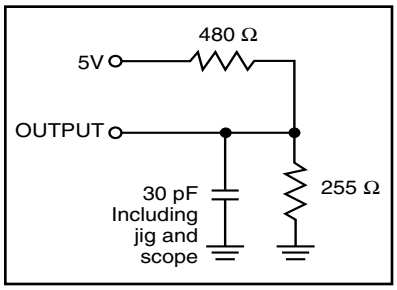


Figure 1

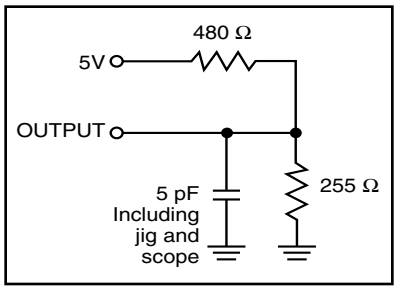
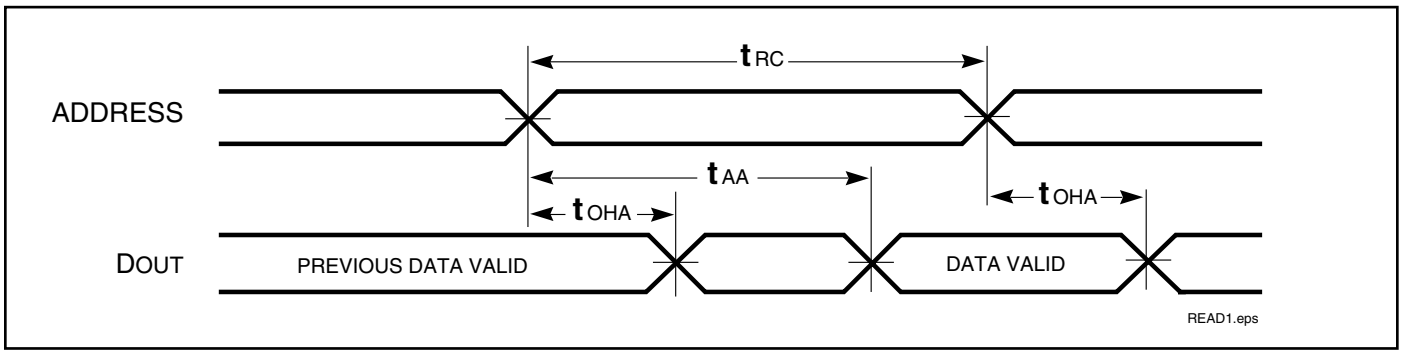


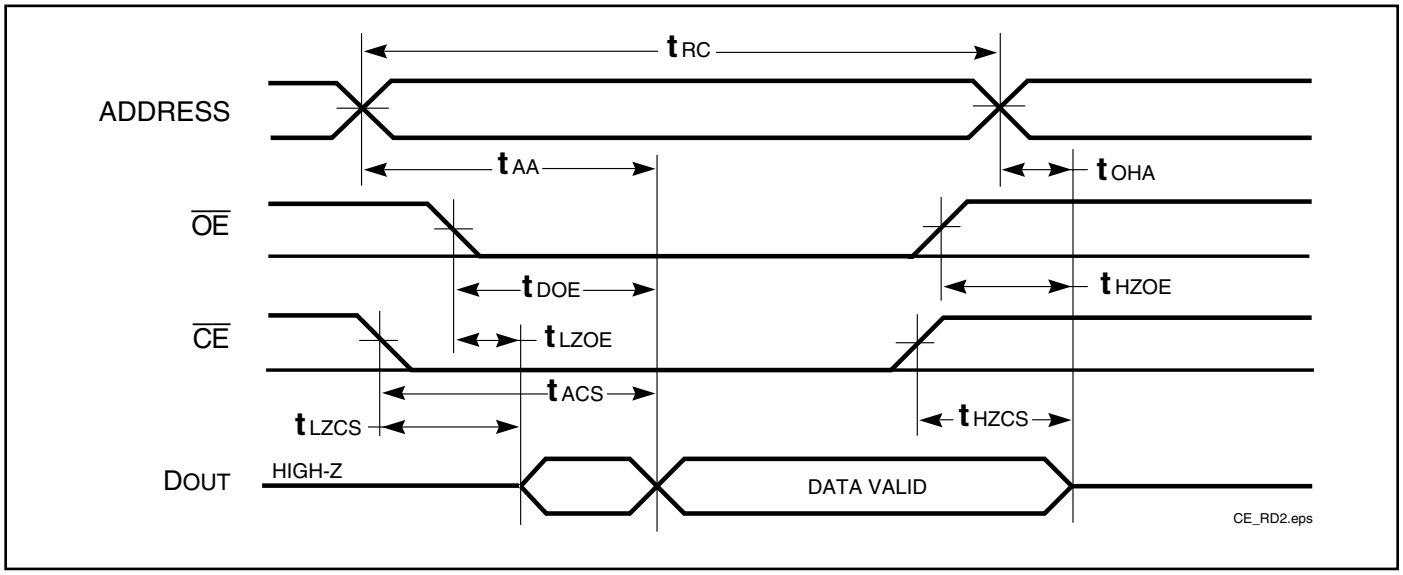
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



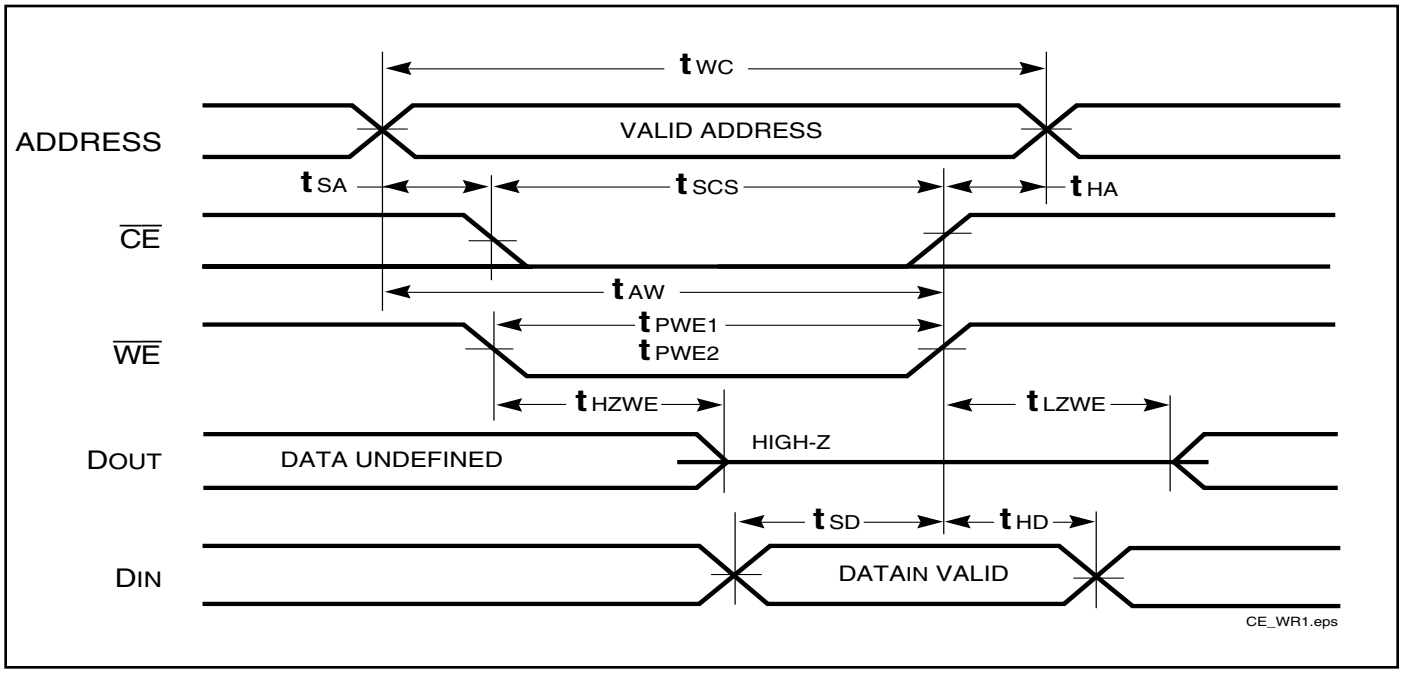
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-25 Min.	-25 Max.	Unit
t_{WC}	Write Cycle Time	10	—	12	—	25	—	ns
t_{SCE}	$\overline{CE}$ to Write End	7	—	9	—	18	—	ns
t_{AW}	Address Setup Time to Write End	7	—	9	—	18	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =High)	7	—	9	—	15	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$=Low)	7	—	9	—	15	—	ns
t_{SD}	Data Setup to Write End	6	—	6	—	15	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	—	15	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	5	—	ns

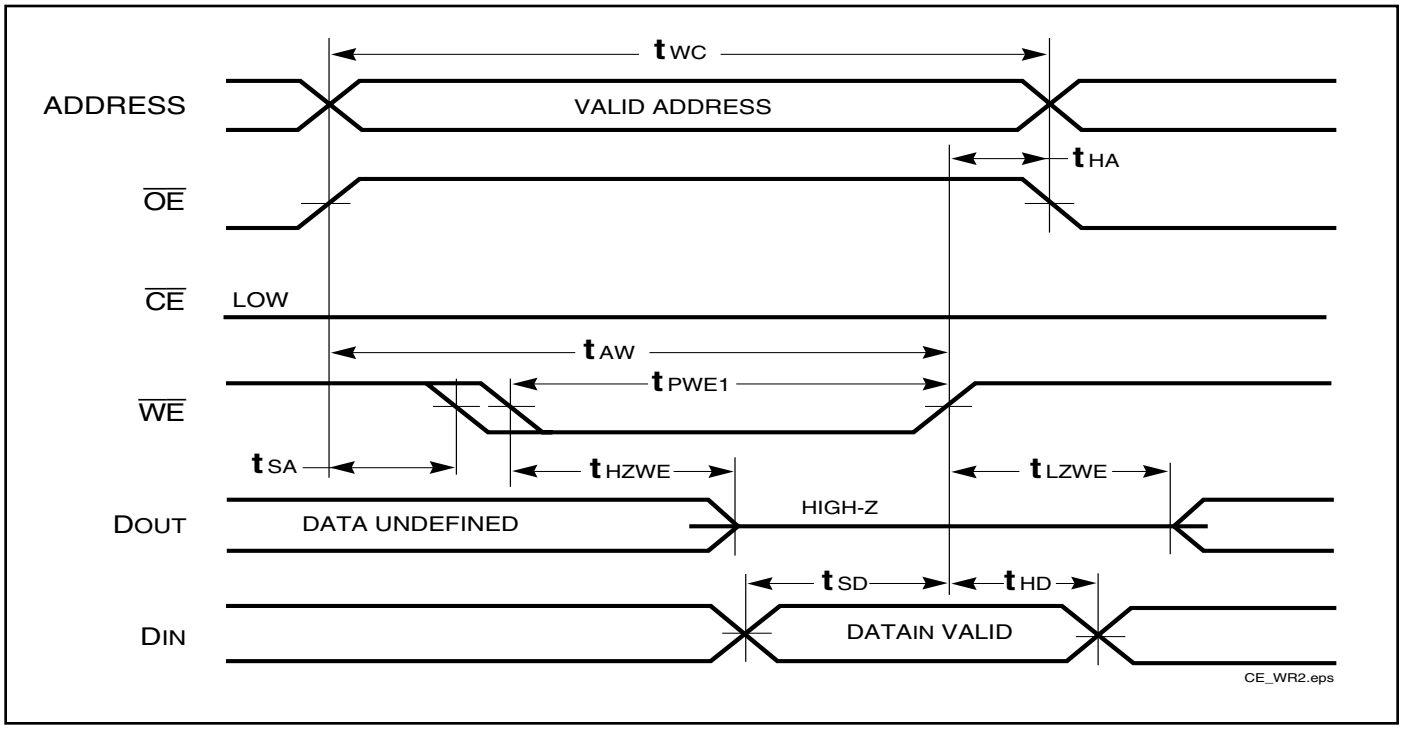
Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]

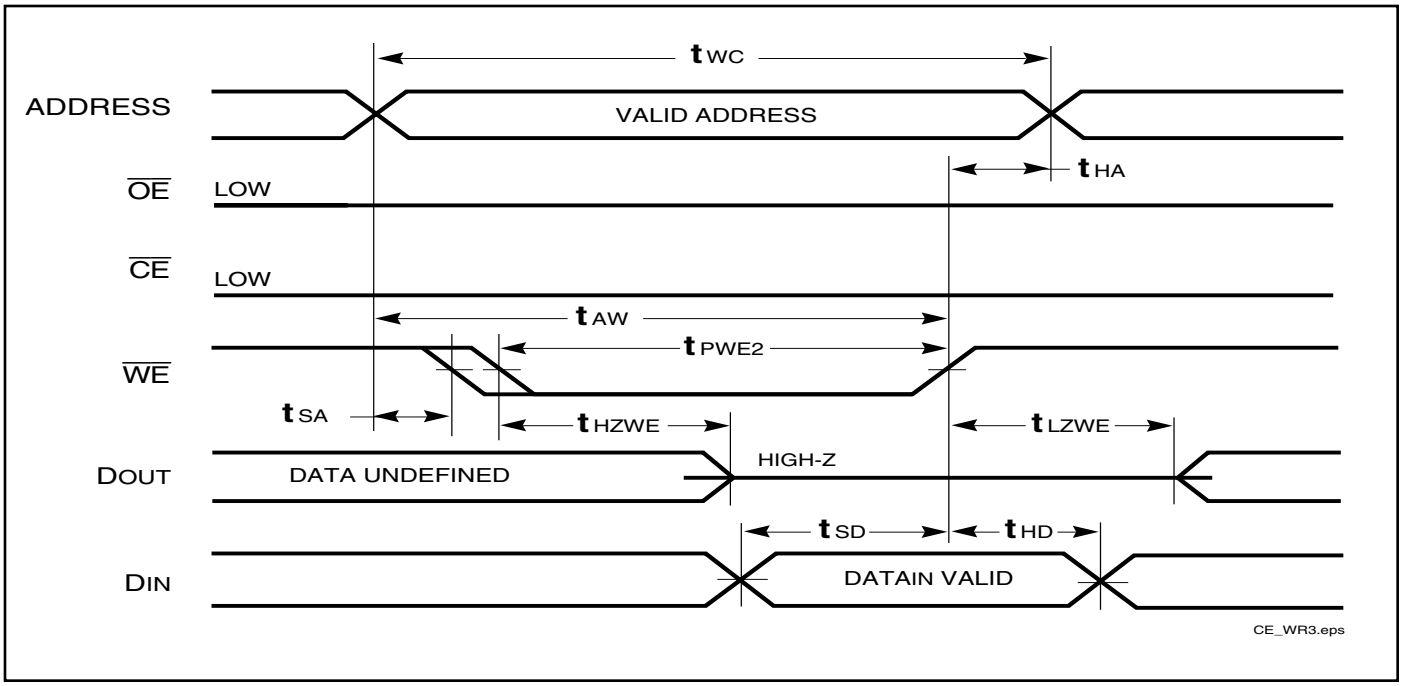


Notes:
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) [1,2]



WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) [1]



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

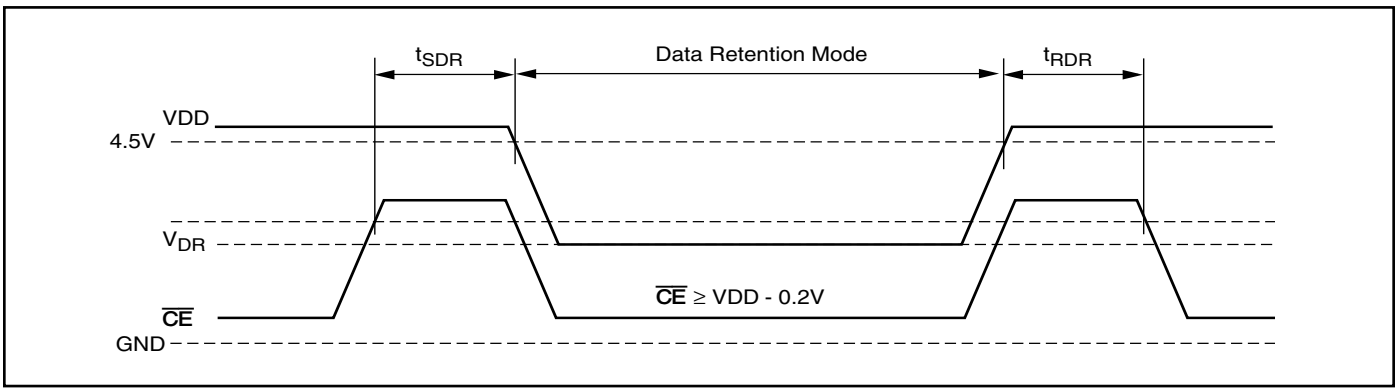
DATA RETENTION SWITCHING CHARACTERISTICS (HIGH SPEED) (IS61/64C5128AL)

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.9	5.5	V
I_{DR}	Data Retention Current	V_{DD} = 2.9V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	8	mA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Ind.	—	10	
			Auto.	—	15	
			typ. (1)	1		
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

Note:

1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



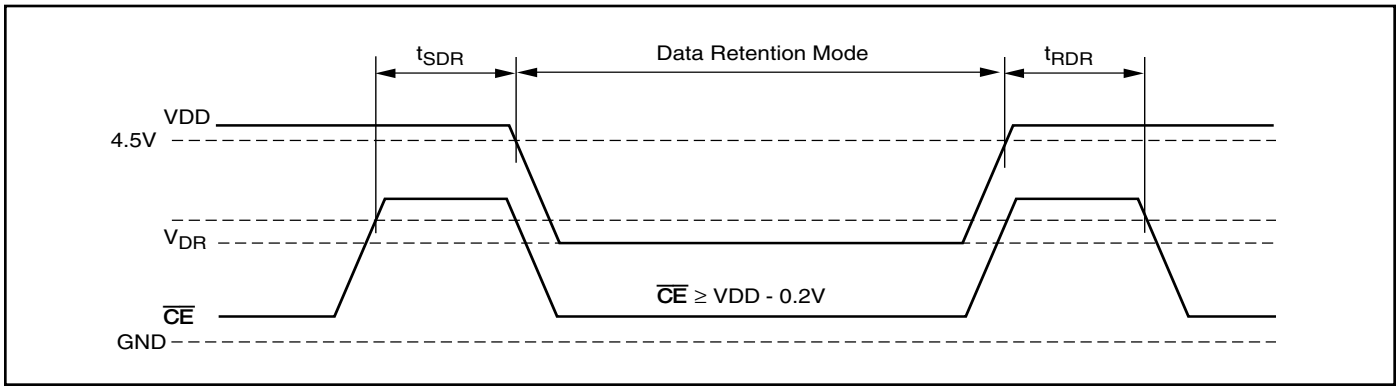
DATA RETENTION SWITCHING CHARACTERISTICS (LOW POWER) (IS61/64C5128AS)

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.9	5.5	V
I_{DR}	Data Retention Current	V_{DD} = 2.9V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	0.8	mA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Ind.	—	0.9	
			Auto.	—	2	
			typ. (1)	0.2		
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

Note:

1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



HIGH SPEED (IS61/64C5128AL)

ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS61C5128AL-10KLI	400-mil Plastic SOJ, Lead-free
	IS61C5128AL-10TLI	44-pin TSOP-II, Lead-free

Automotive Range: –40°C to +125°C

Speed (ns)	Order Part No.	Package
12	IS64C5128AL-12KLA3	400-mil Plastic SOJ, Lead-free
	IS64C5128AL-12CTLA3	44-pin TSOP-II, Lead-free, Copper Leadframe

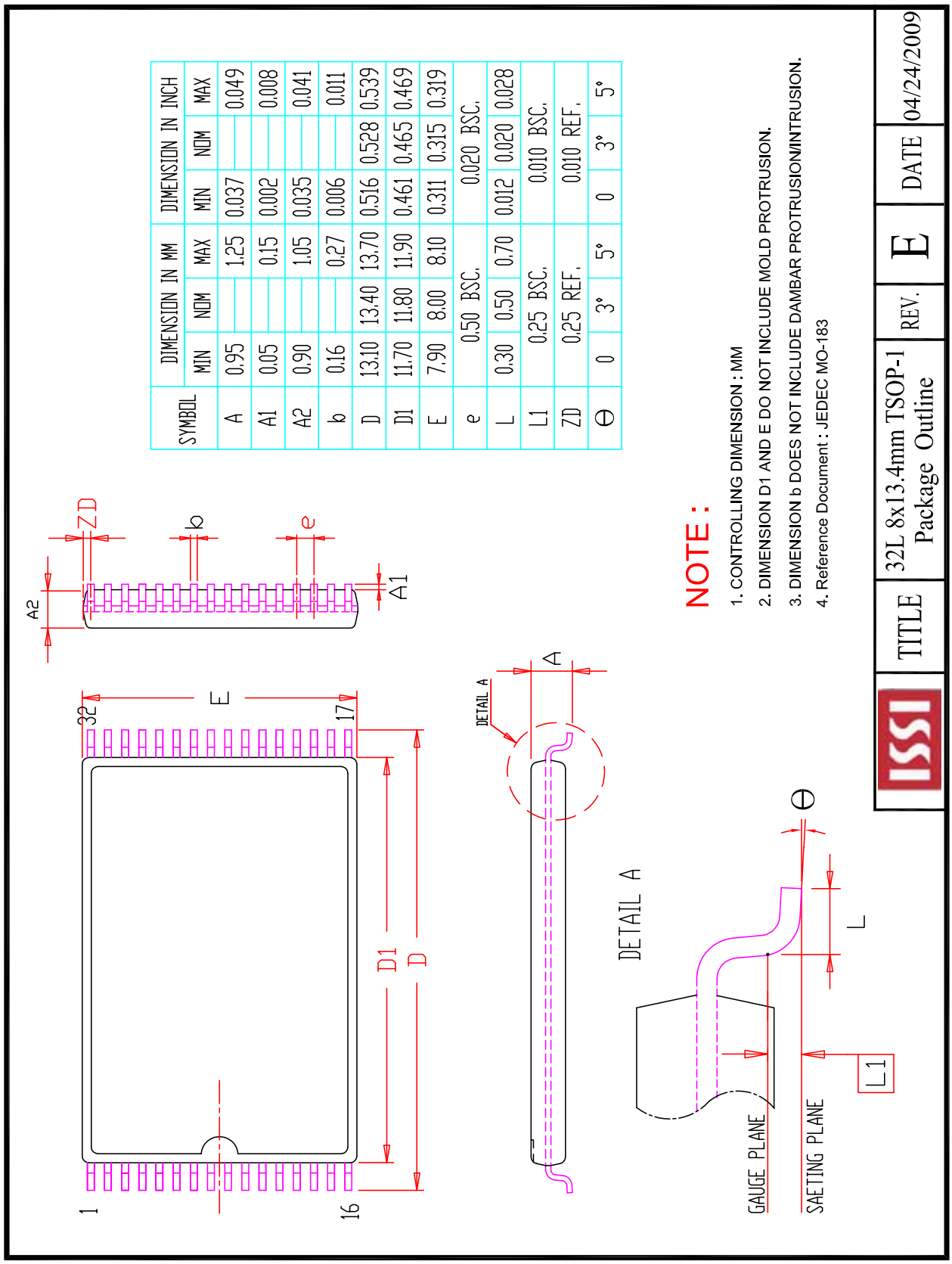
LOW POWER (IS61/64C5128AS)

ORDERING INFORMATION

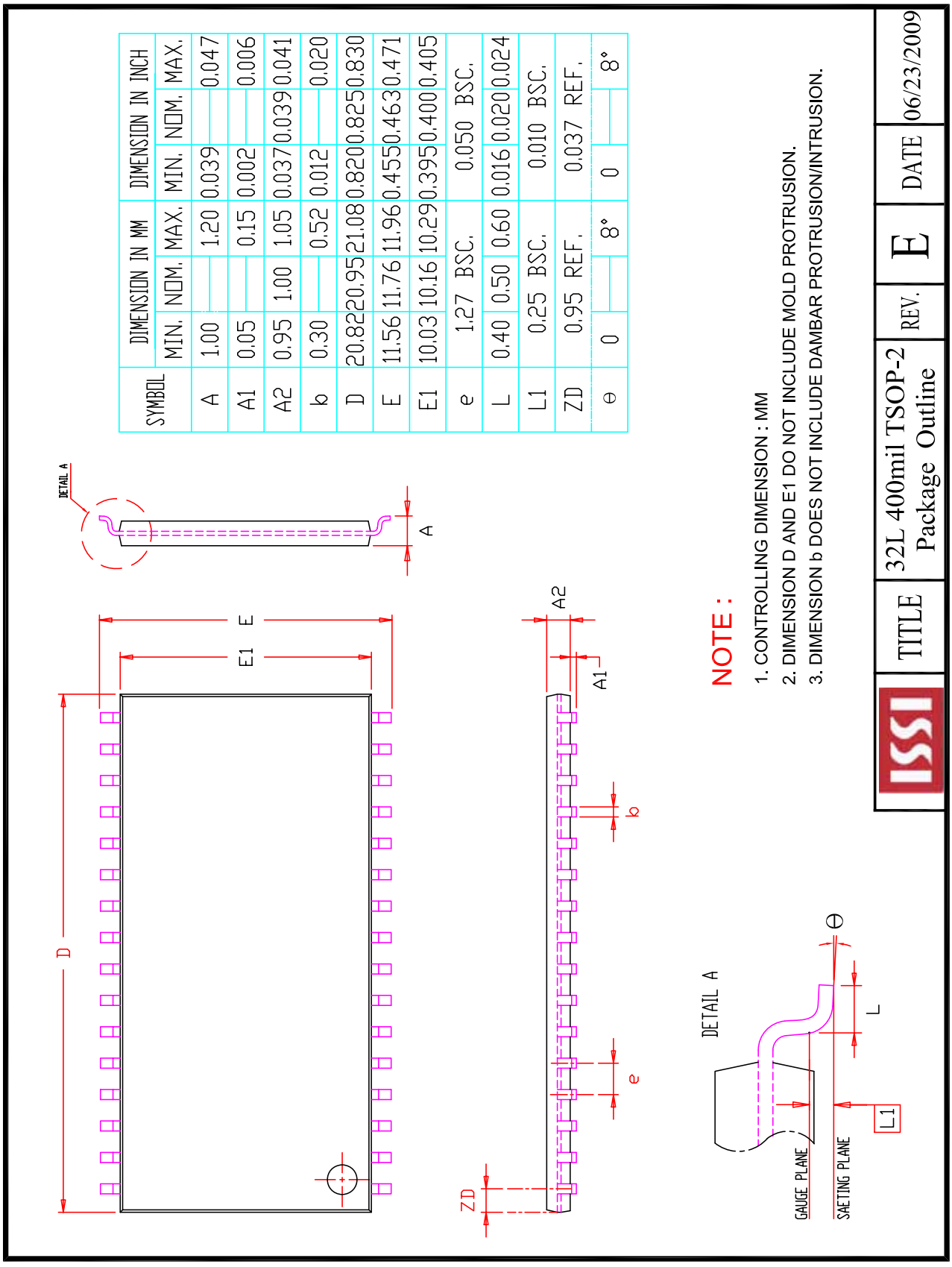
Industrial Range: –40°C to +85°C

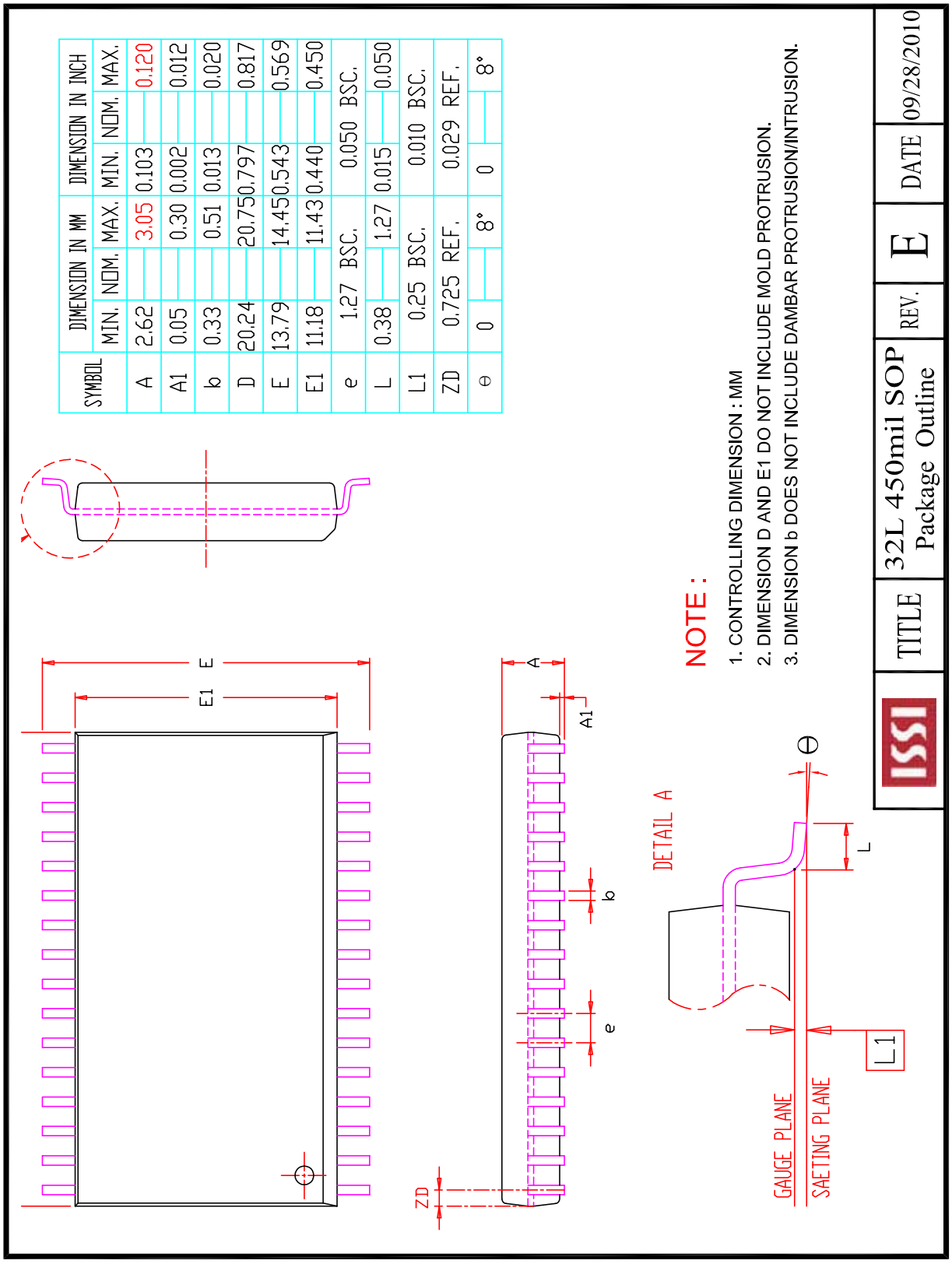
Speed (ns)	Order Part No.	Package
25	IS61C5128AS-25QLI	450-mil Plastic SOP, Lead-free
	IS61C5128AS-25HLI	32-pin STSOP-I, Lead-free
	IS61C5128AS-25TLI	32-pin TSOP-II, Lead-free

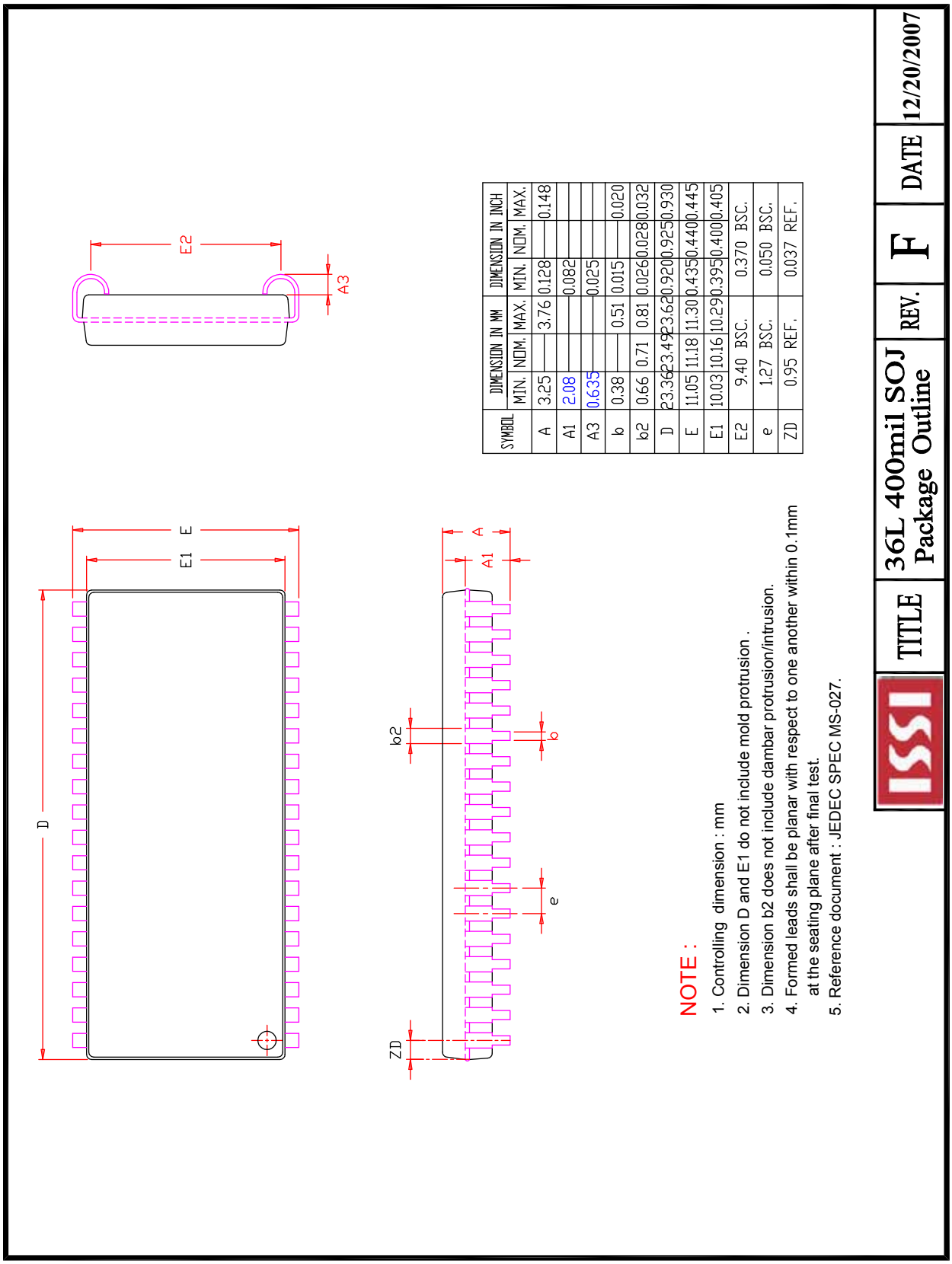
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95	----	1.25	0.037	----	0.049
A1	0.05	----	0.15	0.002	----	0.008
A2	0.90	----	1.05	0.035	----	0.041
b	0.16	----	0.27	0.006	----	0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
Θ	0	3°	5°	0	3°	5°



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.52	0.012	—	0.020
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	1.27 BSC.			0.050 BSC.		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BSC.			0.010 BSC.		
ZD	0.95 REF.			0.037 REF.		
θ	0	—	8°	0	—	8°







SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.25	——	3.76	0.128	——	0.148
A1	2.08	——	——	0.082	——	——
A3	0.635	——	——	0.025	——	——
b	0.38	——	0.51	0.015	——	0.020
b2	0.66	0.71	0.81	0.026	0.028	0.032
D	23.36	23.49	23.62	0.920	0.925	0.930
E	11.05	11.18	11.30	0.435	0.440	0.445
E1	10.03	10.16	10.29	0.395	0.400	0.405
E2	9.40 BSC.			0.370 BSC.		
e	1.27 BSC.			0.050 BSC.		
ZD	0.95 REF.			0.037 REF.		

NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
5. Reference document : JEDEC SPEC MS-027.

	TITLE	36L 400mil SOJ Package Outline	REV.	F	DATE	12/20/2007

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	—	0.69	0.016	—	0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
θ	0	—	8°	0	—	8°