

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	338 <sup>①</sup>	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	239	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	240	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	1450	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	375	W
	Linear Derating Factor	2.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>③</sup>	526	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>④</sup>	1029	
$I_{AR}$	Avalanche Current <sup>②</sup>	See Fig 14, 15, 23a, 23b	A
$E_{AR}$	Repetitive Avalanche Energy <sup>②</sup>		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case <sup>⑧</sup>	—	0.40	°C/W
$R_{\theta JA}$	Junction-to-Ambient <sup>⑩</sup>	—	40	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	33	—	mV/°C	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$ <sup>②</sup>
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.15	1.4	mΩ	$V_{GS} = 10\text{V}$ , $I_D = 100\text{A}$
		—	1.4	—	mΩ	$V_{GS} = 6.0\text{V}$ , $I_D = 50\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.1	—	3.7	V	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 60\text{V}$ , $V_{GS} = 0\text{V}$
		—	—	150	μA	$V_{DS} = 60\text{V}$ , $V_{GS} = 0\text{V}$ , $T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20\text{V}$
$R_G$	Gate Resistance	—	2.2	—	Ω	

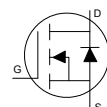
**Notes:**

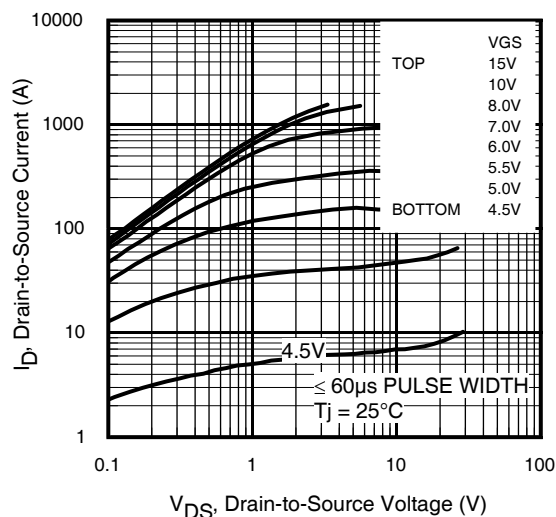
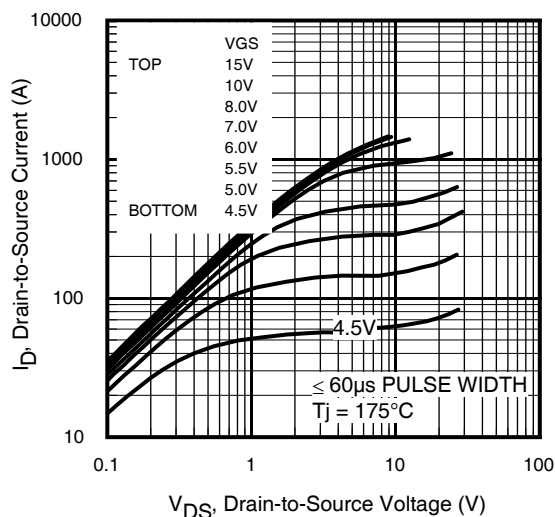
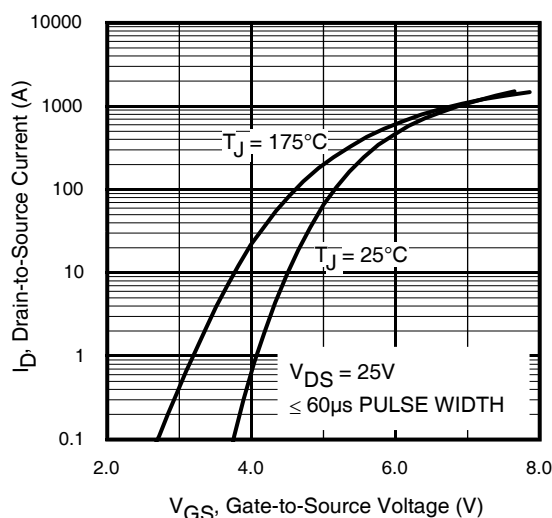
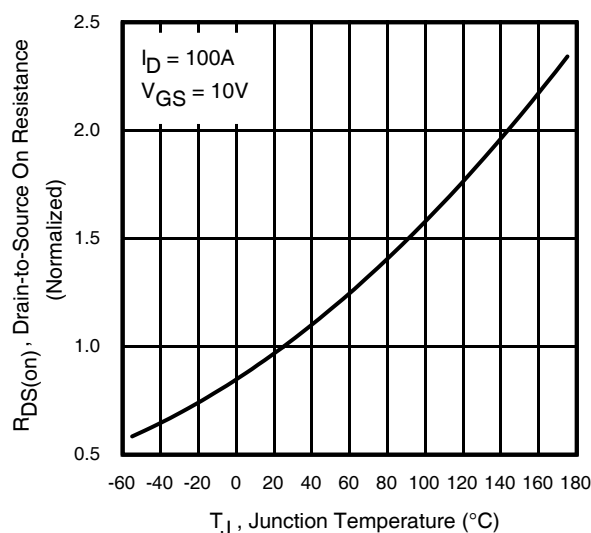
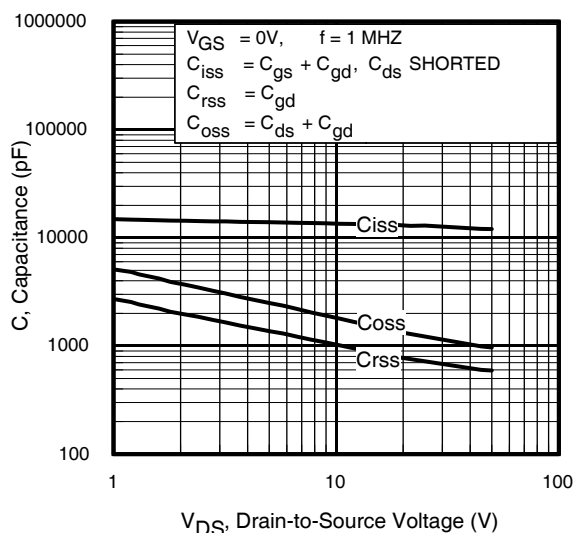
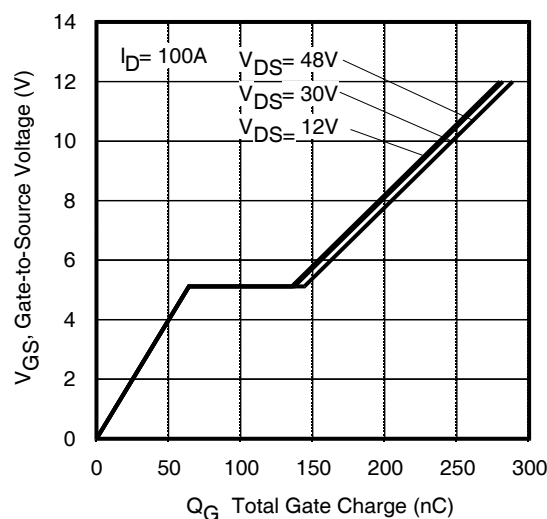
- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 105\mu\text{H}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 100\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ④  $I_{SD} \leq 100\text{A}$ ,  $di/dt \leq 1575\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑥  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑧  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑨ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 45\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ⑩ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994: <http://www.irf.com/technical-info/appnotes/an-994.pdf>

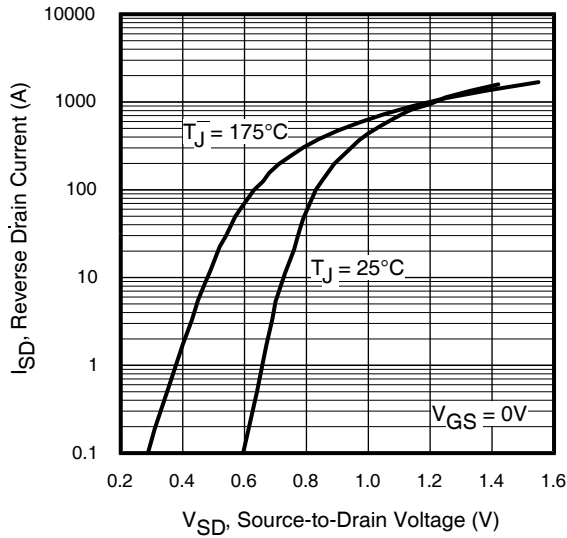
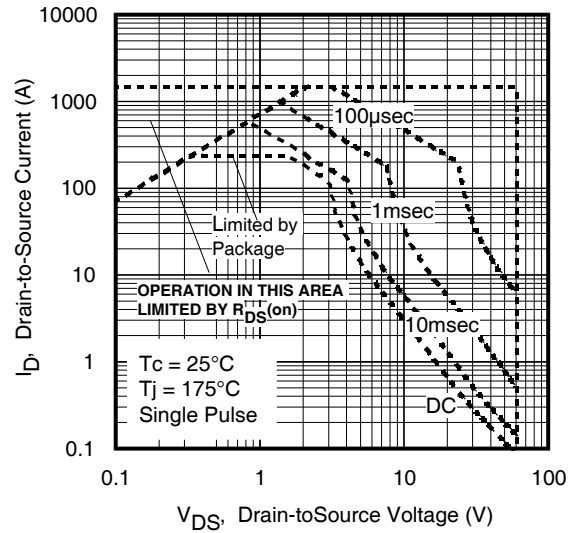
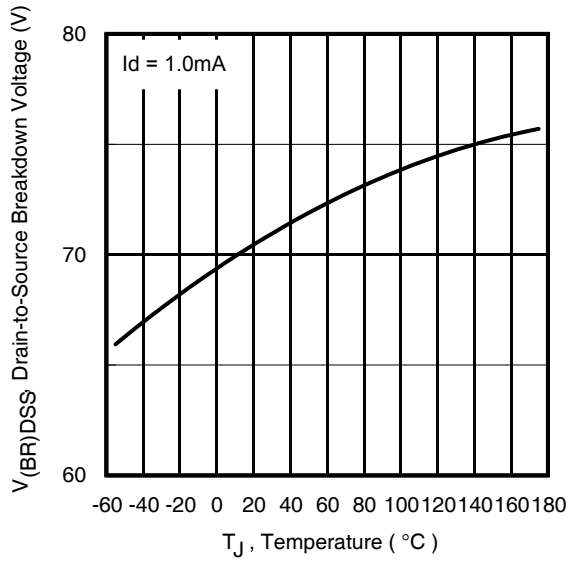
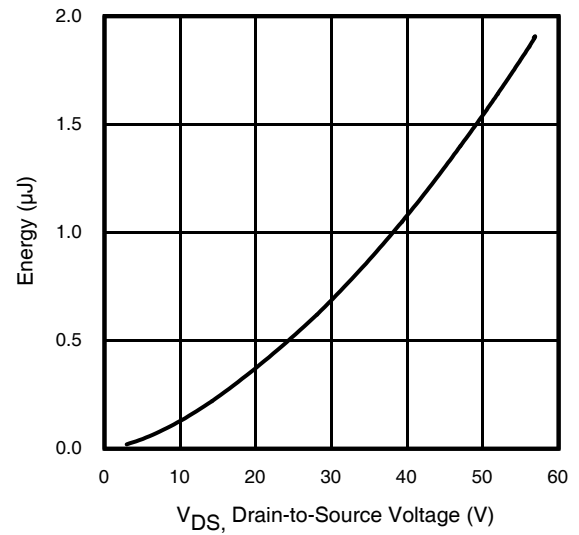
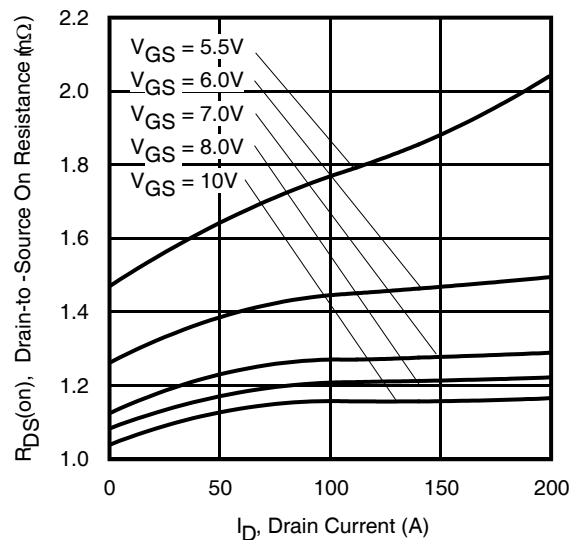
**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	249	—	—	S	$V_{DS} = 10\text{V}$ , $I_D = 100\text{A}$
$Q_g$	Total Gate Charge	—	236	354	nC	$I_D = 100\text{A}$ $V_{DS} = 30\text{V}$ $V_{GS} = 10\text{V}$
$Q_{gs}$	Gate-to-Source Charge	—	62	—		
$Q_{gd}$	Gate-to-Drain Charge	—	73	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	163	—		
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	$V_{DD} = 30\text{V}$ $I_D = 100\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 10\text{V}^{(5)}$
$t_r$	Rise Time	—	102	—		
$t_{d(off)}$	Turn-Off Delay Time	—	168	—		
$t_f$	Fall Time	—	79	—		
$C_{iss}$	Input Capacitance	—	12960	—	pF	$V_{GS} = 0\text{V}$
$C_{oss}$	Output Capacitance	—	1270	—		$V_{DS} = 25\text{V}$
$C_{rss}$	Reverse Transfer Capacitance	—	760	—		$f = 1.0\text{MHz}$
$C_{oss\text{ eff.}(ER)}$	Effective Output Capacitance (Energy Related)	—	1248	—		$V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $48\text{V}^{(7)}$
$C_{oss\text{ eff.}(TR)}$	Output Capacitance (Time Related)	—	1590	—		$V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $48\text{V}^{(6)}$

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode) <sup>(1)</sup>	—	—	338 <sup>(1)</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) <sup>(1)</sup>	—	—	1450		
$V_{SD}$	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$ , $I_S = 100\text{A}$ , $V_{GS} = 0\text{V}^{(5)}$
$dv/dt$	Peak Diode Recovery $dv/dt$ <sup>(4)</sup>	—	8.5	—	V/ns	$T_J = 175^\circ\text{C}$ , $I_S = 100\text{A}$ , $V_{DS} = 60\text{V}^{(5)}$
$t_{rr}$	Reverse Recovery Time	—	48	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 51\text{V}$
		—	50	—		$T_J = 125^\circ\text{C}$ $I_F = 100\text{A}$ ,
$Q_{rr}$	Reverse Recovery Charge	—	72	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}^{(5)}$
		—	83	—		$T_J = 125^\circ\text{C}$
$I_{RRM}$	Reverse Recovery Current	—	2.5	—	A	$T_J = 25^\circ\text{C}$


**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs.**

**Fig 8. Typical Gate Charge vs.  
Gate-to-Source Voltage**


**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 12.** Typical  $C_{oss}$  Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current

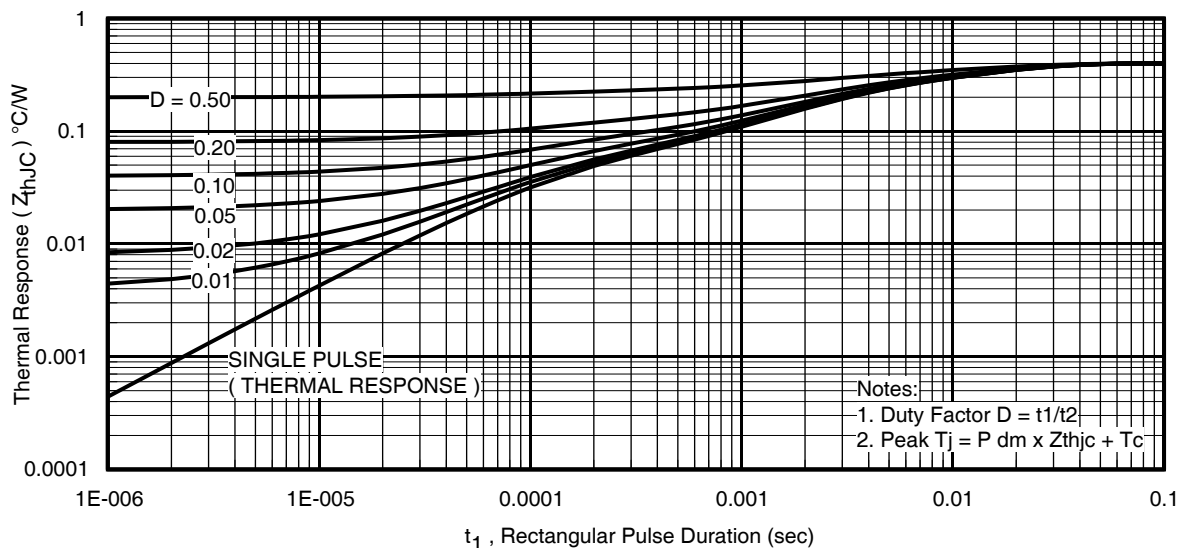


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

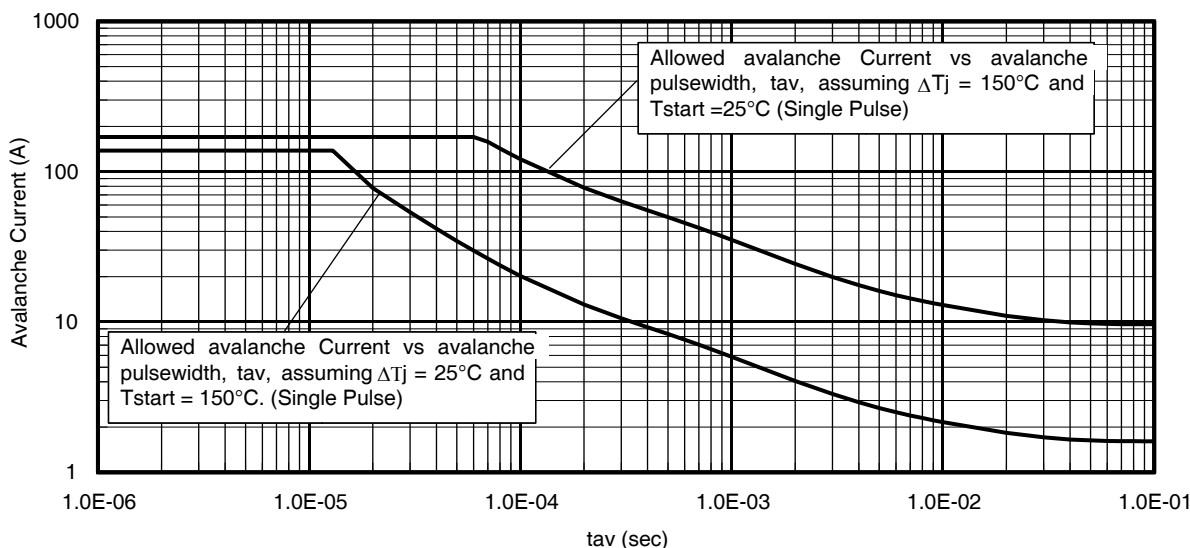


Fig 15. Avalanche Current vs. Pulse Width

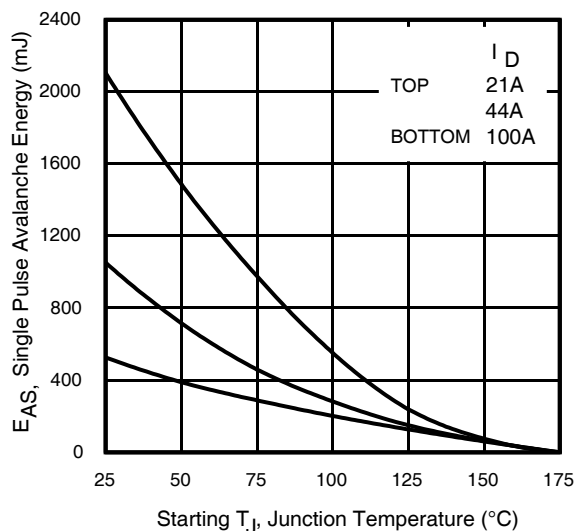
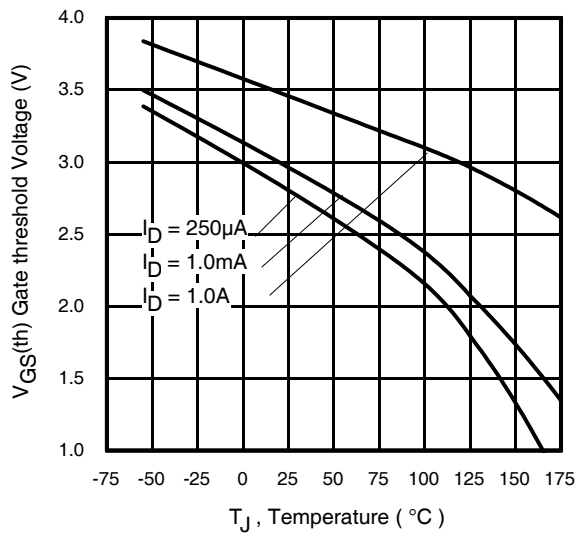
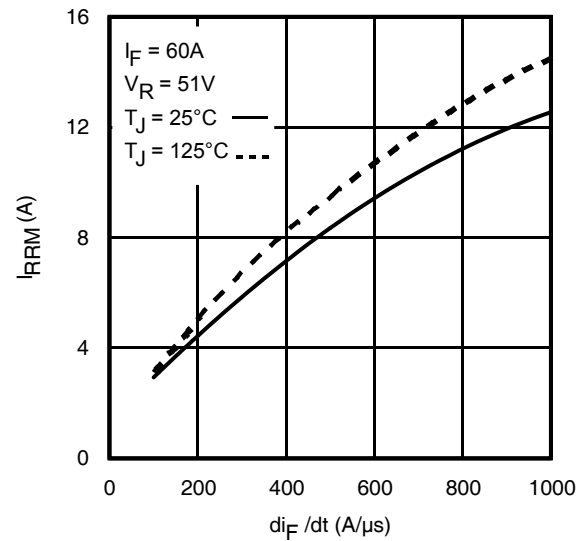
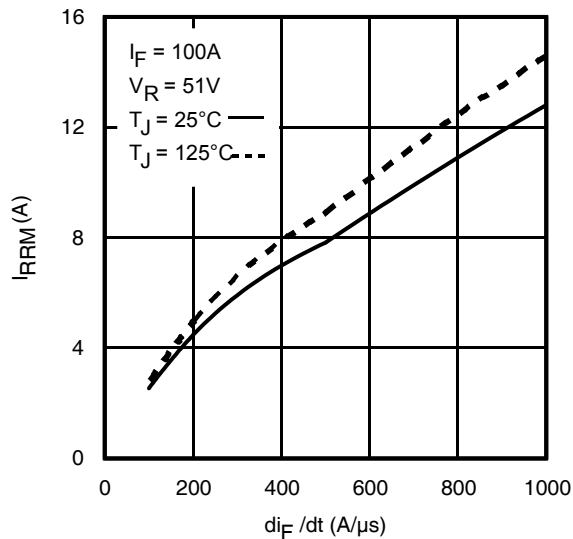
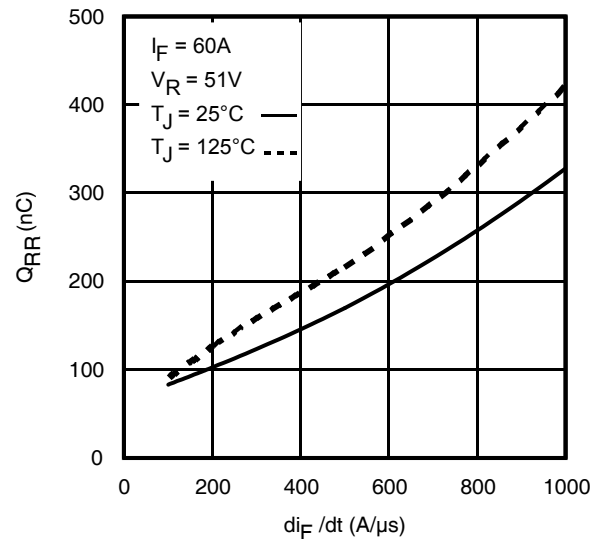
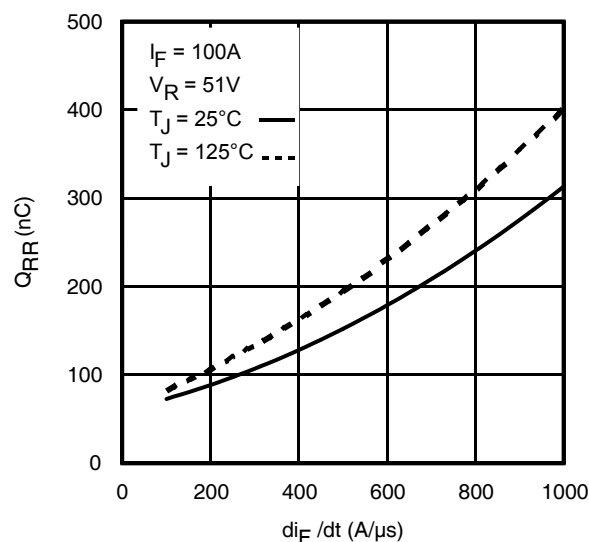
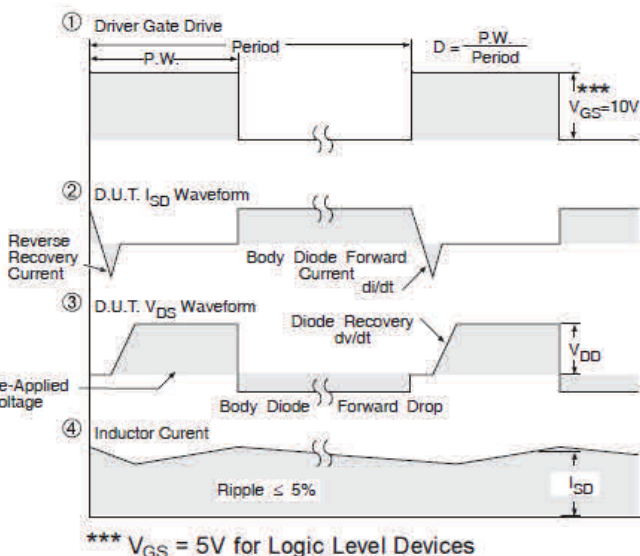
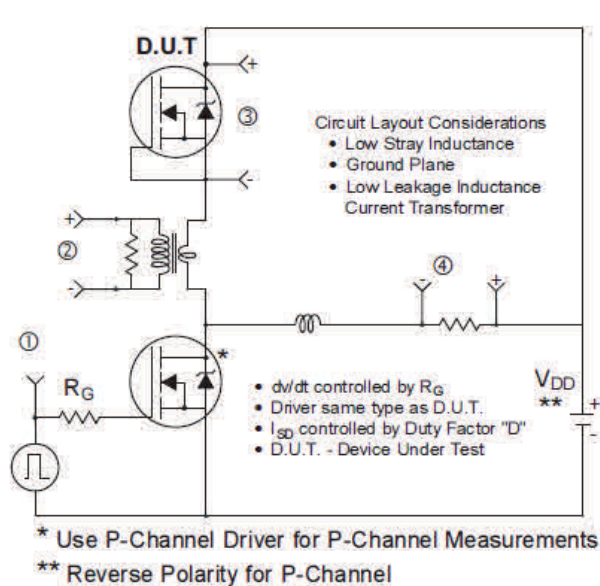


Fig 16. Maximum Avalanche Energy vs. Temperature

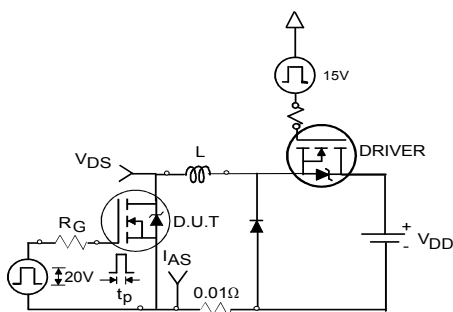
#### Notes on Repetitive Avalanche Curves , Figures 14, 15: (For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)  
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$

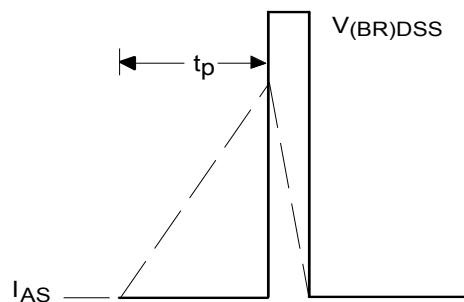

**Fig 17.** Threshold Voltage vs. Temperature

**Fig 18.** Typical Recovery Current vs. dif/dt

**Fig 19.** Typical Recovery Current vs. dif/dt

**Fig 20.** Typical Stored Charge vs. dif/dt

**Fig 21.** Typical Stored Charge vs. dif/dt



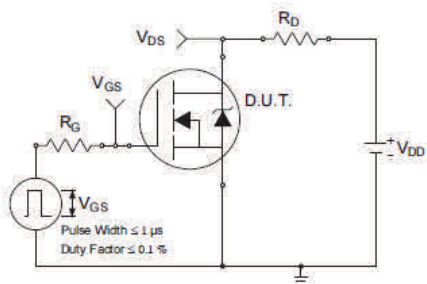
**Fig 22. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



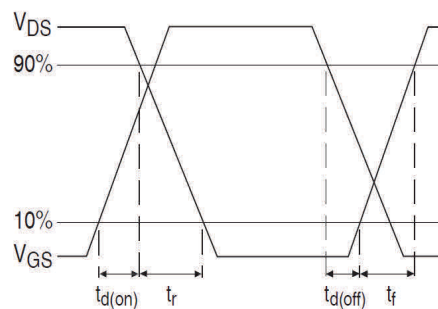
**Fig 23a. Unclamped Inductive Test Circuit**



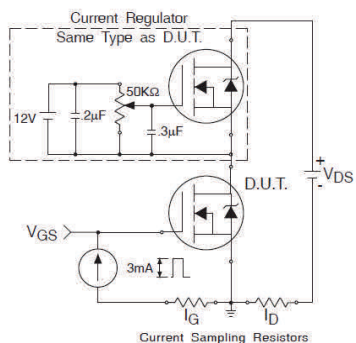
**Fig 23b. Unclamped Inductive Waveforms**



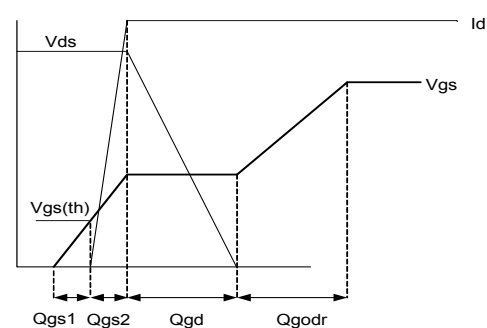
**Fig 24a. Switching Time Test Circuit**



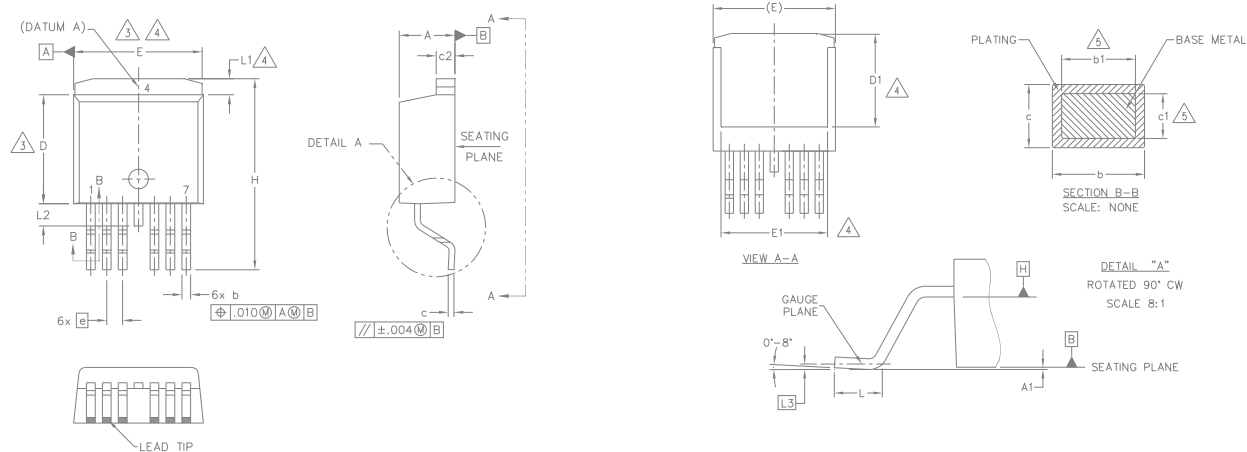
**Fig 24b. Switching Time Waveforms**



**Fig 25a. Gate Charge Test Circuit**



**Fig 25b. Gate Charge Waveform**

**D<sup>2</sup>Pak-7Pin Package Outline** (Dimensions are shown in millimeters (inches))


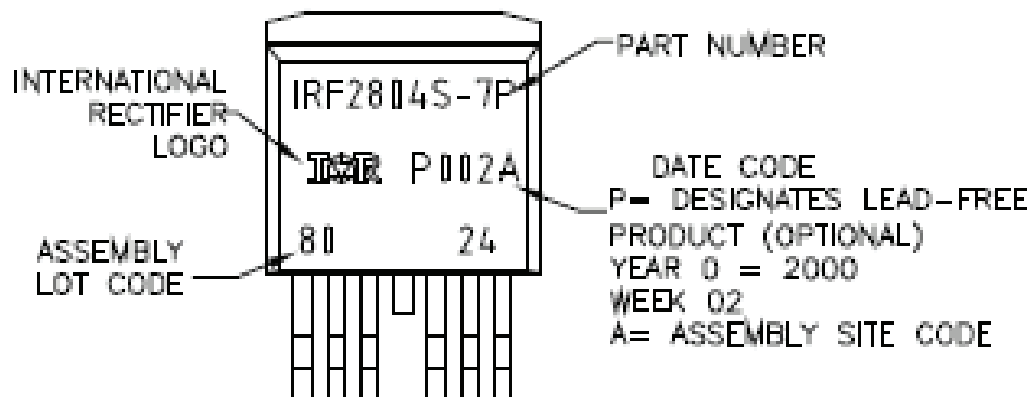
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	—	0.254	—	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	3,4
D	8.38	9.65	.330	.380	
D1	6.86	7.42	.270	.292	
E	9.65	10.54	.380	.415	
E1	6.22	8.48	.245	.334	
e	1.27 BSC		.050 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

**NOTES:**

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB. EXCEPT FOR DIMS. E, E1 & D1.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## D<sup>2</sup>Pak-7Pin Part Marking Information

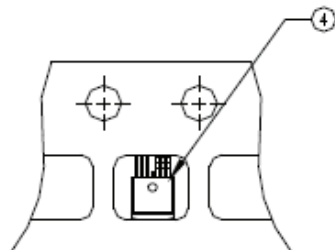


## D2Pak-7Pin Tape and Reel

### NOTES, TAPE & REEL, LABELLING:

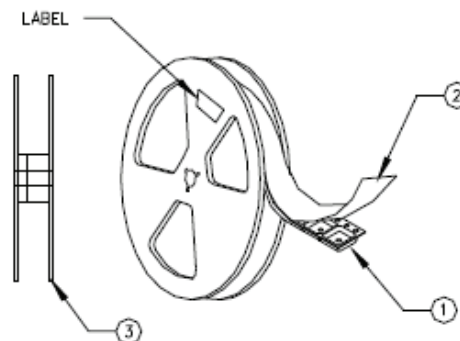
#### 1. TAPE AND REEL

- 1.1 REEL SIZE 13 INCH DIAMETER.
- 1.2 EACH REEL CONTAINING 800 DEVICES.
- 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
- 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
- 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
- 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.



#### 2. LABELLING (REEL AND SHIPPING BAG).

- 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
- 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
- 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
- 2.4 QUANTITY:
- 2.5 VENDOR CODE: IR
- 2.6 LOT CODE:
- 2.7 DATE CODE:



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) <sup>††</sup>	
<b>Moisture Sensitivity Level</b>	D <sup>2</sup> Pak-7Pin	MSL1 (per JEDEC J-STD-020D <sup>††</sup> )
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comment
03/05/2015	<ul style="list-style-type: none"> <li>Updated E<sub>AS</sub> (L = 1mH) = 1029mJ on page 2</li> <li>Updated note 9 "Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 1mH, R<sub>G</sub> = 50Ω, I<sub>AS</sub> = 45A, V<sub>GS</sub> = 10V" on page 2</li> <li>Updated package outline on page 9 .</li> </ul>

International  
 Rectifier

**IR WORLD HEADQUARTERS:** 101 N. Sepulveda Blvd., El Segundo, California 90245, USA

To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>

## IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenhheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office ([www.infineon.com](http://www.infineon.com)).

## WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.