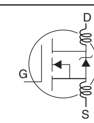
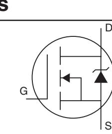
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.057	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	0.011	0.013	Ω	V_{GS} = 10V, I_D = 30A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = 10V, I_D = 250μA
g_{fs}	Forward Transconductance	41	——	——	S	V_{DS} = 25V, I_D = 30A
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 55V, V_{GS} = 0V
		——	——	250		V_{DS} = 55V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V
Q_g	Total Gate Charge	——	62	93	nC	I_D = 30A
Q_{gs}	Gate-to-Source Charge	——	17	26		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	22	33		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	——	13	——	ns	V_{DD} = 28V
t_r	Rise Time	——	74	——		I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time	——	43	——		R_G = 6.8Ω
t_f	Fall Time	——	54	——		V_{GS} = 10V ④
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance	——	7.5	——		from package and center of die contact 
C_{iss}	Input Capacitance	——	2030	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	470	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	91	——		ƒ = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	2600	——		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	——	330	——		V_{GS} = 0V, V_{DS} = 44V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	——	630	——		V_{GS} = 0V, V_{DS} = 0V to 44V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	71	A	MOSFET symbol showing the
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	280		integral reverse p-n junction diode. 
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 30A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	70	105	ns	T_J = 25°C, I_F = 30A, V_{DD} = 28V
Q_{rr}	Reverse RecoveryCharge	——	180	270	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes ① through ⑧ are on page 11

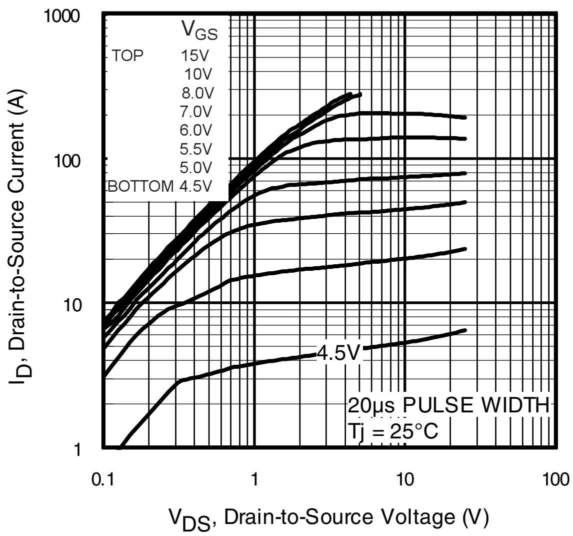


Fig 1. Typical Output Characteristics

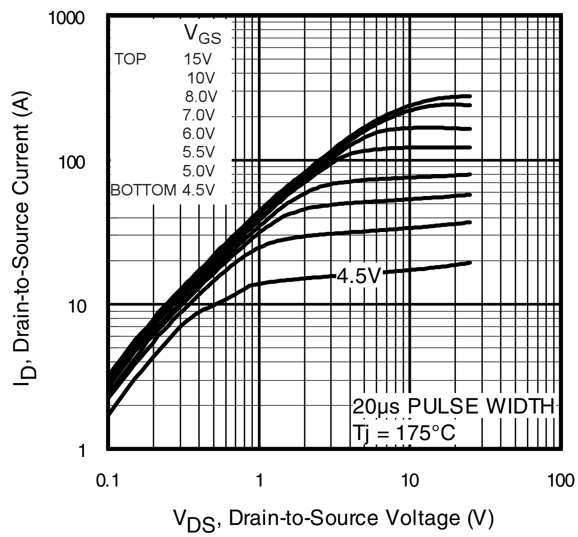


Fig 2. Typical Output Characteristics

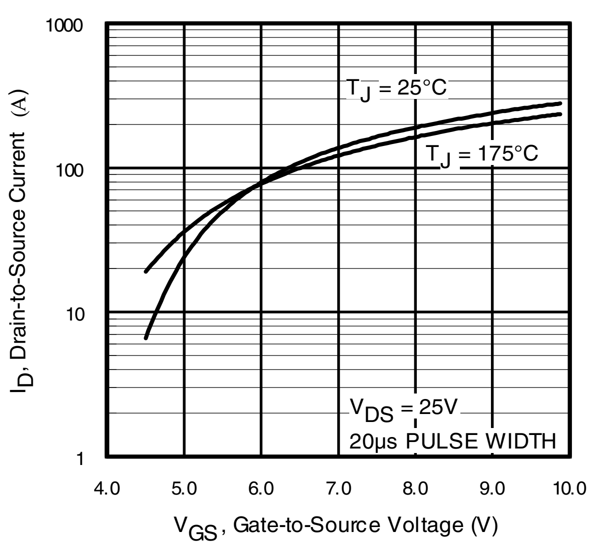


Fig 3. Typical Transfer Characteristics

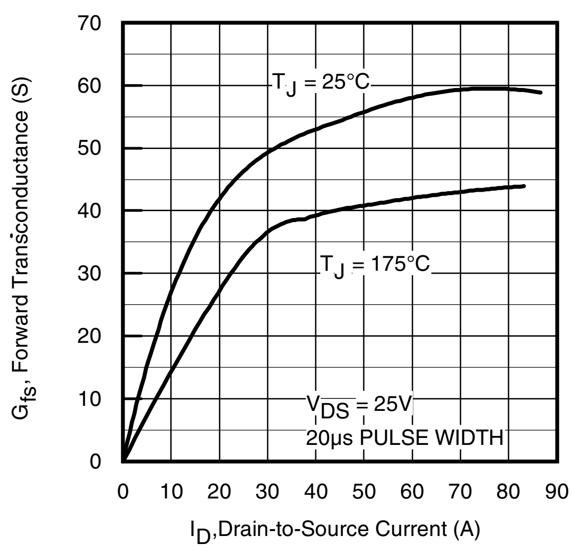


Fig 4. Typical Forward Transconductance Vs. Drain Current

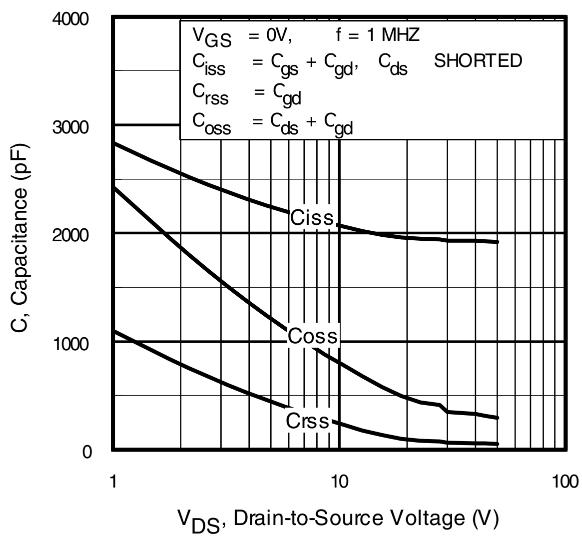


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

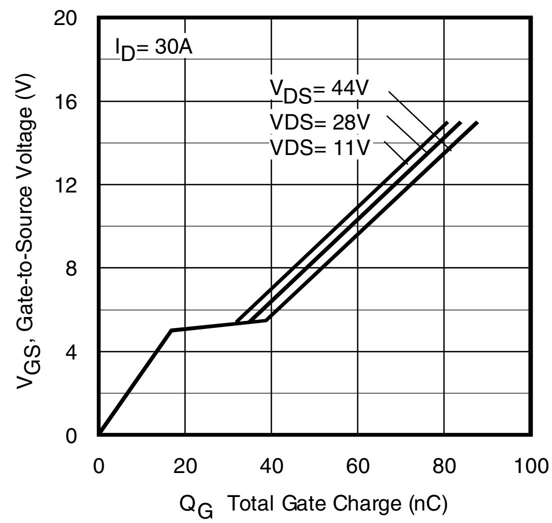


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

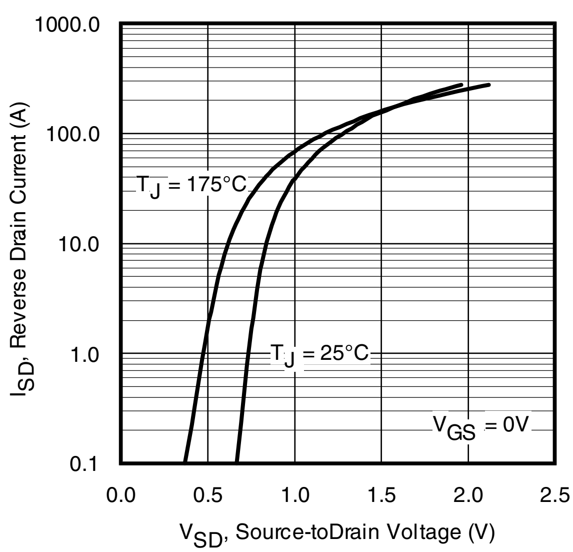


Fig 7. Typical Source-Drain Diode Forward Voltage

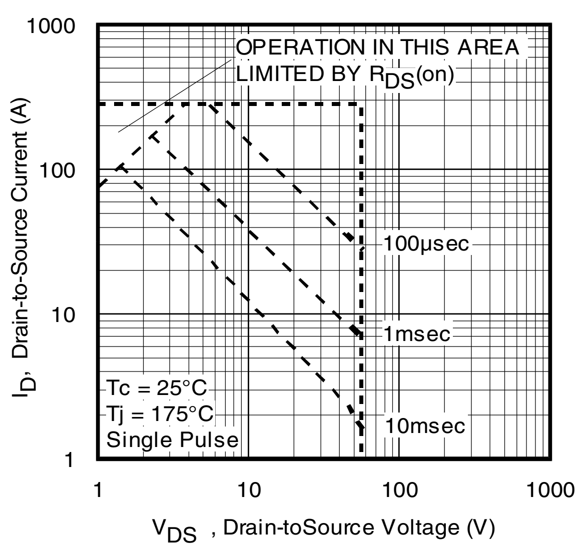


Fig 8. Maximum Safe Operating Area

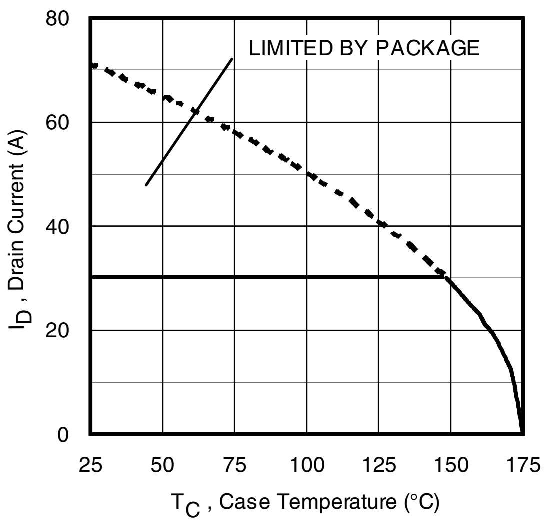


Fig 9. Maximum Drain Current Vs. Case Temperature

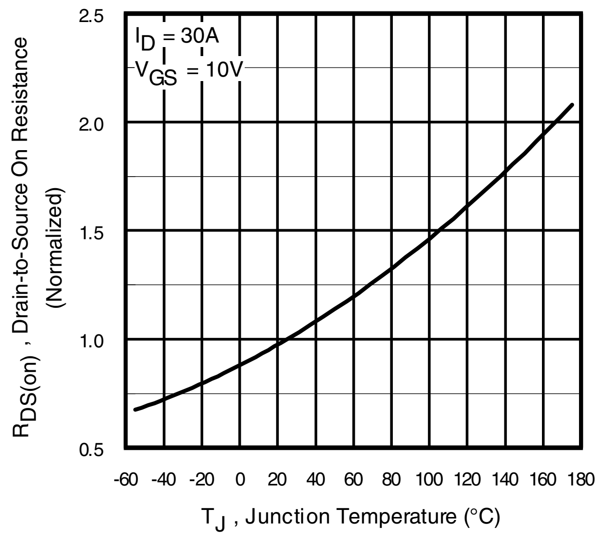


Fig 10. Normalized On-Resistance Vs. Temperature

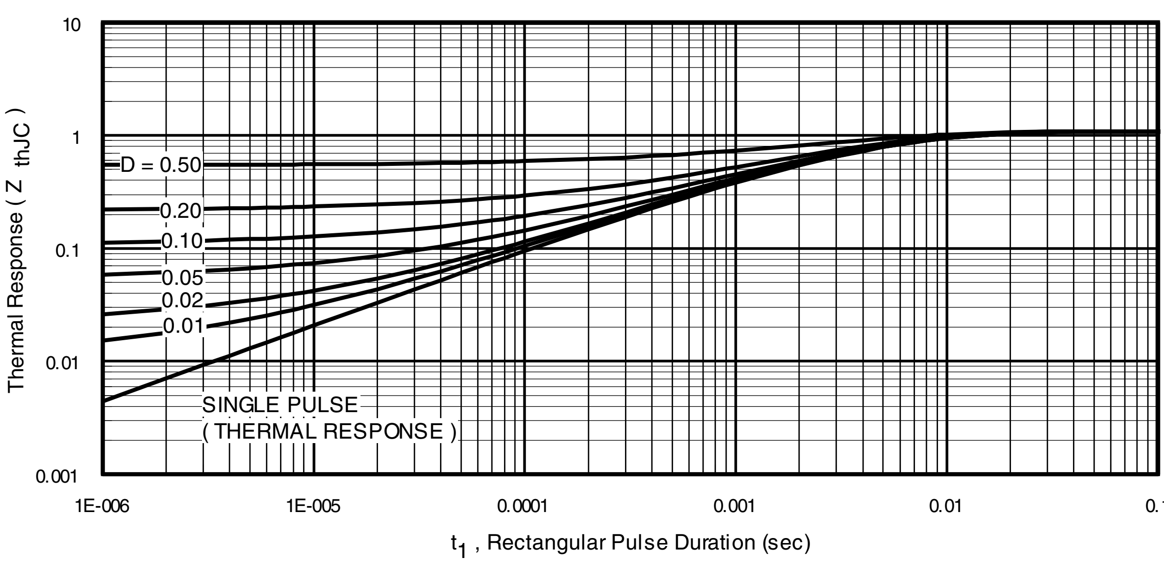


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

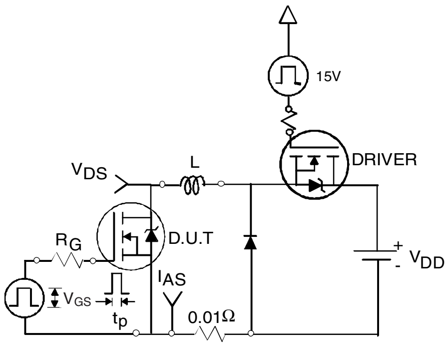


Fig 12a. Unclamped Inductive Test Circuit

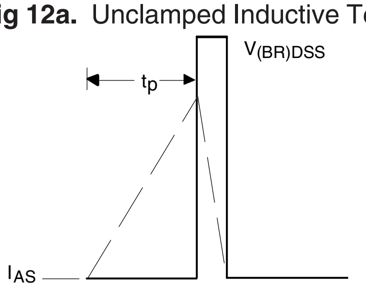


Fig 12b. Unclamped Inductive Waveforms

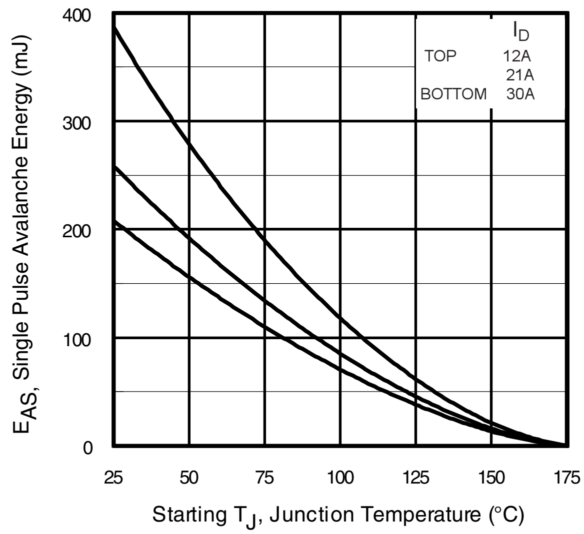


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

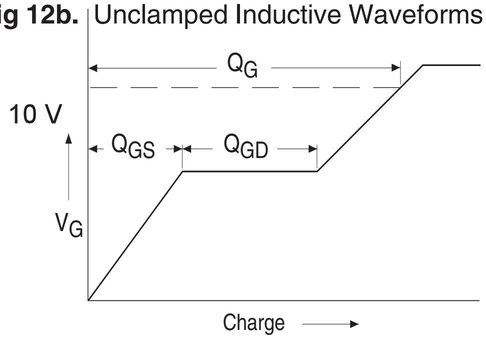


Fig 13a. Basic Gate Charge Waveform

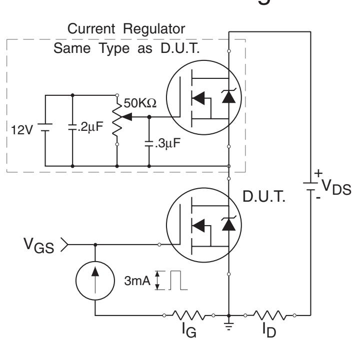


Fig 13b. Gate Charge Test Circuit

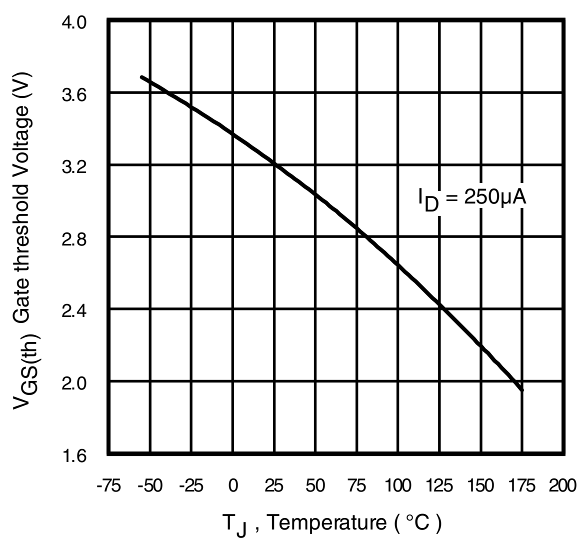


Fig 14. Threshold Voltage Vs. Temperature

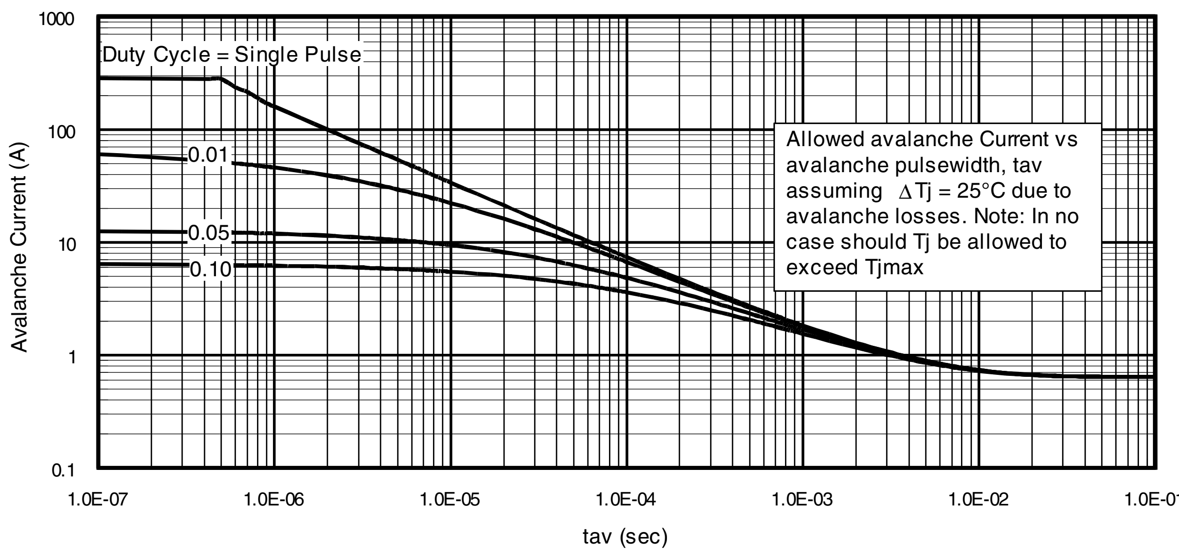


Fig 15. Typical Avalanche Current Vs.Pulsewidth

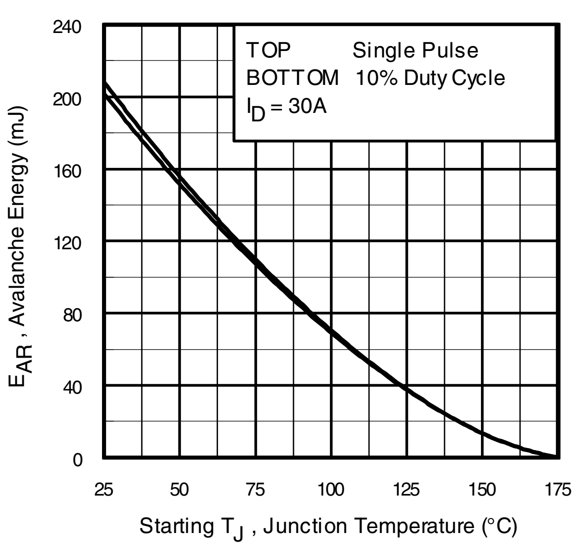
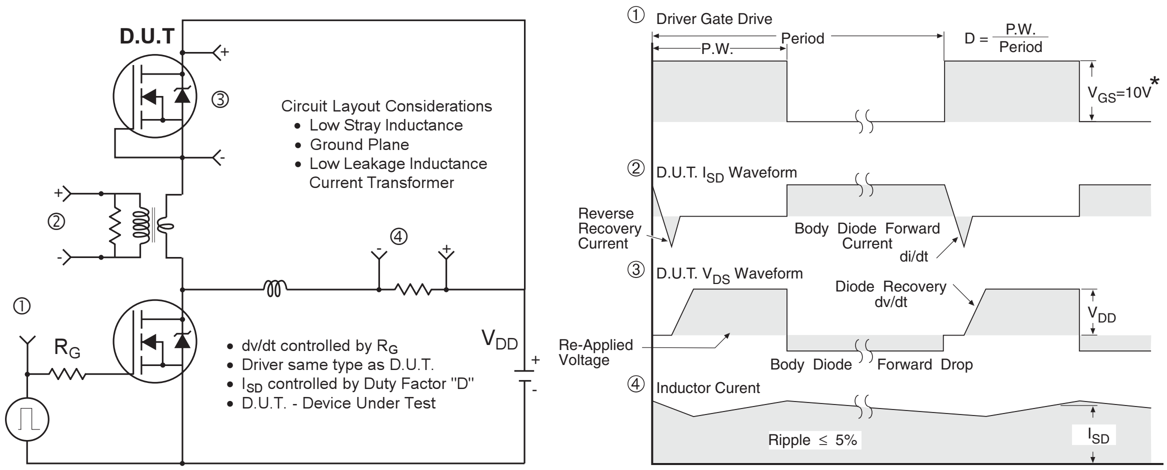


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$



* V_{GS} = 5V for Logic Level Devices

Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

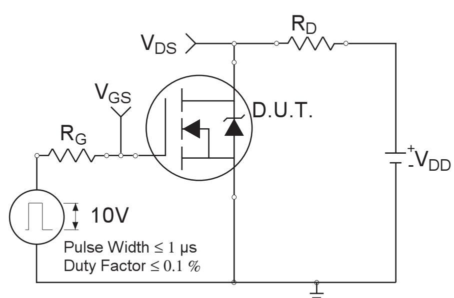


Fig 18a. Switching Time Test Circuit

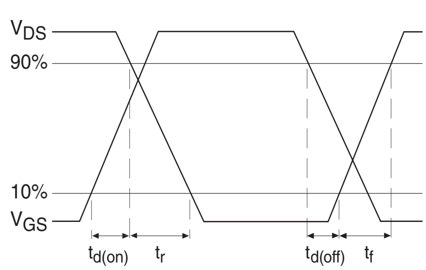
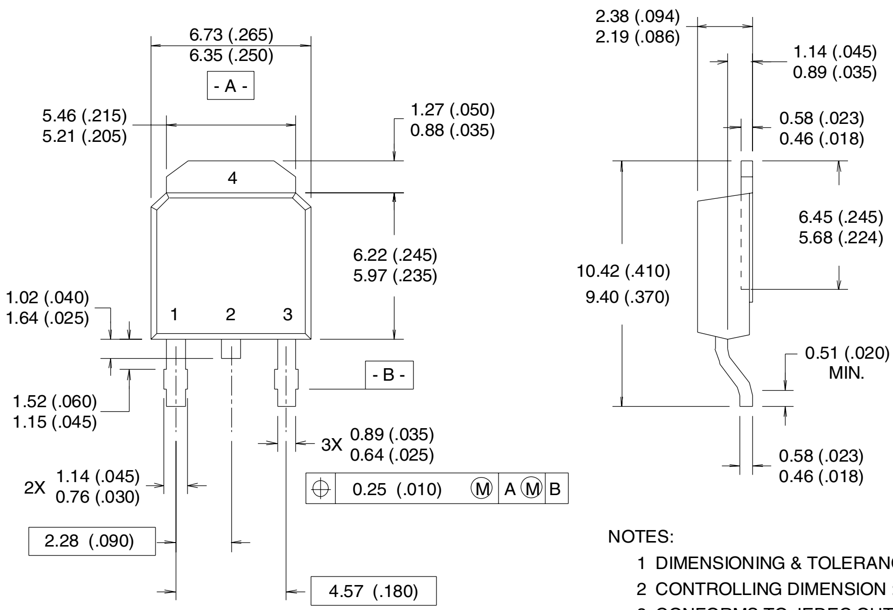


Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)

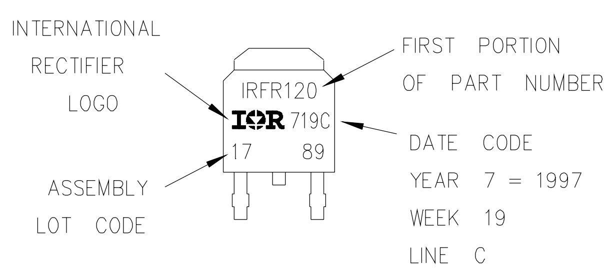


LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

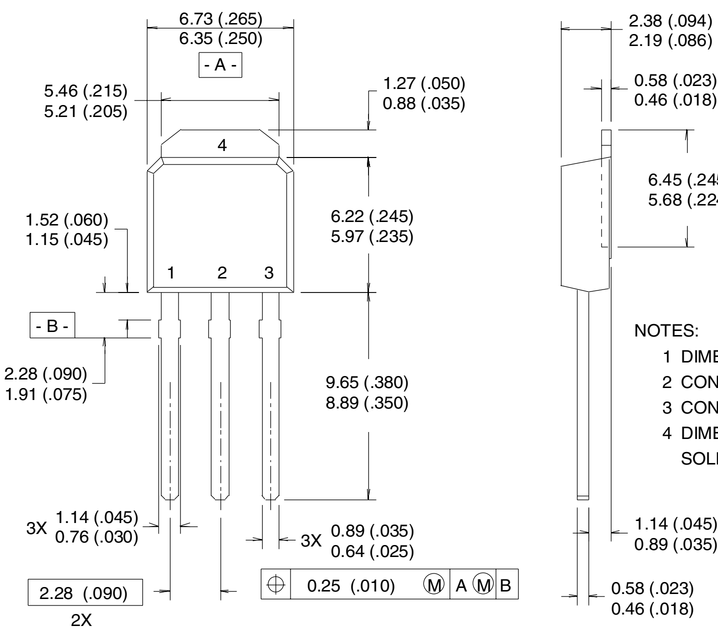
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

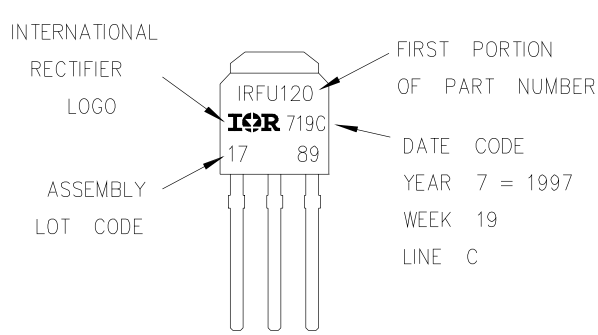


LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

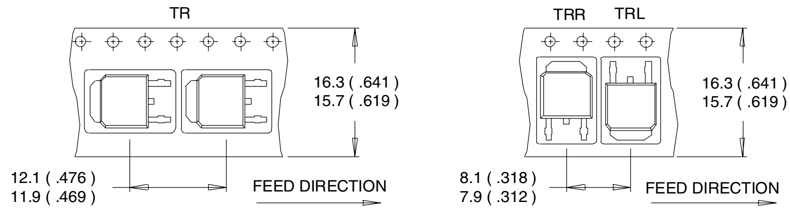
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

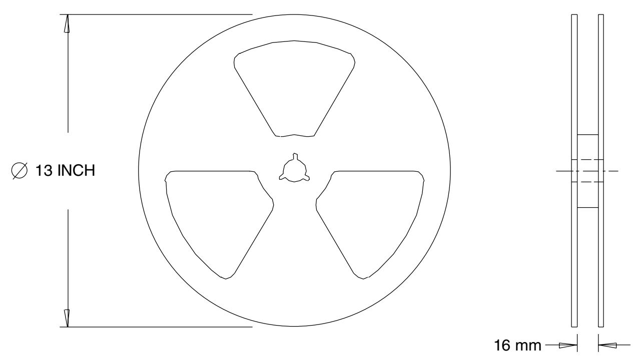


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by T_{Jmax}, starting $T_J = 25°C$, L = 0.47mH $R_G = 25\Omega$, $I_{AS} = 30A$, $V_{GS} = 10V$. Part not recommended for use above this value.

③ $I_{SD} \leq 30A$, di/dt $\leq$ 300A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$

④ Pulse width $\leq$ 1.0ms; duty cycle $\leq$ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑦ This value determined from sample failure population. 100% tested to this value in production.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material) . For recommended footprint and soldering techniques refer to application note #AN-994

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101]market.
Qualification Standards can be found on IR's Web site.

International
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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/