

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High side floating supply voltage	-0.3	625	V	
V <sub>S</sub>	High side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3		
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3		
V <sub>LO</sub>	Low side output voltage	-0.3	V <sub>CC</sub> + 0.3		
V <sub>RT</sub>	R <sub>T</sub> voltage	-0.3	V <sub>CC</sub> + 0.3		
V <sub>CT</sub>	C <sub>T</sub> voltage	-0.3	V <sub>CC</sub> + 0.3		
I <sub>CC</sub>	Supply current (note 1)	—	25	mA	
I <sub>RT</sub>	R <sub>T</sub> output current	-5	5		
dV <sub>S</sub> /dt	Allowable offset supply voltage transient	—	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	(8 lead DIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
R <sub>θJA</sub>	Thermal resistance, junction to ambient	(8 lead DIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-55	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_B$	High side sloating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
$V_S$	High side floating supply offset voltage	—	600	
$V_{HO}$	High side floating output voltage	$V_S$	$V_B$	
$V_{LO}$	Low side output voltage	0	$V_{CC}$	
$I_{CC}$	Supply current (note 1)	—	5	mA
$T_A$	Ambient temperature	-40	125	$^\circ\text{C}$

Note 1: Because of the IR2151's application specificity toward off-line supply systems, this IC contains a zener clamp structure between the chip  $V_{CC}$  and COM which has a nominal breakdown voltage of 15.6V. Therefore, the IC supply voltage is normally derived by forcing current into the supply lead (typically by means of a high value resistor connected between the chip  $V_{CC}$  and the rectified line voltage and a local decoupling capacitor from  $V_{CC}$  to COM) and allowing the internal zener clamp circuit to determine the nominal supply voltage. Therefore, this circuit should not be driven by a DC, low impedance power source of greater than  $V_{CLAMP}$ .

## Dynamic Electrical Characteristics

 $V_{BIAS} (V_{CC}, V_{BS}) = 12V$ ,  $C_L = 1000 \text{ pF}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_r$	Turn-on rise time	—	80	120	ns	
$t_f$	Turn-off fall time	—	40	70		
DT	Deadtime	0.50	1.20	2.25	$\mu\text{s}$	
D	$R_T$ duty cycle	48	50	52	%	

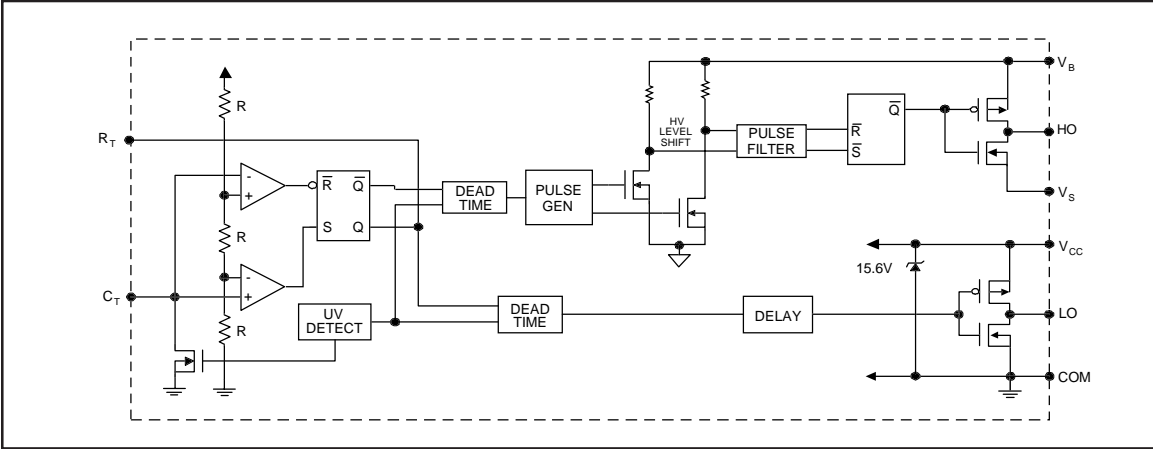
## Static Electrical Characteristics

 $V_{BIAS} (V_{CC}, V_{BS}) = 12V$ ,  $C_L = 1000 \text{ pF}$ ,  $C_T = 1 \text{ nF}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$f_{OSC}$	Oscillator frequency	19.4	20.0	20.6	kHz	$R_T = 35.7 \text{ k}\Omega$
		94	100	106		$R_T = 7.04 \text{ k}\Omega$
$V_{CLAMP}$	$V_{CC}$ zener shunt clamp voltage	14.4	15.6	16.8	V	$I_{CC} = 5 \text{ mA}$
$V_{CT+}$	2/3 $V_{CC}$ threshold	7.8	8.0	8.2		
$V_{CT-}$	1/3 $V_{CC}$ threshold	3.8	4.0	4.2		
$V_{CTUV}$	$C_T$ undervoltage lockout	—	20	50	mV	$2.5V < V_{CC} < V_{CCUV+}$
$V_{RT+}$	$R_T$ high level output voltage, $V_{CC} - R_T$	—	0	100		$I_{RT} = -100 \mu\text{A}$
		—	200	300		$I_{RT} = -1 \text{ mA}$
$V_{RT-}$	$R_T$ Low Level Output Voltage	—	20	50		$I_{RT} = 100 \mu\text{A}$
		—	200	300		$I_{RT} = 1 \text{ mA}$
$V_{RTUV}$	$R_T$ Undervoltage Lockout, $V_{CC} - R_T$	—	0	100		$2.5V < V_{CC} < V_{CCUV+}$
$V_{OH}$	High Level Output Voltage, $V_{BIAS} - V_O$	—	—	100		$I_O = 0 \text{ A}$
$V_{OL}$	Low Level Output Voltage, $V_O$	—	—	100		$I_O = 0 \text{ A}$
$I_{LK}$	Offset Supply Leakage Current	—	—	50	$\mu\text{A}$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	—	10	50		
$I_{QCC}$	Quiescent $V_{CC}$ Supply Current	—	400	950		
$I_{CT}$	$C_T$ Input Current	—	0.001	1.0		
$V_{CCUV+}$	$V_{CC}$ Supply Undervoltage Positive Going Threshold	7.7	8.4	9.2	V	
$V_{CCUV-}$	$V_{CC}$ Supply Undervoltage Negative Going Threshold	7.4	8.1	8.9		
$V_{CCUVH}$	$V_{CC}$ Supply Undervoltage Lockout Hysteresis	200	500	—	mV	
$I_{O+}$	Output High Short Circuit Pulsed Current	100	125	—	mA	$V_O = 0V$
$I_{O-}$	Output Low Short Circuit Pulsed Current	210	250	—		$V_O = 15V$

# IR2151

## Functional Block Diagram

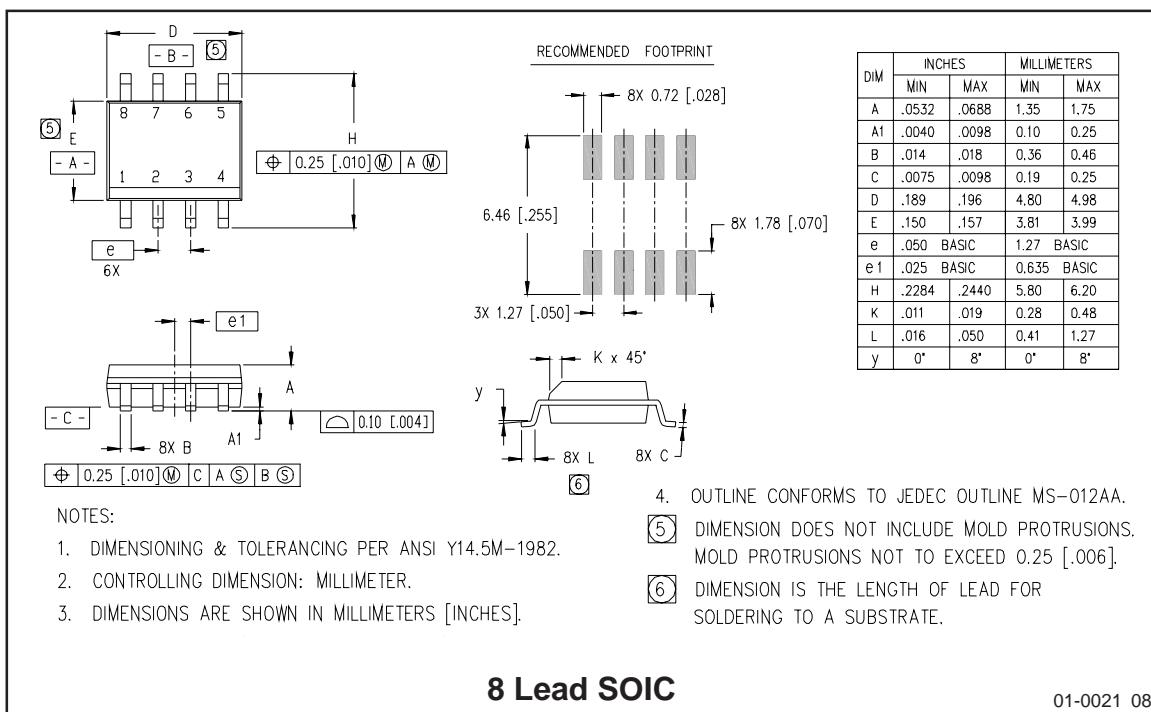
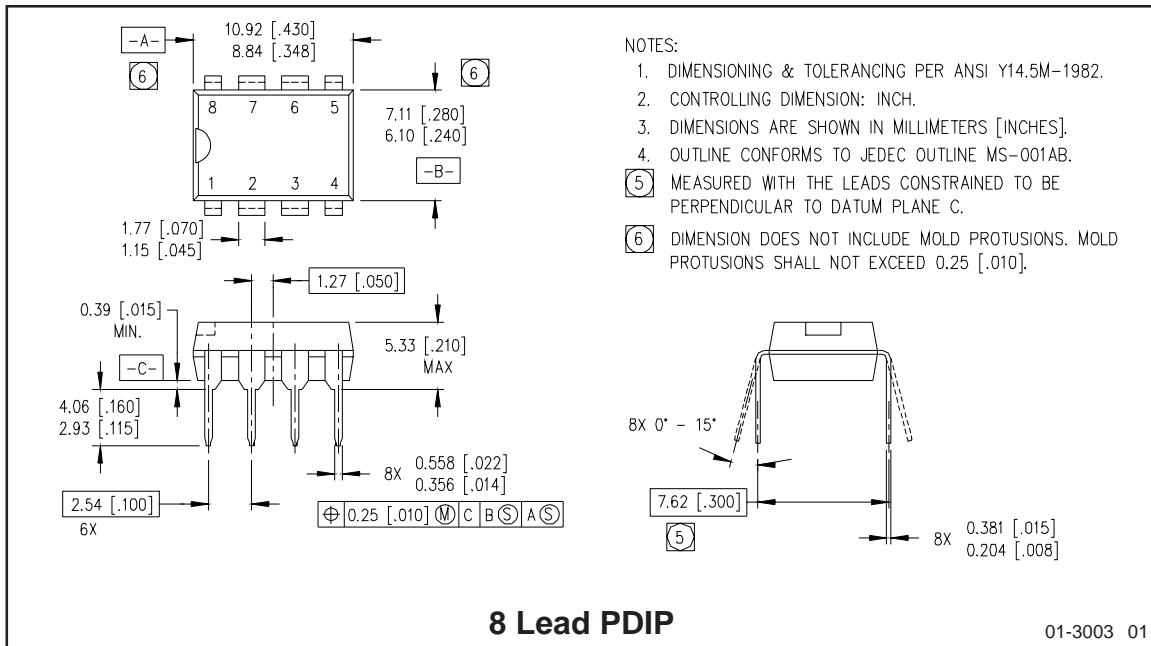


## Lead Definitions

Symbol	Description
R <sub>T</sub>	Oscillator timing resistor input,in phase with LO for normal IC operation
C <sub>T</sub>	Oscillator timing capacitor input, the oscillator frequency according to the following equation: $f = \frac{1}{1.4 \times (R_T + 75\Omega) \times C_T}$ where 75Ω is the effective impedance of the R <sub>T</sub> output stage
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return
V <sub>CC</sub>	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

## Lead Assignments

<p>8 Lead DIP <b>IR2151</b></p>	<p>8 Lead SOIC <b>IR2151S</b></p>
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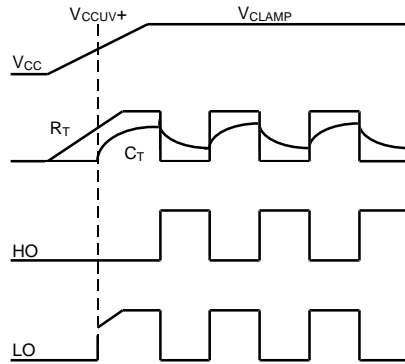


Figure 1. Input/Output Timing Diagram

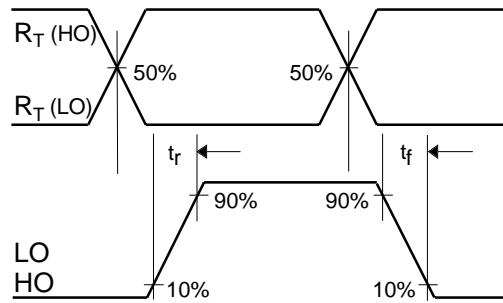


Figure 2. Switching Time Waveform Definitions

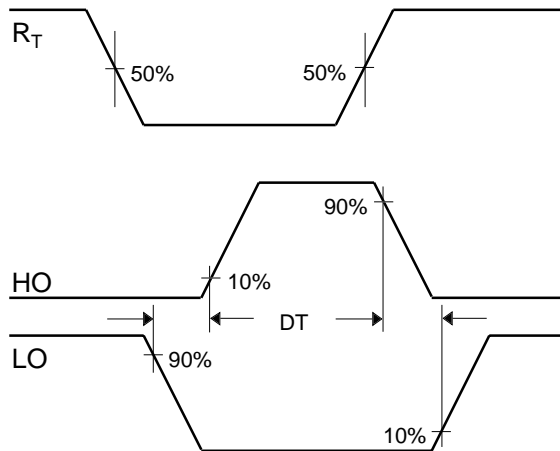


Figure 3. Deadtime Waveform Definitions