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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	8.5 5.0	A	$T_C = 20^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	20.5	A	$T_C = 25^\circ\text{C}$
Application (Flyback) relevant avalanche current, single pulse ³⁾	I_{AS}	-	-	3.2	A	measured with standard leakage inductance of transformer of $7\mu\text{H}$
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	V_{GS}	-16 -30	-	16 30	V	static; AC ($f > 1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	24.9	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	I_S	-	-	4.5	A	$T_C = 25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	20.5	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ⁴⁾	dv/dt	-	-	1	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$
Maximum diode commutation speed ⁴⁾	di/dt	-	-	50	A/ μs	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_S$, $T_j = 25^\circ\text{C}$
Insulation withstand voltage	V_{ISO}	-	-	2500	V	V_{rms} , $T_C = 25^\circ\text{C}$, $t = 1\text{ min}$

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction	R_{thJC}	-	-	5.0	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	$^\circ\text{C/W}$	lead
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	$^\circ\text{C/W}$	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	$^\circ\text{C}$	1.6 mm (0.063 in.) from case for 10s

¹⁾ DPAK / IPAK equivalent. Limited by $T_{j,max}$. $T_j = 20^\circ\text{C}$. Maximum duty cycle $D = 0.5$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Proven during verification test. For explanation please read AN - CoolMOS™ 700V P7.

⁴⁾ $V_{DClink} = 400\text{V}$; $V_{DS,peak} < V_{(BR)DSS}$; identical low side and high side switch with identical R_G

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	$V_{DS}=V_{GS}$, $I_D=0.09mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=700V$, $V_{GS}=0V$, $T_j=25^\circ C$ $V_{DS}=700V$, $V_{GS}=0V$, $T_j=150^\circ C$
Gate-source leakage current incl. Zener diode	I_{GSS}	-	-	1	μA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.49 1.03	0.60 -	Ω	$V_{GS}=10V$, $I_D=1.8A$, $T_j=25^\circ C$ $V_{GS}=10V$, $I_D=1.8A$, $T_j=150^\circ C$
Gate resistance	R_G	-	10	-	Ω	$f=1\text{ MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	364	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Output capacitance	C_{oss}	-	7	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	17	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	200	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=1.4A$, $R_G=5.3\Omega$
Rise time	t_r	-	5.5	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=1.4A$, $R_G=5.3\Omega$
Turn-off delay time	$t_{d(off)}$	-	63	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=1.4A$, $R_G=5.3\Omega$
Fall time	t_f	-	23	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=1.4A$, $R_G=5.3\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.6	-	nC	$V_{DD}=400V$, $I_D=1.4A$, $V_{GS}=0\text{ to }10V$
Gate to drain charge	Q_{gd}	-	3.7	-	nC	$V_{DD}=400V$, $I_D=1.4A$, $V_{GS}=0\text{ to }10V$
Gate charge total	Q_g	-	10.5	-	nC	$V_{DD}=400V$, $I_D=1.4A$, $V_{GS}=0\text{ to }10V$
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	$V_{DD}=400V$, $I_D=1.4A$, $V_{GS}=0\text{ to }10V$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=2.5A, T_J=25^{\circ}C$
Reverse recovery time	t_{rr}	-	190	-	ns	$V_R=400V, I_F=1.4A, di_F/dt=50A/\mu s$
Reverse recovery charge	Q_{rr}	-	0.8	-	μC	$V_R=400V, I_F=1.4A, di_F/dt=50A/\mu s$
Peak reverse recovery current	I_{rrm}	-	9	-	A	$V_R=400V, I_F=1.4A, di_F/dt=50A/\mu s$

4 Electrical characteristics diagrams

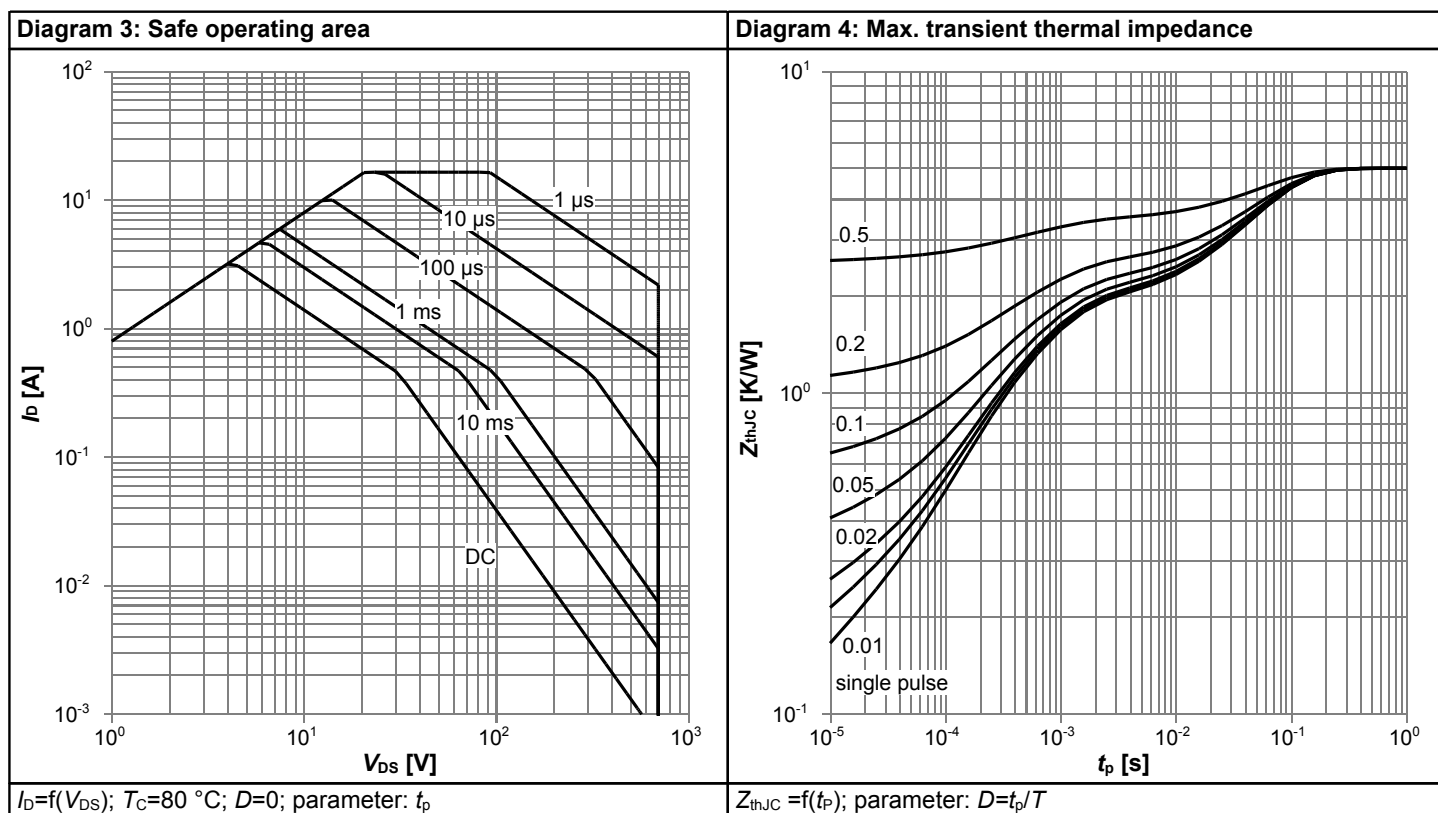
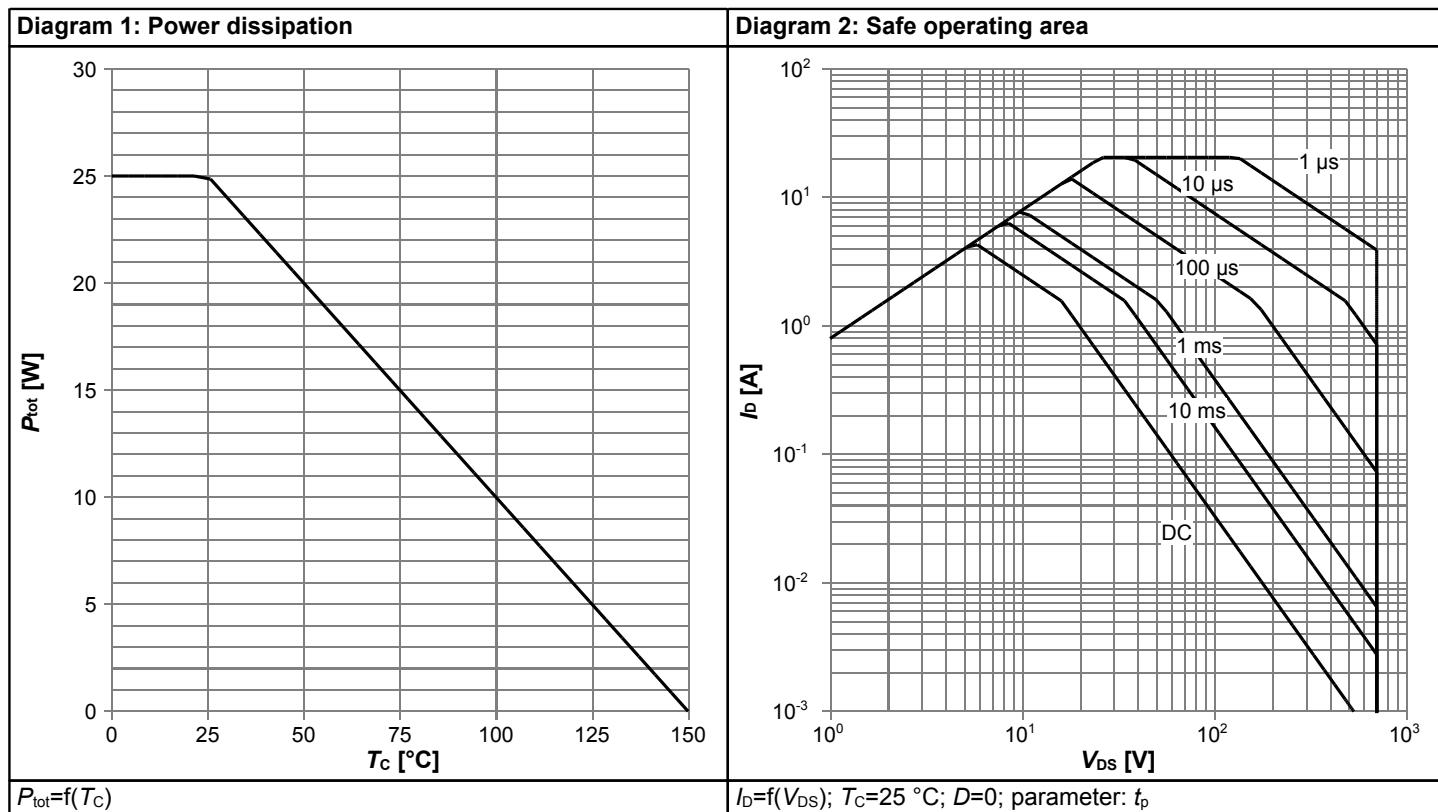
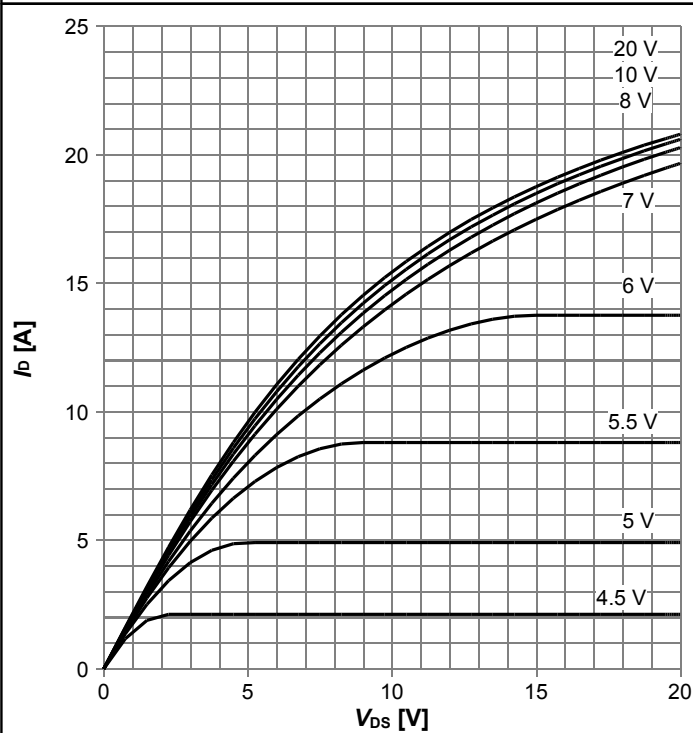
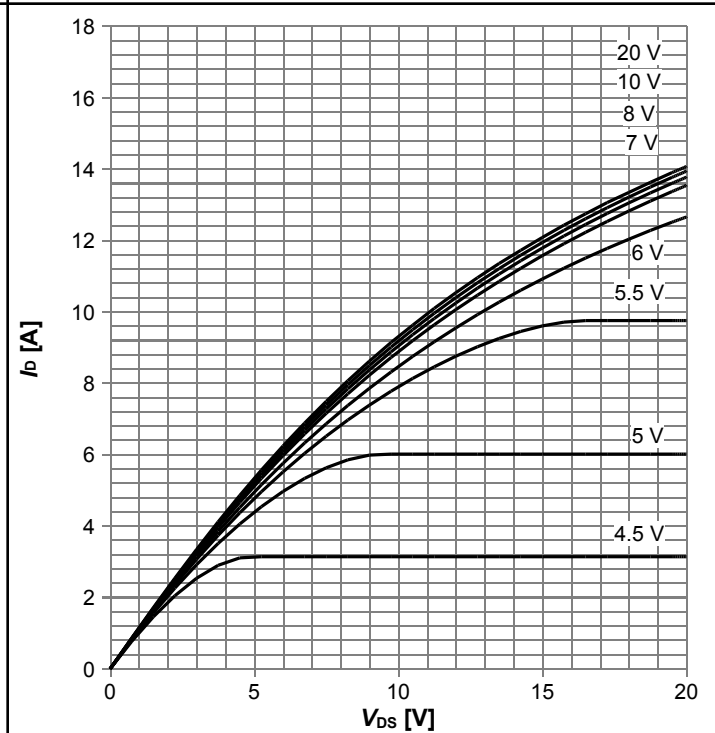


Diagram 5: Typ. output characteristics



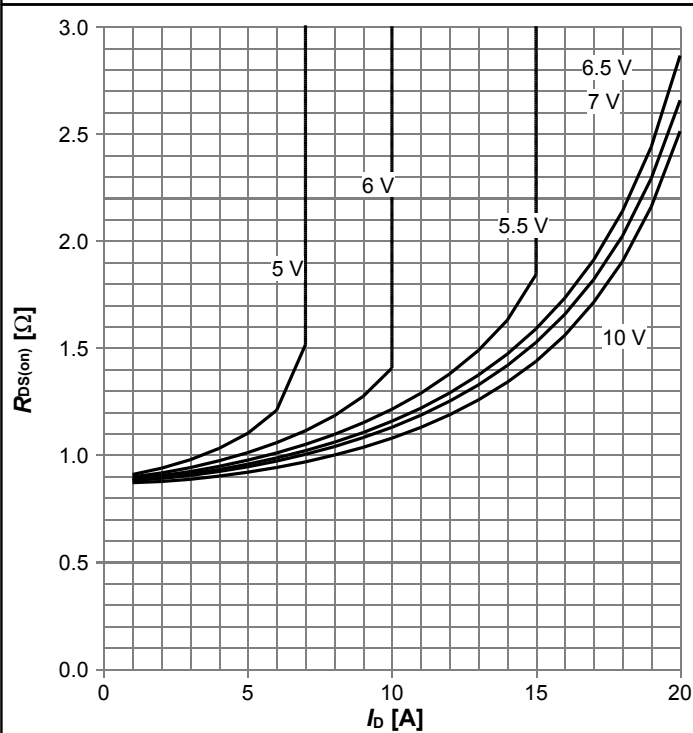
$I_D = f(V_{DS})$; $T_J = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



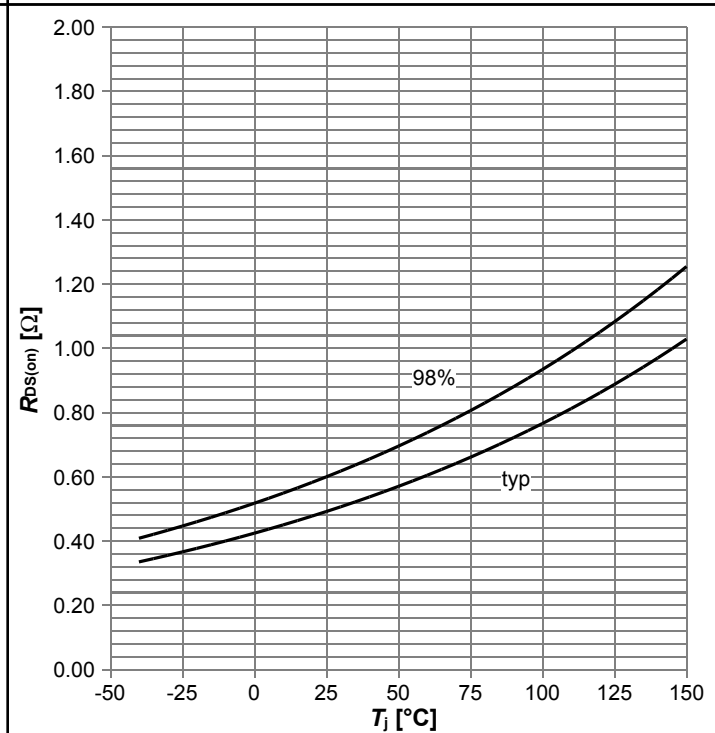
$I_D = f(V_{DS})$; $T_J = 125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



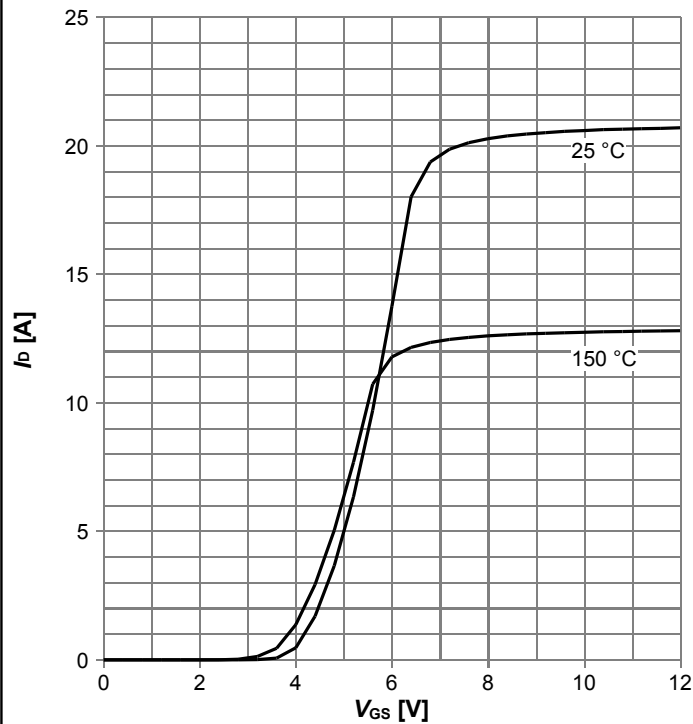
$R_{DS(on)} = f(I_D)$; $T_J = 125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



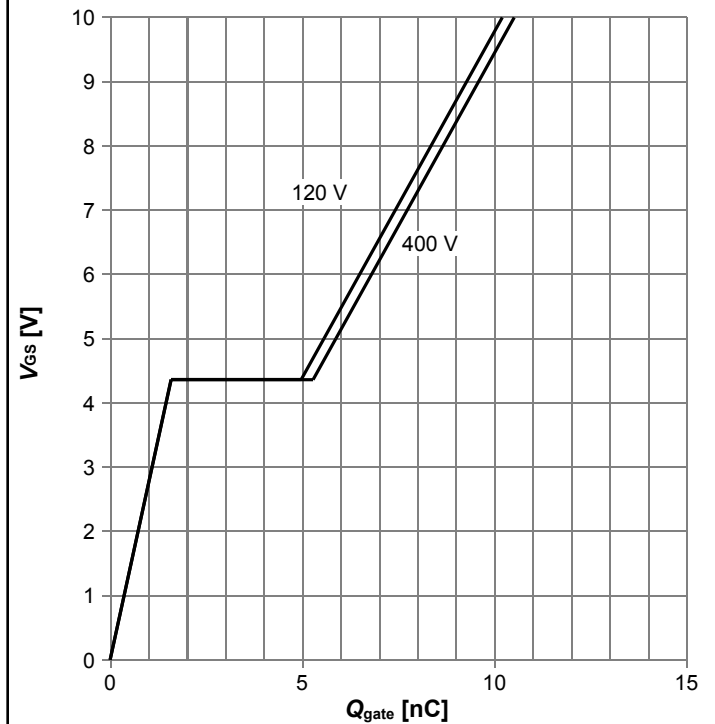
$R_{DS(on)} = f(T_J)$; $I_D = 1.8\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



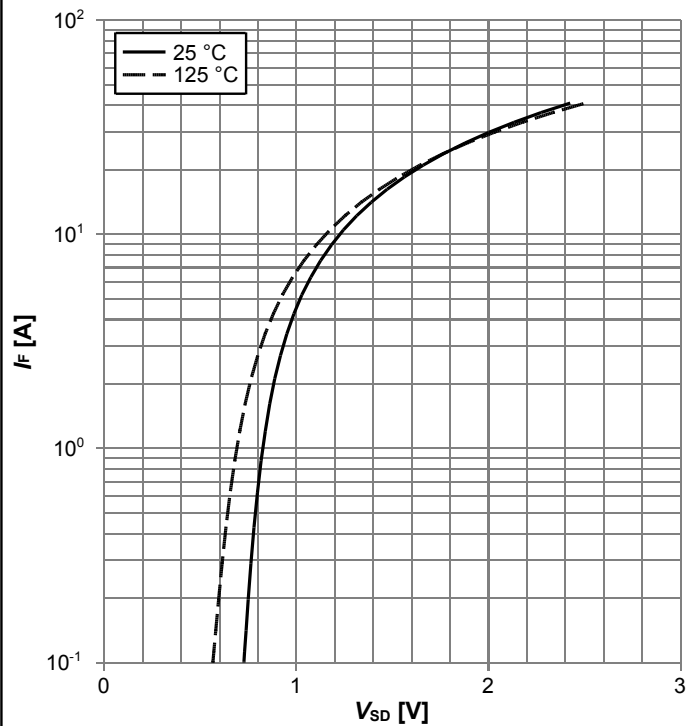
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



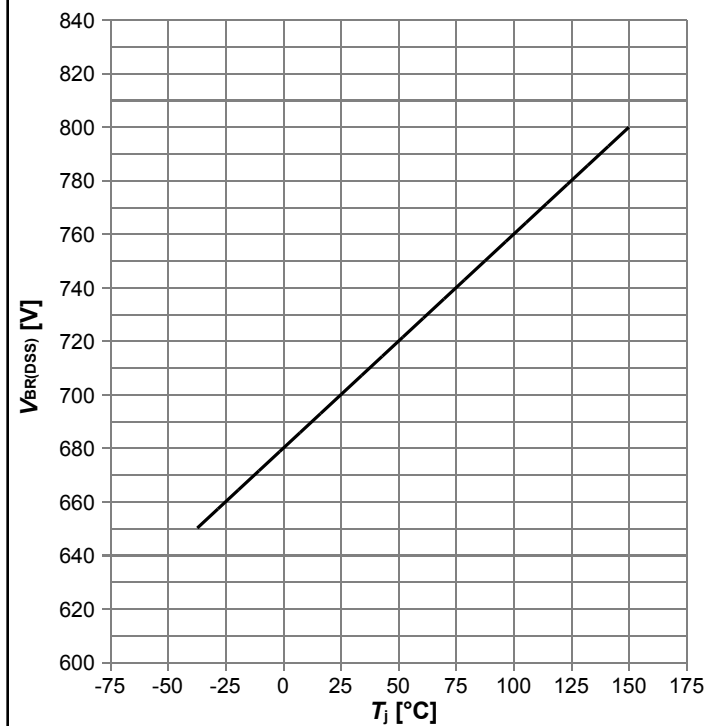
$V_{GS} = f(Q_{gate})$; $I_D = 1.4 A$ pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode

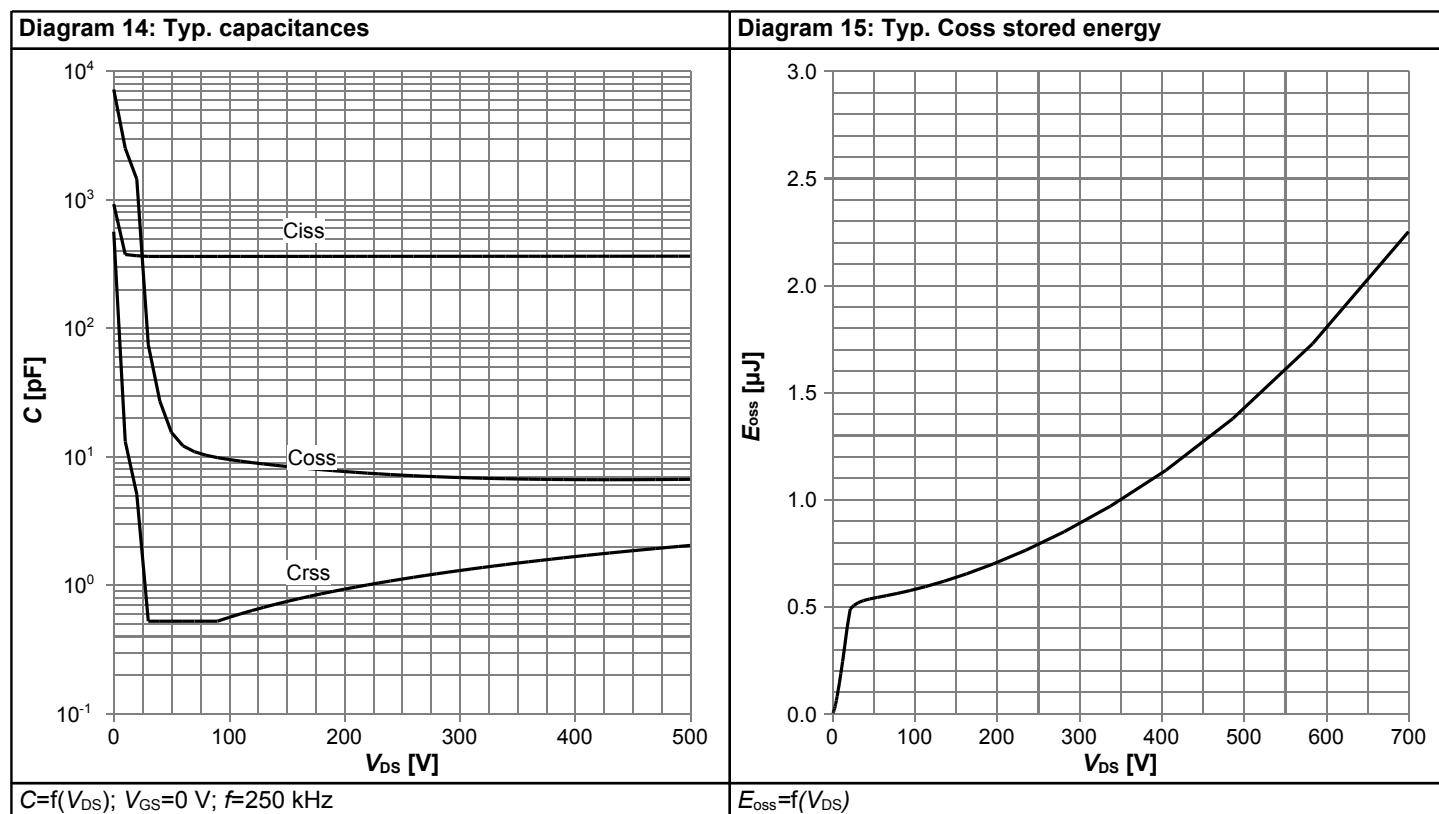


$I_F = f(V_{SD})$; parameter: T_j

Diagram 13: Drain-source breakdown voltage



$V_{BR(DSS)} = f(T_j)$; $I_D = 1 mA$



5 Test Circuits

Table 8 Diode characteristics

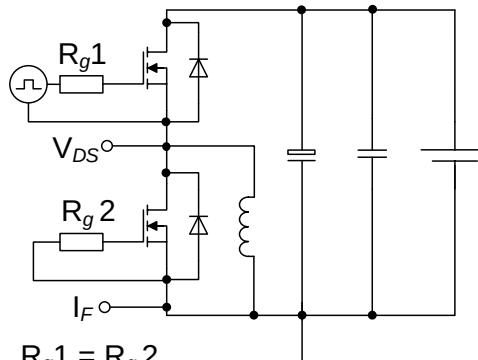
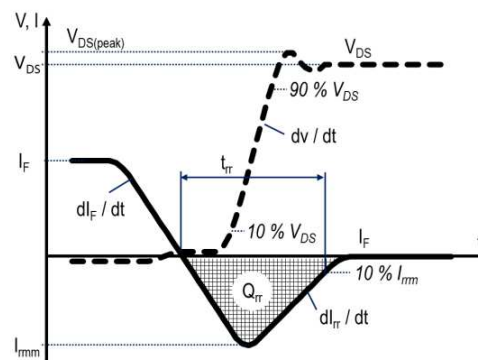
Test circuit for diode characteristics	Diode recovery waveform
 $R_{g1} = R_{g2}$	

Table 9 Switching times

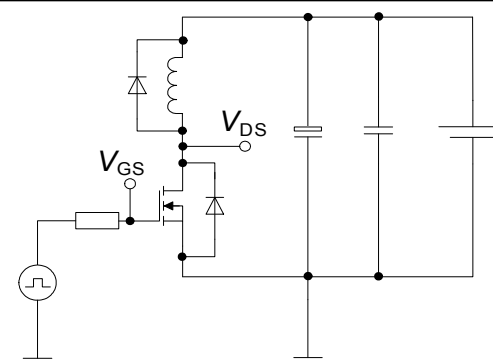
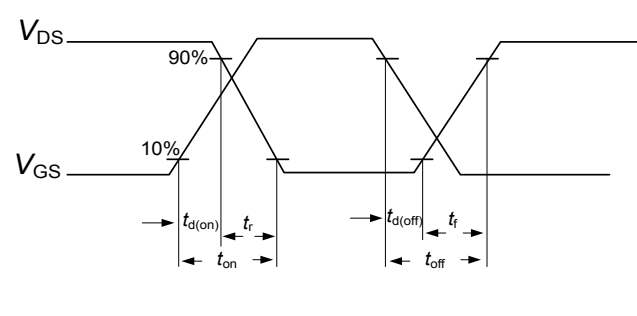
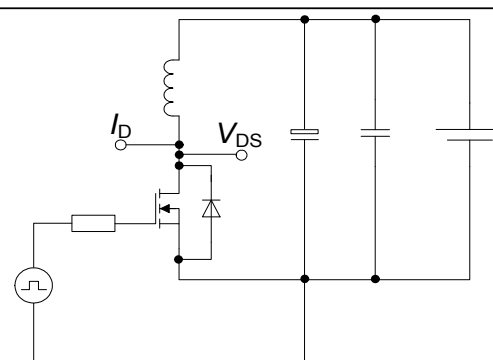
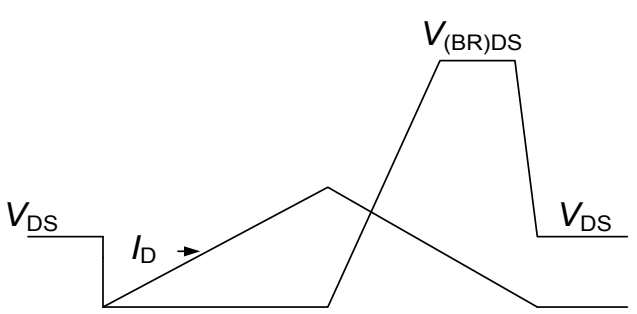
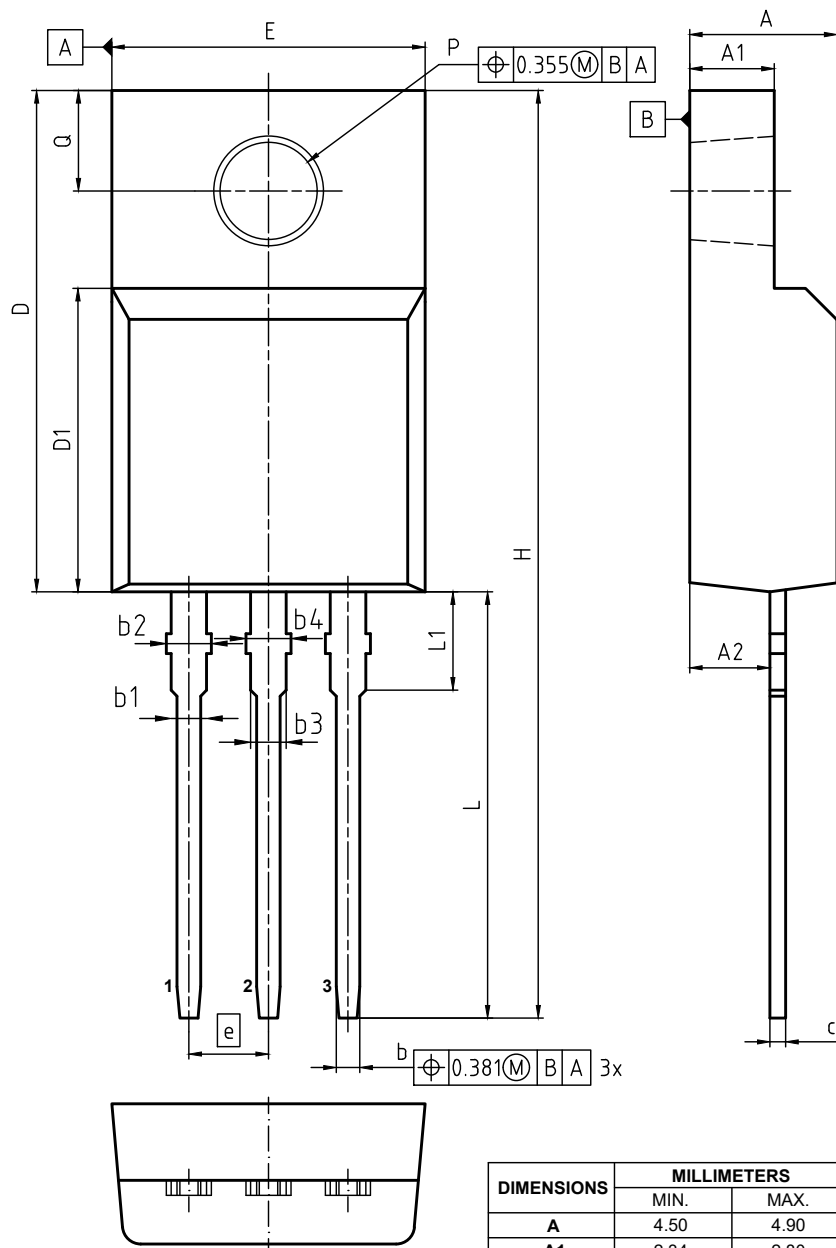
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



NOTES:
STANDARD QUALITY GRADE
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PRO-
TRUSIONS OR GATE BURRS

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.80
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	1.20	1.50
b3	0.65	1.38
b4	1.20	1.50
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
øP	3.00	3.38
Q	3.15	3.50

DOCUMENT NO. Z8B00181328
REVISION 03
ISSUE DATE 23.07.2018
SCALE 5:1 0 1 2 3 4 5mm
EUROPEAN PROJECTION

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS™ P7 Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPA70R600P7S

Revision: 2020-01-27, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-10-11	Release of final version
2.1	2018-02-12	Corrected front page text
2.2	2020-01-27	Updated package drawing, symbol ID and product validation

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