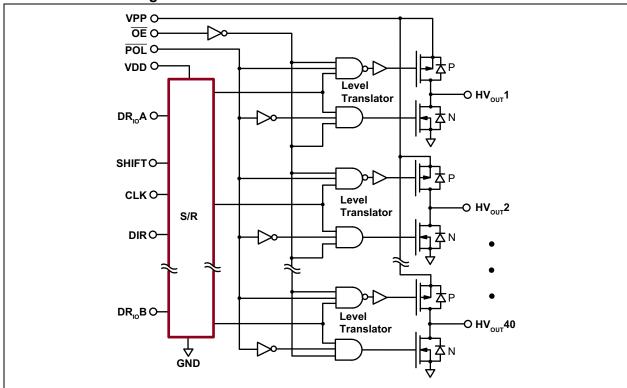
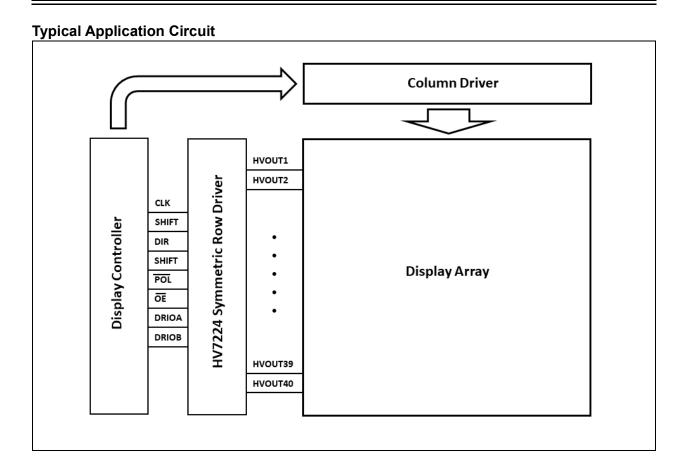
Functional Block Diagram





1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage, V _{DD}	–0.5V to +7V
High-Voltage Supply Voltage, V _{PP}	
Logic Input Levels	
Maximum Junction Temperature, T _{J(MAX)}	
Storage Temperature, T _S	
Continuous Total Power Dissipation:	
64-lead PQFP (Note 1)	1200 mW

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: For operations above 25°C ambient, derate linearly to maximum operating temperature at 20 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	4.5	_	5.5	V	
High-Voltage Supply Voltage	V_{PP}	0	_	240	V	Note 1
High-Level Input Voltage	V _{IH}	0.7 V _{DD}	_	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	_	0.2 V _{DD}	V	
Clock Frequency	f _{CLK}	_	_	3	MHz	
Operating Ambient Temperature	T _A	-40	_	+85	°C	
High-Voltage Output Current	I _O	_	_	±70	mA	
Allowable Current through Output Diodes	I _O	_	_	±300	mA	
Note 1: Output will not switch at V _{PP} = 0)V.					

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise stated, V_{DD} = 5V, V_{PP} = 240V, T_A = 25°C.

Parameter		Sym.	Min.	Тур.	Max.	Unit	Conditions
V _{DD} Supply Current	I _{DD}	_	_	10	mA	f _{CLK} = 3 MHz, V _{DD} = 5.5V	
V Supply Current			_	_	2	mA	All outputs low or High-Z
V _{PP} Supply Current		I _{PP}	_	_	4	mA	One output high (Note 1)
Quiescent V _{DD} Supply Current	I_{DDQ}		_	100	μΑ	All V_{IN} = GND or V_{DD}	
High-Level Logic Input Current		I _{IH}		_	1	μΑ	$V_{IH} = V_{DD}$
Low-Level Logic Input Current		I _{IL}		_	-1	μΑ	V _{IL} = 0V
High-Level Output Voltage	HV _{OUT}	V _{OH}	190	_		>	$I_{O} = -70 \text{ mA}$
Trigii-Level Output Voltage	Data Out		4.5	_		>	I _O = -100 μA
Low Lovel Output Voltage	HV _{OUT}	V.		_	50	>	I _O = 70 mA
Low-Level Output Voltage Data Out		V_{OL}		_	0.5	>	Ι _Ο = 100 μΑ
LIV Cotumetics Comment	P-channel	1.	-80	_	_	mA	
HV _{OUT} Saturation Current	N-channel	ISAT	75	_	_	mA	

Note 1: Only one output can be turned on at a time.

AC ELECTRICAL CHARACTERISTICS

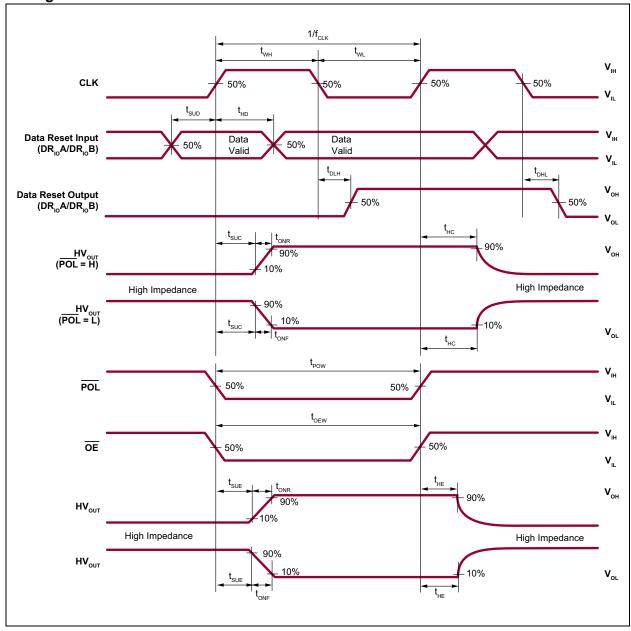
Electrical Specifications: V _{DD} = 5V and T _A = 25°C.							
Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions	
Clock Frequency	f _{CLK}	_	_	3	MHz	Per register, C _L = 15 pF	
Clock Width, High or Low	t_{WL} , t_{WH}	150	_	_	ns		
Data Setup Time before Clock Rises	t _{SUD}	50	_	_	ns		
Data Hold Time after Clock Rises	t _{HD}	50	_	_	ns		
HV _{OUT} Delay from Clock Rises (High-Z to H or L)	t _{suc}	_	_	1	μs	$C_L = 330 \text{ pF} // R_L = 10 \text{ k}\Omega$	
HV _{OUT} Delay from Output Enable OE Falls	t _{SUE}	_	_	600	ns	$C_L = 330 \text{ pF} // R_L = 10 \text{ k}\Omega$	
HV _{OUT} Delay from Clock Rises (H or L to High-Z)	t _{HC}	_	_	2	μs	$C_L = 330 \text{ pF } / / R_L = 10 \text{ k}\Omega$	
HV _{OUT} Delay from Output Enable OE Falls	t _{HE}	_	_	600	ns	$C_L = 330 \text{ pF} // R_L = 10 \text{ k}\Omega$	
Delay Time Clock to Data Output Falls	t _{DHL}	_	_	250	ns	C _L = 15 pF (Note 1)	
Delay Time Clock to Data Output Rises	t _{DLH}	_	_	250	ns	C _L = 15 pF (Note 1)	
HV _{OUT} Fall Time	t _{ONF}	_	_	2	μs	$C_L = 330 \text{ pF} // R_L = 10 \text{ k}\Omega$	
HV _{OUT} Rise Time	t _{ONR}		_	2	μs	$C_L = 330 \text{ pF} // R_L = 10 \text{ k}\Omega$	
POL Pulse Width	t _{POW}	3	_	_	μs		
Output Enable OE Pulse Width	t _{OEW}	3	_		μs		
Slew Rate, V _{PP}	SR	_	_	45	V/µs	One active output driving 4.7 nF load	

Note 1: The delay is measured from the trailing edge of the clock but the data is triggered by the rising edge of the clock. There is an internal delay for the data output which is equal to t_{WH}.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions		
TEMPERATURE RANGE								
Operating Ambient Temperature	T_A	-40	_	+85	°C			
Storage Temperature	T _S	- 65	_	+150	ŷ			
Maximum Junction Temperature	$T_{J(MAX)}$	-65	_	+150	°C			
PACKAGE THERMAL RESISTANCE								
64-lead PQFP	$\theta_{\sf JA}$		41	_	°C/W			

Timing Waveforms



2.0 PIN DESCRIPTION

The two pin function options for the HV7224 64-lead PQFP are specified in Table 2-1 and Table 2-2. Refer to **Package Type** for the location of pins.

TABLE 2-1: OPTION A PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT1/40	High-voltage output
2	HVOUT2/39	High-voltage output
3	HVOUT3/38	High-voltage output
4	HVOUT4/37	High-voltage output
5	HVOUT5/36	High-voltage output
6	HVOUT6/35	High-voltage output
7	HVOUT7/34	High-voltage output
8	HVOUT8/33	High-voltage output
9	HVOUT9/32	High-voltage output
10	HVOUT10/31	High-voltage output
11	HVOUT11/30	High-voltage output
12	HVOUT12/29	High-voltage output
13	HVOUT13/28	High-voltage output
14	HVOUT14/27	High-voltage output
15	HVOUT15/26	High-voltage output
16	HVOUT16/25	High-voltage output
17	HVOUT17/24	High-voltage output
18	HVOUT18/23	High-voltage output
19	HVOUT19/22	High-voltage output
20	HVOUT20/21	High-voltage output
21	VPP	High-voltage power supply
22	NC	No connection
23	GND (Power)	High-voltage supply ground
24	GND (Logic)	Logic supply ground
25	DIR	Direction pin
26	VDD	Logic supply voltage
27	CLK	Clock pin
28	NC	No connection
29	SHIFT	Shift pin
30	NC	No connection
31	DRIOA	Data reset pin A
32	NC	No connection
33	NC	No connection
34	DRIOB	Data reset pin B

Note: Pin designation for DIR H/L, Shift = L. Example: For DIR = H, Pin 1 is $HV_{OUT}1$

For DIR = L, Pin 1 is $HV_{OUT}40$

HV7224

TABLE 2-1: OPTION A PIN FUNCTION TABLE (CONTINUED)

TABLE 2-1.	OF HOMA FIN I GNOTION TABLE (CONTINUED)						
Pin Number	Pin Name	Description					
35	ŌE	Output Enable pin					
36	NC	No connection					
37	POL	Polarity pin					
38	NC	No connection					
39	VDD	Logic supply voltage					
40	NC	No connection					
41	GND (Logic)	Logic supply ground					
42	GND (Power)	High-voltage supply ground					
43	NC	No connection					
44	VPP	High-voltage power supply					
45	HVOUT21/20	High-voltage output					
46	HVOUT22/19	High-voltage output					
47	HVOUT23/18	High-voltage output					
48	HVOUT24/17	High-voltage output					
49	HVOUT25/16	High-voltage output					
50	HVOUT26/15	High-voltage output					
51	HVOUT27/14	High-voltage output					
52	HVOUT28/13	High-voltage output					
53	HVOUT29/12	High-voltage output					
54	HVOUT30/11	High-voltage output					
55	HVOUT31/10	High-voltage output					
56	HVOUT32/9	High-voltage output					
57	HVOUT33/8	High-voltage output					
58	HVOUT34/7	High-voltage output					
59	HVOUT35/6	High-voltage output					
60	HVOUT36/5	High-voltage output					
61	HVOUT37/4	High-voltage output					
62	HVOUT38/3	High-voltage output					
63	HVOUT39/2	High-voltage output					
64	HVOUT40/1	High-voltage output					

Note: Pin designation for DIR H/L, Shift = L.

Example: For DIR = H, Pin 1 is HV_{OUT}1
For DIR = L, Pin 1 is HV_{OUT}40

TABLE 2-2: OPTION B PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT20/21	High-voltage output
2	HVOUT19/22	High-voltage output
3	HVOUT18/23	High-voltage output
4	HVOUT17/24	High-voltage output
5	HVOUT16/25	High-voltage output
6	HVOUT15/26	High-voltage output
7	HVOUT14/27	High-voltage output
8	HVOUT13/28	High-voltage output
9	HVOUT12/29	High-voltage output
10	HVOUT11/30	High-voltage output
11	HVOUT10/31	High-voltage output
12	HVOUT9/32	High-voltage output
13	HVOUT8/33	High-voltage output
14	HVOUT7/34	High-voltage output
15	HVOUT6/35	High-voltage output
16	HVOUT5/36	High-voltage output
17	HVOUT4/37	High-voltage output
18	HVOUT3/38	High-voltage output
19	HVOUT2/39	High-voltage output
20	HVOUT1/40	High-voltage output
21	VPP	High-voltage power supply
22	NC	No connection
23	GND (Power)	High-voltage supply ground
24	GND (Logic)	Logic supply ground
25	DIR	Direction pin
26	VDD	Logic supply voltage
27	CLK	Clock pin
28	NC	No connection
29	SHIFT	Shift pin
30	NC	No connection
31	DRIOA	Data reset pin A
32	NC	No connection
33	NC	No connection
34	DRIOB	Data reset pin B
35	ŌĒ	Output enable pin
36	NC	No connection
37	POL	Polarity pin
38	NC	No connection
39	VDD	Logic supply voltage

Note: Pin designation for DIR H/L, Shift = H.

Example: For DIR = H, Pin 1 is HVOUT20

For DIR = L, Pin 1 is HVOUT21

HV7224

TABLE 2-2: OPTION B PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
		·
40	NC	No connection
41	GND (Logic)	Logic supply ground
42	GND (Power)	Ground power
43	NC	No connection
44	VPP	High-voltage power supply
45	HVOUT40/1	High-voltage output
46	HVOUT39/2	High-voltage output
47	HVOUT38/3	High-voltage output
48	HVOUT37/4	High-voltage output
49	HVOUT36/5	High-voltage output
50	HVOUT35/6	High-voltage output
51	HVOUT34/7	High-voltage output
52	HVOUT33/8	High-voltage output
53	HVOUT32/9	High-voltage output
54	HVOUT31/10	High-voltage output
55	HVOUT30/11	High-voltage output
56	HVOUT29/12	High-voltage output
57	HVOUT28/13	High-voltage output
58	HVOUT27/14	High-voltage output
59	HVOUT26/15	High-voltage output
60	HVOUT25/16	High-voltage output
61	HVOUT24/17	High-voltage output
62	HVOUT23/18	High-voltage output
63	HVOUT22/19	High-voltage output
64	HVOUT21/20	High-voltage output

Note: Pin designation for DIR H/L, Shift = H.

Example: For DIR = H, Pin 1 is HVOUT20 For DIR = L, Pin 1 is HVOUT21

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV7224.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

	Power-Up		Power-Down
Step	Description	Step	Description
1	Connect ground.	1	Remove V _{PP.} (Note 1)
2	Apply V _{DD} .	2	Remove all inputs.
3	Set all inputs (Data, CLK, EN, etc.) to a known state.	3	Remove V _{DD.}
4	Apply V _{PP.} (Note 1)	4	Disconnect ground.

Note 1: The V_{PP} should not drop below V_{DD} during operation.

TABLE 3-2: TRUTH FUNCTION TABLE

		Inputs				
I/O Relations	CLK	DIR	S/R DATA	POL	OE	High-voltage Outputs
O/P HIGH	Х	Х	Н	Н	L	Н
O/P OFF	Х	Х	L	Х	L	High-Z
O/P LOW	Х	Х	Н	L	L	L
O/P OFF	Х	Х	Х	Х	Н	All O/P High-Z

Note: H = High-logic level

L = Low-logic level

X = Irrelevant

Data input (DR_{IO}) loaded on the low-to-high transition of the clock.

Only one active output can be set at a time.

TABLE 3-3: OUTPUT SEQUENCE OPERATION TABLE

DIR	SHIFT	Data Reset In	Data Reset Out	HV _{OUT} # Sequence	Direction (Note 1)
L	L	DR _{IO} B	DR _{IO} A (Note 2)	40 → 1	•
Н	L	DR _{IO} A	DR _{IO} B (Note 3)	1 → 40	<u> </u>
L	Н	DR _{IO} B	DR _{IO} A (Note 2)	$20 \rightarrow 1 \rightarrow 40 \rightarrow 21$	$\overline{}$
Н	Н	DR _{IO} A	DR _{IO} B (Note 3)	$21 \rightarrow 40 \rightarrow 1 \rightarrow 20$	$ \uparrow $

Note 1: Reference to package outline or chip layout drawing

2: DR_{IO}A is DR_{IO}B delayed by 40 clock pulses.

3: DR_{IO}B is DR_{IO}A delayed by 40 clock pulses.

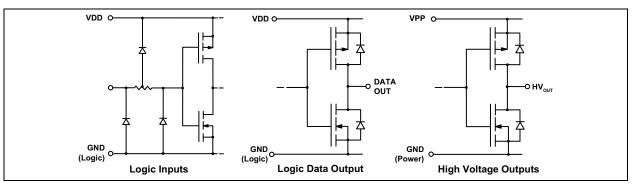
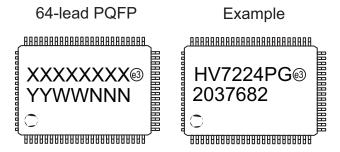


FIGURE 3-1: Input and Output Equivalent Circuits.

4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information

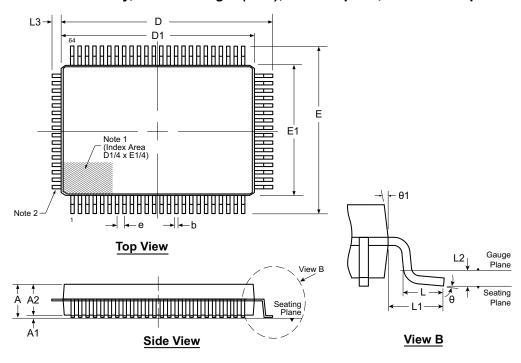


Legend: XX...X Product Code or Customer-specific information
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code
By-free JEDEC® designator for Matte Tin (Sn)
This package is Pb-free. The Pb-free JEDEC designator (a)
can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

64-Lead PQFP (3-Sided) Package Outline (PG)

20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

- A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
- The leads on this side are trimmed.

Symi	ool	Α	A1	A2	b	D	D1	Е	E1	е	L	L1	L2	L3	θ	θ1
Dimen- sion (mm)	MIN	2.80	0.25	2.55	0.30	22.25	19.80	17.65	13.80	0.80 BSC 0.88	0.73	1			0°	5°
	NOM	-	-	2.80	-	22.50	20.00	17.90	14.00		1.95 REF		0.55 REF	3.5°	-	
	MAX	3.40	0.50	3.05	0.45	22.75	20.20	18.15	14.20		1.03		200		7 °	16°

Drawings not to scale.



NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2020)

- Converted Supertex Doc # DSFP-HV7224 to Microchip DS20005895A
- Removed "HVCMOS® Technology" in the Features section
- · Changed the package marking format
- · Made minor changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>XX</u>	-	<u>X</u> - <u>X</u>	Example:	
Package Options		Environmental Media Type	a) HV7224PG-G:	40-Channel Symmetric Row Driver, 64-lead PQFP, 66/Tray
HV7224	=	40-Channel Symmetric Row Driver		
PG	=	64-lead PQFP		
G	=	Lead (Pb)-free/RoHS-compliant Package		
(blank)	=	66/Tray for a PG Package		
	Package Options HV7224 PG G	Package Options HV7224 = PG = G =	Package Options Environmental Media Type HV7224 = 40-Channel Symmetric Row Driver PG = 64-lead PQFP G = Lead (Pb)-free/RoHS-compliant Package	Package Options Environmental Media Type a) HV7224PG-G: HV7224 = 40-Channel Symmetric Row Driver PG = 64-lead PQFP G = Lead (Pb)-free/RoHS-compliant Package

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