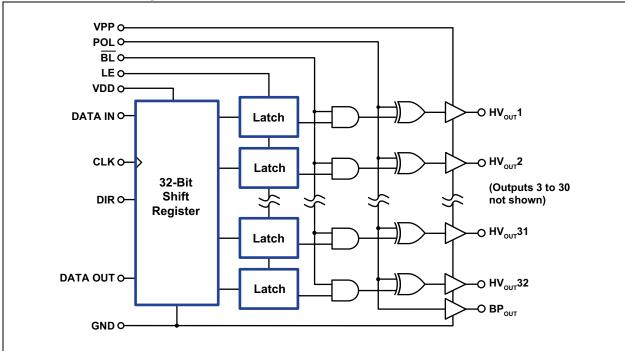
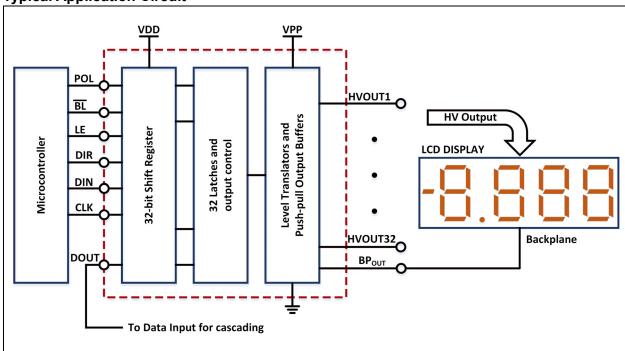
Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Logic Supply Voltage, V _{DD} (Note 1)	–0.5V to +7V
High-Voltage Supply Voltage, V _{PP} (Note 1)	–0.5V to +70V
Logic Input Levels	
Ground Current (Note 2)	
Maximum Junction Temperature, T _{J(MAX)}	
Storage Temperature, T _S	–65°C to +125°C
Continuous Total Power Dissipation:	
44-lead PQFP (Note 3)	1200 mW
44-lead PLCC (Note 3)	1200 mW
• • • • • • • • • • • • • • • • • • • •	

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

- Note 1: All voltages are referenced to GND.
 - **2:** Duty cycle is limited by the total power dissipated in the package.
 - 3: For operations above 25°C ambient, derate linearly to 85°C at 20 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	4.5	_	5.5	V	
High-Voltage Supply Voltage	V_{PP}	12	_	60	V	
High-Level Input Voltage	V_{IH}	2.4	_	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	_	0.8	V	
Clock Frequency	f _{CLK}	0	_	5	MHz	
Operating Ambient Temperature	T_A	-40	_	+85	°C	
Allowable Current through Output Diodes	I _{OD}	_	_	200	mA	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise stated. V _{DD} = 5V, V _{PP} = 60V.												
Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions						
V _{DD} Supply Current		I _{DD}	_	_	15	mA	f _{CLK} = 5 MHz, V _{DD} = 5.5V					
Quiescent V _{PP} Supply Current		I _{PPQ}	_	_	0.5	mA						
Quiescent V _{DD} Supply Current		I _{DDQ}	_	_	0.5	mA	All V _{IN} = GND or VDD					
High-Level Logic Input Current	I _{IH}	_	_	1	μΑ	$V_{IH} = V_{DD}$						
Low-Level Logic Input Current	I _{IL}	_	_	-1	μΑ	V _{IL} = 0V						
High-Level Output Data Out	HV _{OUT}	\/	50	_	_	V	$I_{O} = -5 \text{ mA}, V_{PP} = 60 \text{V}$					
High-Level Output Data Out	Data Out	V _{OH}	4.6	_	_	V	I _O = -100 μA					
Low Lovel Output Voltage	HV _{OUT}	\/	_	_	8	V	$I_O = 5 \text{ mA}, V_{PP} = 60 \text{V}$					
Low-Level Output Voltage	Data Out	V _{OL}	_	_	0.4	V	I _O = 100 μA					
Low-Level Output Voltage, Backp	V _{OLBP}	_	_	3	V	I _O = 10 mA						
High-Level Output Voltage, Back	olane	V _{OHBP}	57	_	_	V	I _O = -10 mA					

AC ELECTRICAL CHARACTERISTICS

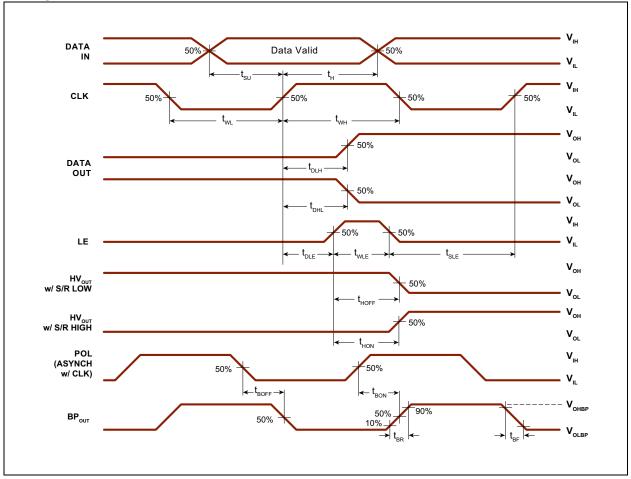
Electrical Specifications: V _{DD} = 5V, V _{PP} = 60V, T _A = 25°C, Logic Input Rise/Fall Time = 10 ns.											
Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions					
Clock Frequency	f _{CLK}		_	5	MHz						
Clock Width, High or Low	t_{WL} , t_{WH}	100	_	_	ns						
Data Setup Time before Clock Rises	t _{SU}	25	_	_	ns						
Data Hold Time after Clock Rises	t _H	50	_	_	ns						
Time from Latch Enable or POL to HV _{OUT}	t _{HON,} t _{HOFF}	ı	_	500	ns	C _L = 20 pF					
Time from POL to BP _{OUT}	t _{BON,} t _{BOFF}		_	500	ns	C _L = 20 pF					
Delay Time Clock to Data High to Low	t _{DHL}			200	ns	C _L = 10 pF					
Delay Time Clock to Data Low to High	t _{DLH}		_	200	ns	C _L = 10 pF					
Delay Time Clock to Latch Enable Low to High	t _{DLE}	50	_	_	ns						
Latch Enable Pulse Width	t _{WLE}	100	_	_	ns						
Latch Enable Setup Time before Clock Falls	t _{SLE}	50	_	_	ns						
BP _{OUT} Rise and Fall Time	t _{BR} , t _{BF}	10	_	1000	μs	C _L = 350 pF					
BP _{OUT} Rise and Fall Time Difference	t _{BR} -t _{BF}		_	100	μs	C _L = 350 pF					

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T _A	-40	_	+85	°C	
Storage Temperature	T _S	-65	_	+125	°C	
PACKAGE THERMAL RESISTANCE						
44-lead PQFP	θ_{JA}	_	51	_	°C/W	
44-lead PLCC	θ_{JA}	_	37	_	°C/W	

HV66

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV66 44-lead PQFP and 44-lead PLCC are in Table 2-1 and Table 2-2, respectively. Refer to **Package Types** for the location of pins.

TABLE 2-1: 44-LEAD PQFP PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT11	High-voltage output
2	HVOUT12	High-voltage output
3	HVOUT13	High-voltage output
4	HVOUT14	High-voltage output
5	HVOUT15	High-voltage output
6	HVOUT16	High-voltage output
7	HVOUT17	High-voltage output
8	HVOUT18	High-voltage output
9	HVOUT19	High-voltage output
10	HVOUT20	High-voltage output
11	HVOUT21	High-voltage output
12	HVOUT22	High-voltage output
13	HVOUT23	High-voltage output
14	HVOUT24	High-voltage output
15	HVOUT25	High-voltage output
16	HVOUT26	High-voltage output
17	HVOUT27	High-voltage output
18	HVOUT28	High-voltage output
19	HVOUT29	High-voltage output
20	HVOUT30	High-voltage output
21	HVOUT31	High-voltage output
22	HVOUT32	High-voltage output
23	DATA OUT	Data output pin
24	GND	Supply ground
25	NC	No connection
26	BL	Blanking pin
27	POL	Polarity pin
28	LE	Latch enable pin
29	VDD	Logic supply voltage
30	CLK	Clock pin
31	DIR	Direction pin
32	DATA IN	Data input pin
33	VPP	High-voltage power supply
34	BPOUT	Back plane output
35	HVOUT1	High-voltage output
36	HVOUT2	High-voltage output

HV66

TABLE 2-1: 44-LEAD PQFP PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description								
37	HVOUT3	High-voltage output								
38	HVOUT4	High-voltage output								
39	HVOUT5	High-voltage output								
40	HVOUT6	High-voltage output								
41	HVOUT7	High-voltage output								
42	HVOUT8	High-voltage output								
43	HVOUT9	High-voltage output								
44	HVOUT10	High-voltage output								

TABLE 2-2: 44-LEAD PLCC PIN FUNCTION TABLE

TT-LLAD I LO	C FIN FUNCTION TABLE
Pin Name	Description
HVOUT16	High-voltage output
HVOUT17	High-voltage output
HVOUT18	High-voltage output
HVOUT19	High-voltage output
HVOUT20	High-voltage output
HVOUT21	High-voltage output
HVOUT22	High-voltage output
HVOUT23	High-voltage output
HVOUT24	High-voltage output
HVOUT25	High-voltage output
HVOUT26	High-voltage output
HVOUT27	High-voltage output
HVOUT28	High-voltage output
HVOUT29	High-voltage output
HVOUT30	High-voltage output
HVOUT31	High-voltage output
HVOUT32	High-voltage output
DATA OUT	Data output pin
GND	Supply ground
NC	No connection
BL	Blanking pin
POL	Polarity pin
LE	Latch enable pin
VDD	Logic supply voltage
CLK	Clock pin
DIR	Direction pin
DATA IN	Data input pin
VPP	High-voltage power supply
	Pin Name HVOUT16 HVOUT17 HVOUT18 HVOUT20 HVOUT21 HVOUT21 HVOUT22 HVOUT23 HVOUT24 HVOUT25 HVOUT26 HVOUT27 HVOUT28 HVOUT29 HVOUT30 HVOUT31 HVOUT31 HVOUT32 DATA OUT GND NC BL POL LE VDD CLK DIR DATA IN

TABLE 2-2: 44-LEAD PLCC PIN FUNCTION TABLE (CONTINUED)

IABLE E E.	TT LLAD I LO	of hit one had table (continues)
Pin Number	Pin Name	Description
29	BPOUT	Black plane output
30	HVOUT1	High-voltage output
31	HVOUT2	High-voltage output
32	HVOUT3	High-voltage output
33	HVOUT4	High-voltage output
34	HVOUT5	High-voltage output
35	HVOUT6	High-voltage output
36	HVOUT7	High-voltage output
37	HVOUT8	High-voltage output
38	HVOUT9	High-voltage output
39	HVOUT10	High-voltage output
40	HVOUT11	High-voltage output
41	HVOUT12	High-voltage output
42	HVOUT13	High-voltage output
43	HVOUT14	High-voltage output
44	HVOUT15	High-voltage output

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV66.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

	Power-up	Power-down				
Step	Description	Step	Description			
1	Connect ground.	1	Remove V _{PP.} (Note 1)			
2	Apply V _{DD} .	2	Remove all inputs.			
3	Set all inputs (Data, CLK, EN, etc.) to a known state.	3	Remove V _{DD.}			
4	Apply V _{PP.} (Note 1)	4	Disconnect ground.			

Note 1: The V_{PP} should not drop below V_{DD} during operation.

TABLE 3-2: TRUTH FUNCTION TABLE

		Inputs Outputs								Outputs																																				
Function	Data	CLK	LE	BL	POL	DIR	Shift Reg	ister		n-voltage Output	Data Out	BP _{OUT}																																		
			1 2	32	1	232	*																																							
Load S/R,	L or H	1	L	Ignore	Ignore	Н	$\text{Data} \to \text{Q}_1$		gnore	Q ₃₂	Ignore																																			
R/L Shift	L or H	1	L	Ignore	Ignore	L	Q ₁ ←Q ₃₂ ← Data		$Q_1 {\leftarrow} Q_{32} \leftarrow Data$		$Q_1 \leftarrow Q_{32} \leftarrow Data$		$Q_1 \leftarrow Q_{32} \leftarrow Data$		$Q_1 \leftarrow Q_{32} \leftarrow Data$		Q ₁ ←Q ₃₂ ← Data		$Q_1 {\leftarrow} Q_{32} \leftarrow Data$		Q ₁ ←Q ₃₂ ← Data		$Q_1 {\leftarrow} Q_{32} \leftarrow Data$		$Q_1 {\leftarrow} Q_{32} \leftarrow Data$		$Q_1 {\leftarrow} Q_{32} \leftarrow Data$		$Q_1 {\leftarrow} Q_{32} \leftarrow Data$		Q ₁ ←Q ₃₂ ← Data		$Q_1 {\leftarrow} Q_{32} \leftarrow Data$		$Q_1 {\leftarrow} Q_{32} \leftarrow Data$		$Q_1 \leftarrow Q_{32} \leftarrow Data$		Q ₁ ←Q ₃₂ ← Data		I	gnore	Q_1	Ignore		
Load	Χ	H or L	Н	Н	Η	Χ	**	**		* *	No Change	Η																																		
Latches	Х	H or L	Н	Н	L	Х	**	** ** No Char		No Change	L																																			
	L or H	1	Н	Н	Η	Η	$\text{Data} \to \text{Q}_1$	$\rightarrow Q_{32}$		* *	Q ₃₂	Η																																		
Transparent	L or H	1	Н	Н	L	Н	Data $\rightarrow Q_1 \rightarrow Q_{32}$			* *	Q ₃₂	L																																		
Mode	L or H	1	Н	Н	Η	L	$Q_1 {\leftarrow} Q_{32} \leftarrow Data$		$Q_1 \leftarrow Q_{32} \leftarrow Data$		$Q_1 \leftarrow Q_{32} \leftarrow Data$		Q ₁ ←Q ₃₂ ← Data **		Q_1	Η																														
	L or H	1	Н	Н	L	L	Q ₁ ←Q ₃₂ ← Data		Q ₁ ←Q ₃₂ ← Data		$Q_1 {\leftarrow} Q_{32} \leftarrow Data$		$Q_1 \leftarrow Q_{32} \leftarrow Data$		$Q_1 \leftarrow Q_{32} \leftarrow Data$		$Q_1 \leftarrow Q_{32} \leftarrow Data$		Q ₁ ←Q ₃₂ ← Data		Q ₁ ←Q ₃₂ ← Data			* *	Q_1	L																				
Blank	Х	Х	Χ	L	L	Х	X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X			LL	Ignore	L
Control	Х	Х	Χ	L	Ι	X	Х НН			Ignore	Ι																																			

Note: H = High-logic level

L = Low-logic level

X = Irrelevant

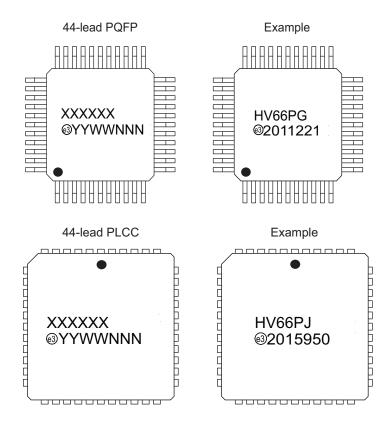
Ignore = The state of the specific input or output is irrelevant to demonstrate the occurred event.

↑ = Low-to-high transition

* = Dependent on the previous stage's state before the last CLK or last LE high

4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information



Legend: XX...X Product Code or Customer-specific information

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code

e3 Pb-free JEDEC® designator for Matte Tin (Sn)

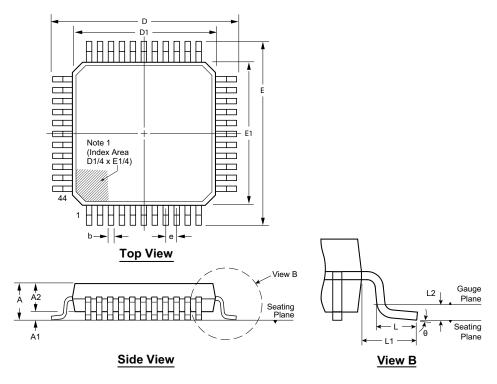
This package is Pb-free. The Pb-free JEDEC designator (e3)

can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

44-Lead PQFP Package Outline (PG)

10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note

 A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbo	ol	Α	A1	A2	b	D	D1	E	E1	е	L	L1	L2	θ
	MIN	1.95*	0.00	1.95	0.30	13.65*	9.80*	13.65*	9.80*		0.73			0 º
Dimension (mm)	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00	0.80 BSC	0.88	1.95 REF	0.25 BSC	3.5°
()	MAX	2.35	0.25	2.10	0.45	14.15*	10.20*	14.15*	10.20*		1.03			7°

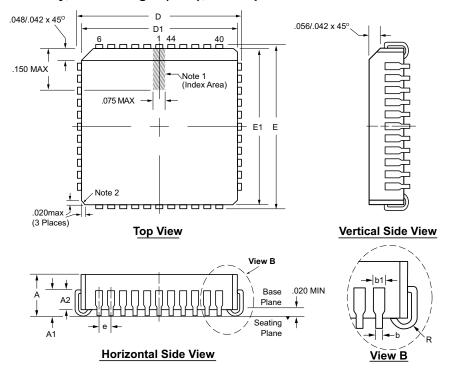
JEDEC Registration MO-112, Variation AA-2, Issue B, Sep.1995.

Drawings not to scale.

^{*} This dimension is not specified in the JEDEC drawing.

44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max), .050in pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging. Notes:

- 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
- Actual shape of this feature may vary.

Symbol		Α	A1	A2	b	b1	D	D1	Е	E1	е	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036 [†]	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993. † This dimension differs from the JEDEC drawing. **Drawings not to scale.**



NOTES:

APPENDIX A: REVISION HISTORY

Revision A (January 2020)

- Converted Supertex Doc # DSFP-HV66 to Microchip DS20005886A
- Removed "HVCMOS® Technology" from the Features section
- Changed the package marking format
- Updated the 44-lead PQFP PG M919 and 44-lead PLCC PJ M903 media types
- · Made minor changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	<u>XX</u>	-	<u>x</u> -	<u>X</u>		Examples:	
Device	Package Options		Environmental	Media Ty	pe	a) HV66PG-G:	32-Channel LCD Driver with Separate Backplane Output, 44-lead PQFP, 96/Tray
Device:	HV66	=	32-Channel LCD Dri Backplane Output	ver with Sepa	arate	b) HV66PJ-G:	32-Channel LCD Driver with Separate Backplane Output, 44-lead PLCC, 27/Tube
Packages:	PG	=	44-lead PQFP				
	PJ	=	44-lead PLCC				
Environmental:	G	=	Lead (Pb)-free/RoHS	G-compliant P	'ackage		
Media Types:	(blank)	=	96/Tray for a PG Pag	ckage			
	(blank)	=	27/Tube for a PJ Pag	kage			

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