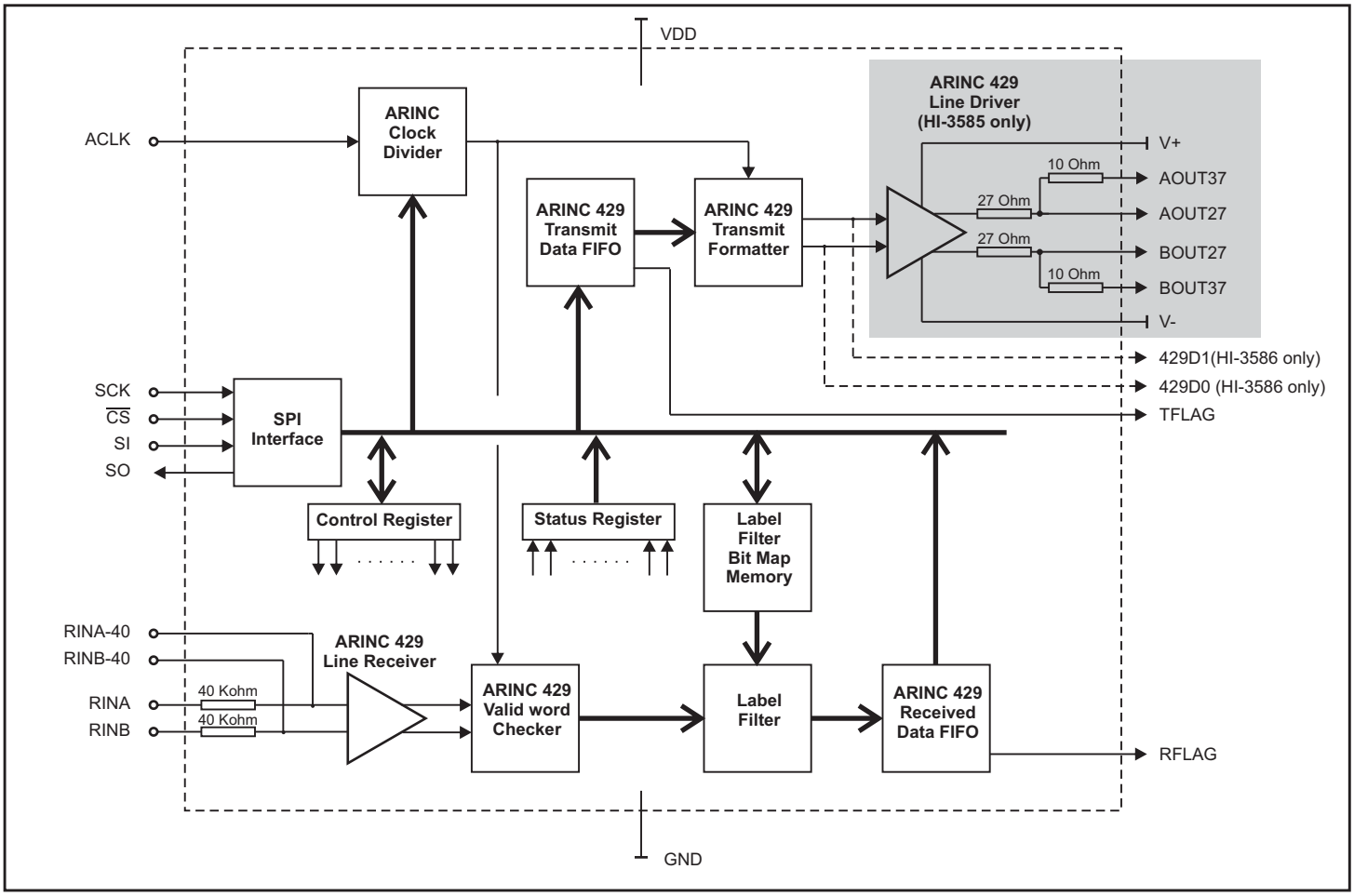
BLOCK DIAGRAM



PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION	NOTE
RINB	INPUT	ARINC receiver negative input. Direct connection to ARINC 429 bus	
RINB-40	INPUT	Alternate ARINC receiver negative input. Requires external 40K ohm resistor	
MR	INPUT	Master Reset. A positive pulse clears Receive and Transmit data FIFOs and flags	10K ohm pull-down*
SI	INPUT	SPI interface serial data input	10K ohm pull-down*
$\overline{CS}$	INPUT	Chip select. Data is shifted into SI and out of SO when $\overline{CS}$ is low.	10K ohm pull-up*
SCK	INPUT	SPI Clock. Data is shifted into or out of the SPI interface using SCK	10K ohm pull-down*
GND	POWER	Chip 0V supply	
ACLK	INPUT	Master timing source for the ARINC 429 receiver and transmitter	10K ohm pull-down*
SO	OUTPUT	SPI interface serial data output	
RFLAG	OUTPUT	Goes high when ARINC 429 Receive FIFO is empty (CR15=0), or full (CR15=1)	
TFLAG	OUTPUT	Goes high when ARINC 429 Transmit FIFO is empty (CR14=0), or full (CR14=1)	
V-	POWER	Minus 5V power supply to ARINC 429 Line Driver	(HI-3585 only)
BOUT37	OUTPUT	ARINC line driver negative output. Direct connection to ARINC 429 bus	(HI-3585 only)
BOUT27	OUTPUT	Alternate ARINC line driver negative output. Requires external 10 ohm resistor	(HI-3585 only)
AOUT27	OUTPUT	Alternate ARINC line driver positive output. Requires external 10 ohm resistor	(HI-3585 only)
AOUT37	OUTPUT	ARINC line driver positive output. Direct connection to ARINC 429 bus	(HI-3585 only)
V+	POWER	Positive 5V power supply to ARINC 429 Line Driver	(HI-3585 only)
VDD	POWER	3.3V or 5.0V logic power	
RINA-40	INPUT	Alternate ARINC receiver positive input. Requires external 40K ohm resistor	
RINA	INPUT	ARINC receiver positive input. Direct connection to ARINC 429 bus	
429D1	OUTPUT	Digital positive output to external line driver	(HI-3586 only)
429D0	OUTPUT	Digital negative output to external line driver	(HI-3586 only)

* Internal Pull-up or Pull-down

INSTRUCTIONS

Instruction op codes are used to read, write and configure the HI-3585. When $\overline{CS}$ goes low, the next 8 clocks at the SCK pin shift an instruction op code into the decoder, starting with the first positive edge. The op code is fed into the SI pin most significant bit first.

For write instructions, the most significant bit of the data word must immediately follow the instruction op code and is clocked into its register on the next rising SCK edge. Data word length varies depending on word type written: 16-bit writes to Control Register, 32-bit ARINC word writes to transmit FIFO or 256-bit writes to the label-matching enable/disable table.

For read instructions, the most significant bit of the requested data word appears at the SO pin after the last op code bit is clocked into the decoder, at the next falling SCK edge. As with write instructions, data field bit-length varies with read instruction type.

Table 1 lists all instructions. Instructions that perform a reset or set, or enable transmission are executed after the last SI bit is received while $\overline{CS}$ is still low.

Example:

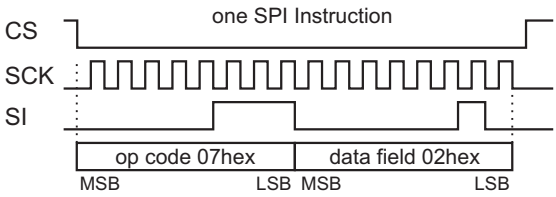


TABLE 1. DEFINED INSTRUCTION OP CODES

OP CODE Hex	DATA FIELD	DESCRIPTION
00	None	No instruction implemented
01	None	After the 8th op code bit is received, perform Master Reset (MR)
02	None	After the 8th op code bit is received, reset all label selections
03	None	After the 8th op code bit is received, set all the label selections
04	8 bits	Reset the label at the address specified in the data field
05	8 bits	Set the label at the address specified in the data field
06	256 bits	Starting with label FF hex, consecutively set or reset each label in descending order For example, a Data Field pattern starting with 1011 will set labels FF, FD, and FC hex and reset label FE hex
07	8 bits	Programs a division of the ACLK input. If the divided ACLK frequency is 1 MHz and Control Register bit CR1 is set, the ARINC receiver and transmitter operate from the divided ACLK clock. Allowable values for division rate are X1, X2, X4, X8, or XA hex. Any other programmed value results in no clock. Note: ACLK input frequency and division ratio must yield 1 MHz clock.
08	32 bits	Read the next word in the Receive FIFO. See note in Status Register section on next page.
09	None	No Instruction Implemented
0A	8 bits	Read the Status Register
0B	16 bits	Read the Control Register
0C	8 bits	Read the ACLK divide value programmed previously using op code 07 hex
0D	256 bits	Read the Label look-up memory table consecutively starting with address FF hex.
0E	N x 32 Bits	Write up to 32 words into the next empty positions of the Transmit FIFO
0F	None	No instruction implemented
10	16 bits	Write the Control Register
11	None	Reset the Transmit FIFO. After the 8th op code bit is received, the transmit FIFO will be empty
12	None	Transmission enabled by this instruction only if Control Register bit 13 is zero

FUNCTIONAL DESCRIPTION

CONTROL WORD REGISTER

The HI-3585 contains a 16-bit Control Register which is used to configure the device. Control Register bits CR15 - CR0 are loaded from a 16-bit data value appended to SPI instruction 10 hex. The Control Register contents may be read using SPI instruction 0B hex. Each bit of the Control Register has the following function:

CR Bit	FUNCTION	STATE	DESCRIPTION
Cr0 (LSB)	Receiver Data Rate Select	0	Data rate = CLK/10 (ARINC 429 High-Speed)
		1	Data rate = CLK/80 (ARINC 429 Low-Speed)
CR1	ARINC Clock Source Select	0	ARINC CLK = ACLK input frequency
		1	ARINC CLK = ACLK divided by the value programmed with SPI Instruction 07 hex
CR2	Enable Label Recognition	0	Label recognition disabled
		1	Label recognition enabled
CR3	Transmitter Parity Bit Enable	0	Transmitter 32nd bit is data
		1	Transmitter 32nd bit is parity
CR4	Receiver Parity Check Enable	0	Receiver parity check disabled
		1	Receiver odd parity check enabled
CR5	Self Test	0	The transmitter's digital outputs are internally connected to the receiver logic inputs
		1	Normal operation
CR6	Receiver Decoder	0	Receiver decoder disabled
		1	ARINC bits 10 and 9 must match CR7 and CR8
CR7	-	-	If receiver decoder is enabled, the ARINC bit 10 must match this bit
CR8	-	-	If receiver decoder is enabled, the ARINC bit 9 must match this bit
CR9	Transmitter Parity Select	0	Transmitter 32nd bit is Odd parity
		1	Transmitter 32nd bit is Even parity
CR10	Transmitter Data Rate	0	Data rate = CLK/10, O/P slope = 1.5us
		1	Data rate = CLK/80, O/P slope = 10us
CR11	ARINC Label Bit Order	0	Label bit order reversed (See Table 2)
		1	Label bit order same as transmitted / received (See Table 2)
CR12	Disable Line Driver	0	Line Driver enabled
		1	Line Driver disabled (force outputs to Null state)
CR13	Transmission Enable Mode	0	Start transmission by SPI instruction12 hex
		1	Transmit whenever data is available in the Transmit FIFO
CR14	TFLAG Definition	0	TFLAG goes high when transmit FIFO is empty
		1	TFLAG goes high when transmit FIFO is full
CR15 (MSB)	RFLAG Definition	0	RFLAG goes high when receive FIFO is empty
		1	RFLAG goes high when receive FIFO is full

STATUS REGISTER

The HI-3585 contains an 8-bit Status Register which can be interrogated to determine the status of the ARINC receiver, data FIFOs and transmitter. The contents of the Status Register are output using SPI instruction 0A hex. Unused bits are output as Zeros. The following table defines the Status Register bits.

NOTE: Reading an empty FIFO will return zeros. However, this is not a recommended method to determine if the FIFO is empty. The host should first examine the Status Register FIFO flags or read the RFLAG pin to determine the FIFO status. Reading the FIFO data without first checking the FIFO flags or the RFLAG pin may result in lost ARINC 429 words.

SR Bit	FUNCTION	STATE	DESCRIPTION
SR0 (LSB)	Receive FIFO Empty	0	Receiver FIFO contains valid data Sets to One when all data has been read. RFLAG pin reflects the state of this bit when CR15=0
		1	Receiver FIFO is empty
SR1	Receive FIFO Half Full	0	Receiver FIFO holds less than 16 words
		1	Receiver FIFO holds at least 16 words
SR2	Receive FIFO Full	0	Receiver FIFO not full. RFLAG pin reflects the state of this bit when CR15=1
		1	Receiver FIFO full. To avoid data loss, the FIFO must be read within one ARINC word period
SR3	Transmit FIFO Empty	0	Transmit FIFO not empty. Sets to One when all data has been sent. TFLAG pin reflects the state of this bit when CR14=0
		1	Transmit FIFO is empty.
SR4	Transmit FIFO Half Full	0	Transmit FIFO contains less than 16 words
		1	Transmit FIFO contains at least 16 words
SR5	Transmit FIFO Full	0	Transmit FIFO not full. TFLAG pin reflects the state of this bit when CR14=1
		1	Transmit FIFO full.
SR6	Not used	0	Always "0"
SR7 (MSB)	Not used	0	Always "0"

FUNCTIONAL DESCRIPTION (cont.)

ARINC 429 DATA FORMAT

Control Register bit CR11 controls how individual bits in the received or transmitted ARINC word are mapped to the HI-3585 SPI data word bits during data read or write operations. The following table describes this mapping:

Table 2. SPI / ARINC bit-mapping

SPI Order	1	2 - 22	23	24	25	26	27	28	29	30	31	32
ARINC bit	32	31 - 11	10	9	1	2	3	4	5	6	7	8
CR11=0	Parity	Data	SDI	SDI	Label (MSB)	Label	Label	Label	Label	Label	Label	Label (LSB)
ARINC bit	32	31 - 11	10	9	8	7	6	5	4	3	2	1
CR11=1	Parity	Data	SDI	SDI	Label (LSB)	Label	Label	Label	Label	Label	Label	Label (MSB)

ARINC 429 RECEIVER

ARINC BUS INTERFACE

Figure 1 shows the input circuit for the on-chip ARINC 429 line receiver. The ARINC 429 specification requires the following detection levels:

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 Volts to +13 Volts
NULL	+2.5 Volts to -2.5 Volts
ZERO	-6.5 Volts to -13 Volts

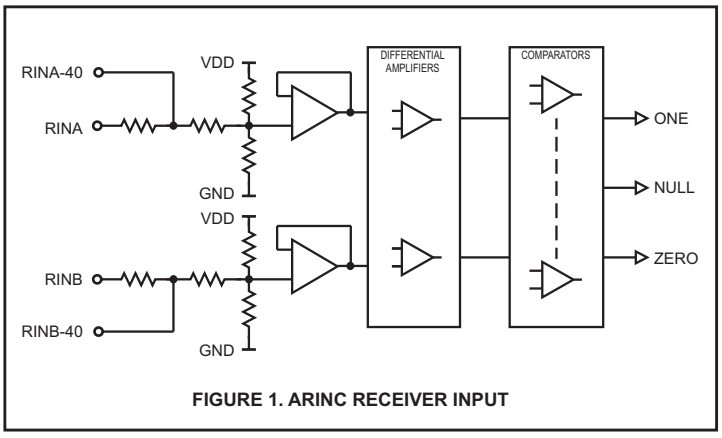


FIGURE 1. ARINC RECEIVER INPUT

The HI-3585 guarantees recognition of these levels with a common mode voltage with respect to GND less than ±30V for the worst case condition (3.15V supply and 13V signal level).

Design tolerances guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal (including nulls) is outside the differential voltage ranges, the HI-3585 receiver rejects the data.

RECEIVER LOGIC OPERATION

Figure 2 is a block diagram showing receiver logic.

BIT TIMING

The ARINC 429 specification defines the following timing tolerances for received data:

	HIGH SPEED	LOW SPEED
BIT RATE	100K BPS ± 1%	12K -14.5K BPS
PULSE RISE TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE FALL TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE WIDTH	5 µsec ± 5%	34.5 to 41.7 µsec

The HI-3585 accepts signals within these tolerances and rejects signals outside these tolerances. Receiver logic achieves this as described below:

1. An accurate 1MHz clock source is required to validate the receive signal timing. Less than 1% error is recommended.

2. The receiver uses three separate 10-bit sampling shift registers for Ones detection, Zeros detection and Null detection. When the input signal is within the differential voltage range for any shift register's state (One Zero or Null) sampling clocks a high bit into that register. When the receive signal is outside the differential voltage range defined for any shift register, a low bit is clocked. Only one shift register can clock a high bit for any given sample. All three registers clock low bits if the differential input voltage is between defined state voltage bands.

Valid data bits require at least three consecutive One or Zero samples (three high bits) in the upper half of the Ones or Zeros sampling shift register, and at least three consecutive Null samples (three high bits) in the lower half of the Null sampling shift register within the data bit interval.

A word gap Null requires at least three consecutive Null samples (three high bits) in the upper half of the Null sampling shift register and at least three consecutive Null samples (three high bits) in the lower half of the Null sampling shift register. This guarantees the minimum pulse width.

3. To validate the receive data bit rate, each bit must follow its preceding bit by not less than 8 samples and not more than 12 samples. With exactly 1MHz input clock frequency, the acceptable data bit rates are:

	HIGH SPEED	LOW SPEED
DATA BIT RATE MIN	83K BPS	10.4K BPS
DATA BIT RATE MAX	125K BPS	15.6K BPS

4. Following the last data bit of a valid reception, the Word Gap timer samples the Null shift register every 10 input clocks (every 80 clocks for low speed). If a Null is present, the Word Gap counter is incremented. A Word Gap count of 3 enables the next reception.

FUNCTIONAL DESCRIPTION (cont.)

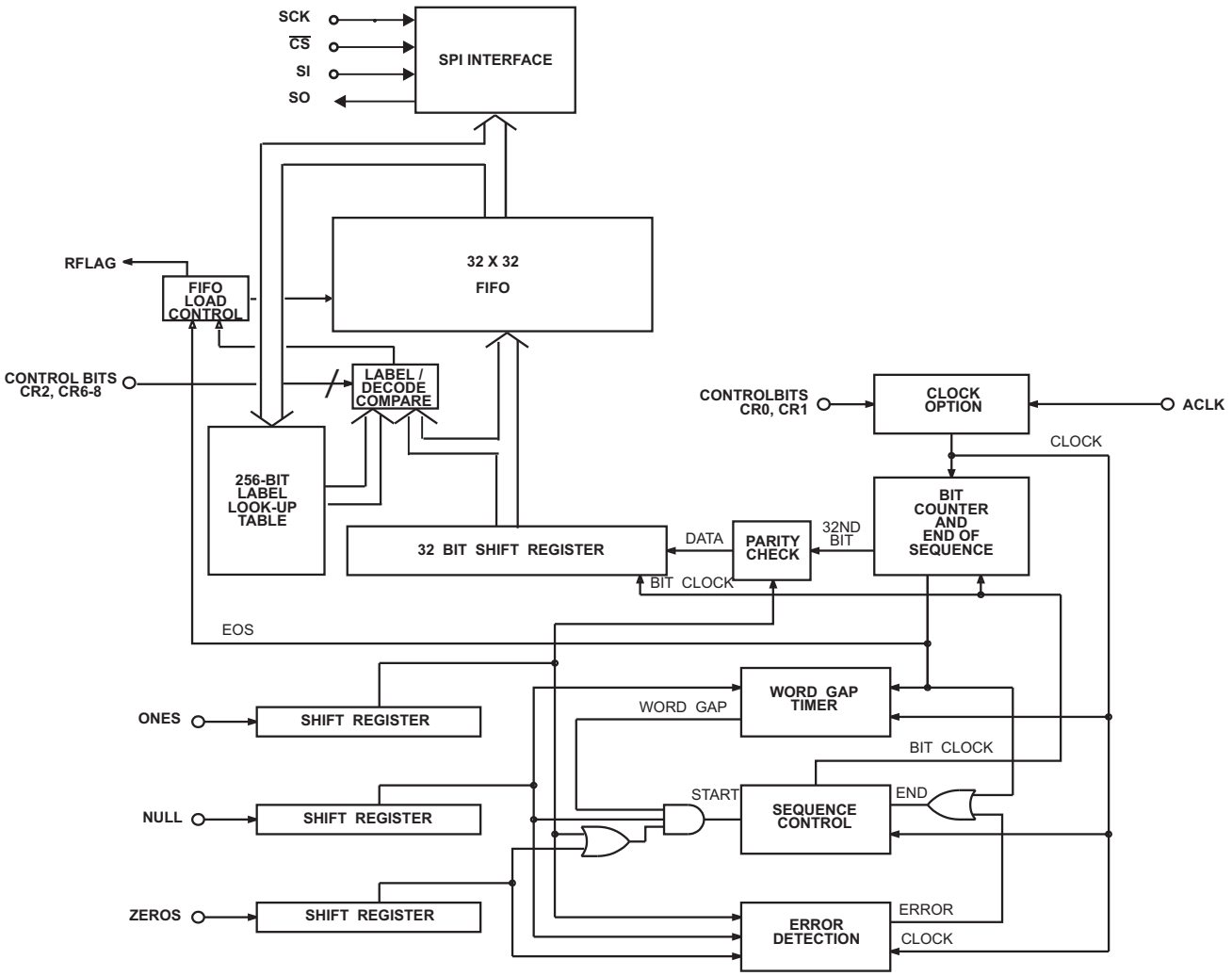


FIGURE 2. **RECEIVER BLOCK DIAGRAM**

FUNCTIONAL DESCRIPTION (cont.)

RETRIEVING DATA

Once 32 valid bits are recognized, the receiver logic generates an End of Sequence (EOS). Depending on the state of Control Register bits CR2, CR6, CR7 and CR8, the received 32-bit ARINC word is then checked for correct decoding and label match before it is loaded into the 32 x 32 Receive FIFO. ARINC words that do not match required 9th and 10th ARINC bit and do not have a label match are ignored and are not loaded into the Receive FIFO. The adjacent table describes this operation.

Once a valid ARINC word is loaded into the FIFO, the EOS signal clocks the Data Ready flip-flop to a "1" and Status Register bit 0 (SR0) to a “0”. The SR0 bit remains low until the Receive FIFO is empty. Each received ARINC word is retrieved via the SPI interface using SPI instruction 08 hex to read a single word.

Up to 32 ARINC words may be held in the Receive FIFO. Status register bit 2 (SR2) goes high when the Receive FIFO is full. Failure to unload the Receive FIFO when full causes additional received valid ARINC words to overwrite Receive FIFO location 32.

A FIFO half-full flag (SR1) is high when the Receive FIFO contains 16 or more ARINC words. SR1 may be interrogated by the system’s external microprocessor, allowing a 16 word data retrieval routine to be performed.

TABLE 3. FIFO LOADING CONTROL

CR2	ARINC word matches Enabled label	CR6	ARINC word bits 10, 9 match CR7, 8	FIFO
0	X	0	X	Load FIFO
1	No	0	X	Ignore data
1	Yes	0	X	Load FIFO
0	X	1	No	Ignore data
0	X	1	Yes	Load FIFO
1	Yes	1	No	Ignore data
1	No	1	Yes	Ignore data
1	No	1	No	Ignore data
1	Yes	1	Yes	Load FIFO

RECEIVER PARITY

The Receiver Parity Check Enable bit (Control Register bit 4, CR4) controls how the 32nd bit of the received ARINC word is interpreted by the HI-3585 receiver.

When CR4 is set to a “0”, the 32nd bit is treated as data and transferred as received from the ARINC bus to the receive FIFO.

When CR4 is set to a “1”, the 32nd bit is treated as a parity error bit.

Odd Parity Received
The receiver expects the 32nd bit of the received word to indicate odd parity. If this is the case, the parity bit is reset to indicate correct parity was received and resulting word is written to the receive FIFO.

Even Parity Received
If the received word is even parity, the receiver sets the 32nd bit to a “1”, indicating a parity error. The resulting word is then written to the receive FIFO.

Therefore, when CR4 is set to “1”, the 32nd bit retrieved from the receiver FIFO will always be “0” when valid (odd parity) ARINC 429 words are received.

CR4	ARINC BUS 32nd bit	FIFO 32nd bit
0	data	data
1	parity bit	Error Bit: 0 = odd parity 1= odd parity error (even parity)

LABEL RECOGNITION

The user loads the 256-bit label look-up table to specify which 8-bit incoming ARINC labels are captured by the receiver, and which are discarded. Setting a “1” in the look-up table enables processing of received ARINC words containing the corresponding label. A “0” in the look-up table causes discard of received ARINC words containing the label. The 256-bit look-up table is loaded using SPI op codes 02 hex, 03 hex or 06 hex, as described in Table 1. After the look-up table is initialized, set Control Register bit CR2 to enable label recognition.

If label recognition is enabled, the receiver compares the label in each new ARINC word against the stored look-up table. If a label match is found, the received word is processed. If no match occurs, the new ARINC word is discarded and no indicators of received ARINC data are presented.

READING THE LABEL LOOK-UP TABLE

The contents of the Label Look-up table may be read via the SPI interface using instruction 0D hex as described in Table 1.

FUNCTIONAL DESCRIPTION (cont.)

TRANSMITTER

FIFO OPERATION

The Transmit FIFO is loaded with ARINC 429 words awaiting transmission. SPI op code 0E hex writes up to 32 ARINC words into the FIFO, starting at the next available FIFO location. If Status Register bit SR3 equals "1" (FIFO empty), then up to 32 words (32 bits each) may be loaded. If Status Register bit SR3 equals "0" then only the available positions may be loaded. If all 32 positions are full, Status Register bit SR5 is asserted. Further attempts to load the Transmit FIFO are ignored until at least one ARINC word is transmitted.

The Transmit FIFO half-full flag (Status Register bit SR4) equals "0" when the Transmit FIFO contains less than 16 words. When SR4 equals "0", the system microprocessor can safely initiate a 16-word ARINC block-write sequence.

In normal operation (Control Register bit CR3 = "1"), the 32nd bit transmitted is a word parity bit. Odd or even parity is selected by programming Control Register bit CR9 to a "0" or "1" respectively. If Control Register bit CR3 equals "0", all 32 bits loaded into the Transmit FIFO are treated as data and are transmitted.

SPI op code 11 hex asynchronously clears all data in the Transmit FIFO. The Transmit FIFO should be cleared after a self-test before starting normal operation to avoid inadvertent transmission of test data.

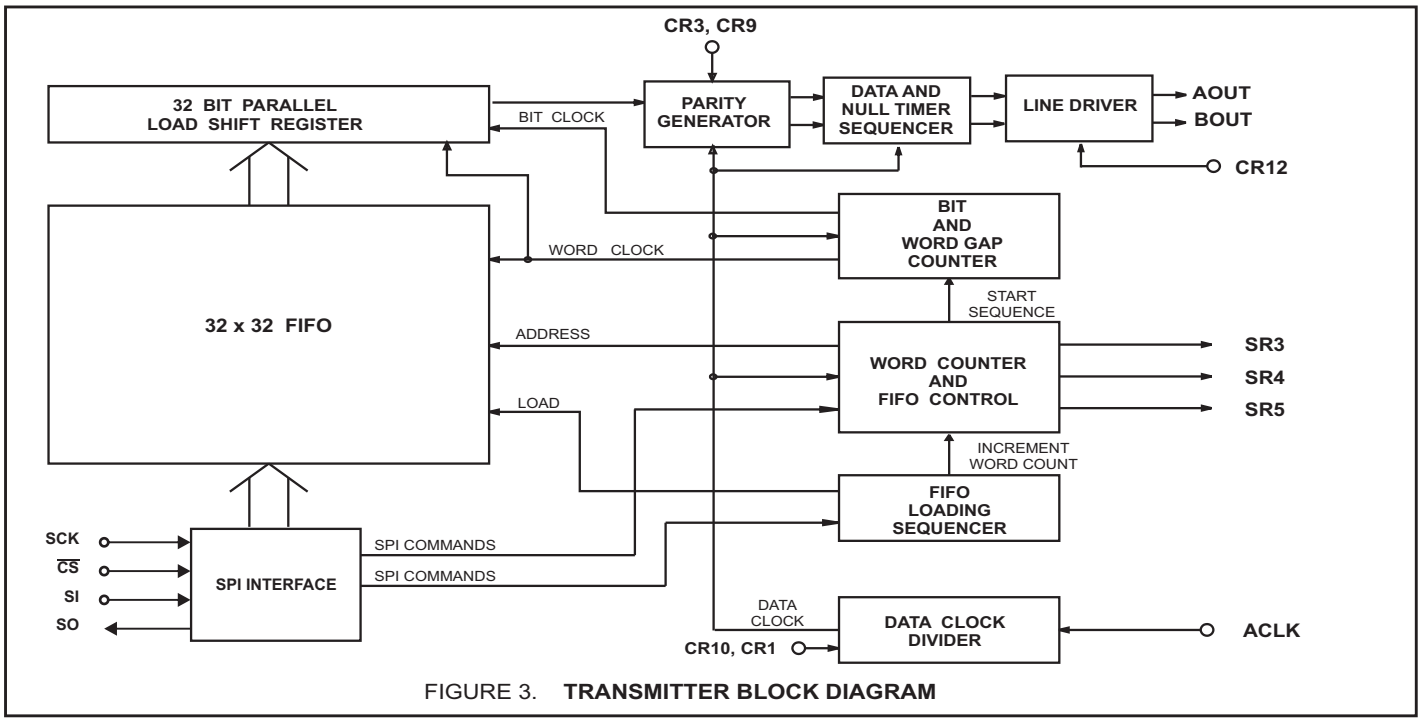
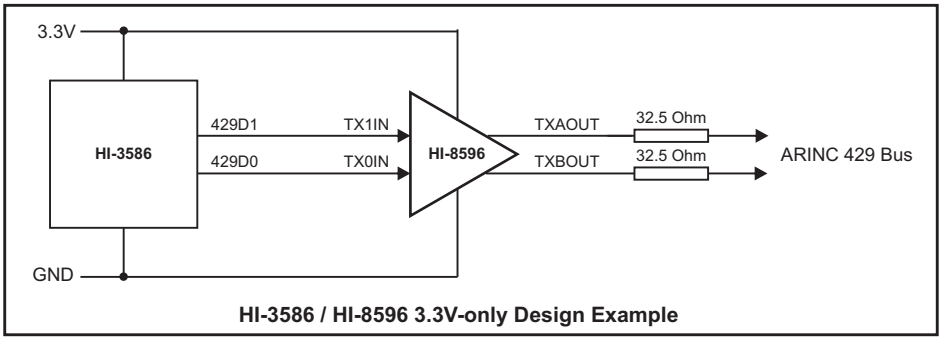


FIGURE 3. **TRANSMITTER BLOCK DIAGRAM**

HI-3586 OPTION

The HI-3586 is functionally identical to the HI-3585 except it does not include an on-chip ARINC 429 Line Driver. Instead, digital output pins 429D1 and 429D0 may be used to drive an external ARINC 429 line driver. This configuration is useful if the desiger wishes to take advantage of Holt's single supply rail line drivers, such as the 5V Hi-8592 or 3.3V HI-8596.



HI-3586 / HI-8596 3.3V-only Design Example

FUNCTIONAL DESCRIPTION (cont.)

DATA TRANSMISSION

If Control Register bit CR13 equals "1", ARINC 429 data is transmitted immediately following the $\overline{CS}$ rising edge of the SPI instruction that loaded data into the Transmit FIFO. Loading Control Register bit CR13 to "0" allows the software to control transmission timing; each time an SPI op code 12 hex is executed, all loaded Transmit FIFO words are transmitted. If new words are loaded into the Transmit FIFO before transmission stops, the new words will also be output. Once the Transmit FIFO is empty and transmission of the last word is complete, the FIFO can be loaded with new data which is held until the next SPI 12 hex instruction is executed. Once transmission is enabled, the FIFO positions are incremented with the top register loading into the data transmission shift register. Within 2.5 data clocks the first data bit appears at AOUT and BOUT. The 31 or 32 bits in the data transmission shift register are presented sequentially to the outputs in the ARINC 429 format with the following timing:

	HIGH SPEED	LOW SPEED
ARINC DATA BIT TIME	10 Clocks	80 Clocks
DATA BIT TIME	5 Clocks	40 Clocks
NULL BIT TIME	5 Clocks	40 Clocks
WORD GAP TIME	40 Clocks	320 Clocks

The word counter detects when all loaded positions have been transmitted and sets the transmitter ready flag, SR3, high.

TRANSMITTER PARITY

The parity generator counts the Ones in the 31-bit word. If control register bit CR9 is set to a "0", the 32nd bit transmitted will make parity odd. If the control bit is a "1", the parity is even. Setting CR3 to "0" bypasses the parity generator, and allows 32 bits of data to be transmitted.

SELF TEST

If Control Register bits CR5 and CR12 equal "0", the transmitter serial output data is internally looped-back into the receiver. Data passes unmodified from transmitter to receiver. Setting Control register bit CR12 to "1" forces AOUT and BOUT to the Null state regardless of CR5 state.

SYSTEM OPERATION

The receiver is independent of the transmitter. Therefore, control of data exchanges is strictly at the option of the user. The only restrictions are:

1. The received data will be overwritten if the Receive FIFO is full and at least one location is not retrieved before the next complete ARINC word is received.

2. The Transmit FIFO can store 32 words maximum and ignores attempts to load additional data when full.

LINE DRIVER OPERATION

The line driver in the HI-3585 directly drives the ARINC 429 bus. The two ARINC outputs (AOUT37 and BOUT37) provide a differential voltage to produce a +10V One, a -10V Zero, and a 0 Volt Null. Control Register bit CR10 controls both the transmitter data rate and the slope of the differential output signal. No additional hardware is required to control the slope.

Transmit timing is derived from a 1 MHZ reference clock. Control Register bit CR1 determines the reference clock source. If CR1 equals "0," a 50% duty cycle 1 MHZ clock should be applied to the ACLK input pin. If CR1 equals "1," the ACLK input is divided to generate the 1 MHZ ARINC clock. SPI op code 07 hex provides the HI-3585 with the correct division ratio to generate a 1 MHZ reference from ACLK.

Loading Control Register bit CR10 to "0" causes a 100 Kbit/s data rate and a slope of 1.5 µs on the ARINC outputs. Loading CR10 to "1" causes a 12.5 Kbit/s data rate and a slope of 10 µs. Timing is set by an on-chip resistor and capacitor and tested to be within ARINC 429 requirements.

LINE DRIVER OUTPUT PINS

The HI-3585 AOUT37 and BOUT37 pins have 37.5 Ohms in series with each line driver output, and may be directly connected to an ARINC 429 bus. The alternate AOUT27 and BOUT27 pins have 27 ohms of internal series resistance and require external 10 ohm resistors at each pin. AOUT27 and BOUT27 are for applications where external series resistance is applied, typically for lightning protection devices.

LINE RECEIVER INPUT PINS

The HI-3585 has two sets of Line Receiver input pins, RINA/B and RINA/B-40. Only one pair may be used to connect to the ARINC 429 bus. The unused pair must be left floating. The RINA/B pins may be connected directly to the ARINC 429 bus. The RINA/B-40 pins require external 40K ohm resistors in series with each ARINC input. These do not affect the ARINC receiver thresholds. By keeping excessive voltage outside the device, this option is helpful in applications where lightning protection is required.

When using the RINA/B-40 pins, each side of the ARINC bus must be connected through a 40K ohm series resistor in order for the chip to detect the correct ARINC levels. The typical 10 Volt differential signal is translated and input to a window comparator and latch. The comparator levels are set so that with the external 40K ohm resistors, they are just below the standard 6.5 volt minimum ARINC data threshold and just above the standard 2.5 volt maximum ARINC null threshold.

Please refer to the Holt AN-300 Application Note for additional information and recommendations on lightning protection of Holt line drivers and line receivers.

POWER SUPPLY SEQUENCING

Power supply sequencing should be controlled to prevent large currents during supply turn-on and turn-off. The recommended sequence is V+ followed by V_{DD}, always ensuring that V+ is the most positive supply. The V- supply is not critical and can be applied at any time.

MASTER RESET (MR)

Application of a Master Reset causes immediate termination of data transmission and data reception. The transmit and receive FIFOs are cleared. Status Register FIFO flags and FIFO status output signals RFLAG and TFLAG are also cleared. The Control Register is not affected by a Master Reset.

SERIAL PERIPHERAL INTERFACE

SERIAL PERIPHERAL INTERFACE (SPI) BASICS

The HI-3585 uses an SPI synchronous serial interface for host access to internal registers and data FIFOs. Host serial communication is enabled through the Chip Select ($\overline{CS}$) pin, and is accessed via a three-wire interface consisting of Serial Data Input (SI) from the host, Serial Data Output (SO) to the host and Serial Clock (SCK). All read / write cycles are completely self-timed.

The SPI (Serial Peripheral Interface) protocol specifies master and slave operation; the HI-3585 operates as an SPI slave.

The SPI protocol defines two parameters, CPOL (clock polarity) and CPHA (clock phase). The possible CPOL-CPHA combinations define four possible "SPI Modes". Without describing details of the SPI modes, the HI-3585 operates in mode 0 where input data for each device (master and slave) is clocked on the rising edge of SCK, and output data for each device changes on the falling edge (CPHA = 0, CPOL = 0). Be sure to set the host SPI logic for mode 0.

As seen in Figure 4, SPI Mode 0 holds SCK in the low state when idle. The SPI protocol transfers serial data as 8-bit bytes. Once $\overline{CS}$ chip select is asserted, the next 8 rising edges on SCK latch input data into the master and slave devices, starting with each byte's most-significant bit.

Multiple bytes may be transferred when the host holds $\overline{CS}$ low after the first byte transferred, and continues to clock SCK in multiples of 8 clocks. A rising edge on $\overline{CS}$ chip select terminates the serial transfer and reinitializes the HI-3585 SPI for the next transfer. If $\overline{CS}$ goes high before a full byte is clocked by SCK, the incomplete byte clocked into the device SI pin is discarded.

In the general case, both master and slave simultaneously send and receive serial data (full duplex), per Figure 4 below. However the HI-3585 operates half duplex, maintaining high impedance on the SO output, except when actually transmitting serial data. When the HI-3110 is sending data on SO during read operations, activity on its SI input is ignored. Figures 5 and 6 show actual behavior for the HI-3585 SO output.

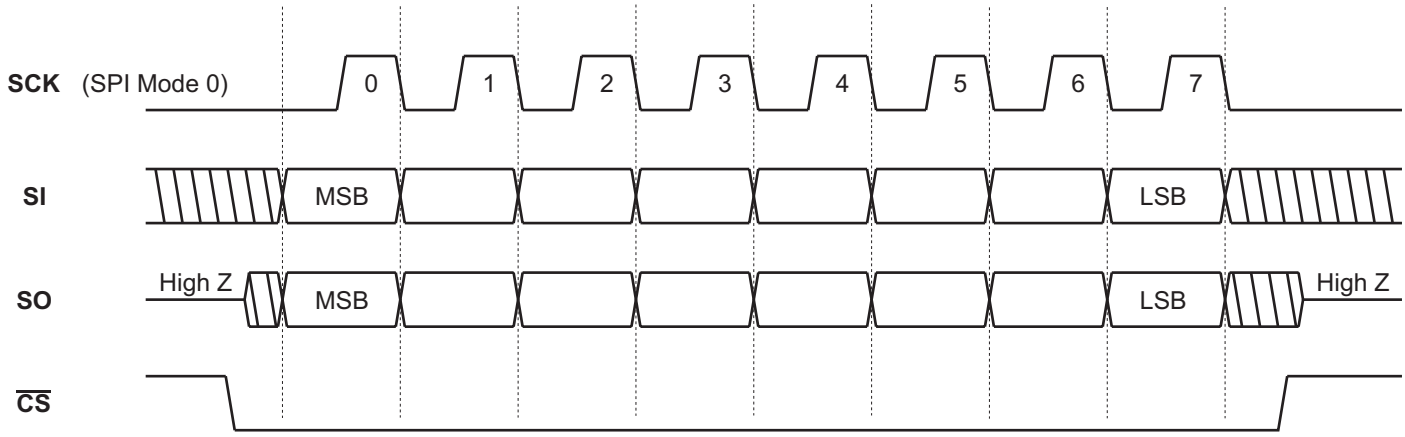


Figure 4. Generalized Single-Byte Transfer Using SPI Protocol Mode 0

HOST SERIAL PERIPHERAL INTERFACE (cont.)

HI-3585 SPI COMMANDS

For the HI-3585, each SPI read or write operation begins with an 8-bit command byte transferred from the host to the device after assertion of $\overline{CS}$. Since HI-3585 command byte reception is half-duplex, the host discards the dummy byte it receives while serially transmitting the command byte.

Figures 5 and 6 show read and write timing as it appears for a single-byte and dual-byte register operation. The command byte is immediately followed by a data byte comprising the 8-bit data word read or written. For a single register read or write, $\overline{CS}$ is negated after the data byte is transferred.

Multiple byte read or write cycles may be performed by transferring more than one byte before $\overline{CS}$ is negated. Table 1 defines the required number of bytes for each instruction.

Note: SPI Instruction op-codes not shown in Tables 1 are "reserved" and must not be used. Further, these op-codes will not provide meaningful data in response to read commands.

Two instruction bytes cannot be "chained"; $\overline{CS}$ must be negated after the command, then reasserted for the following Read or Write command.

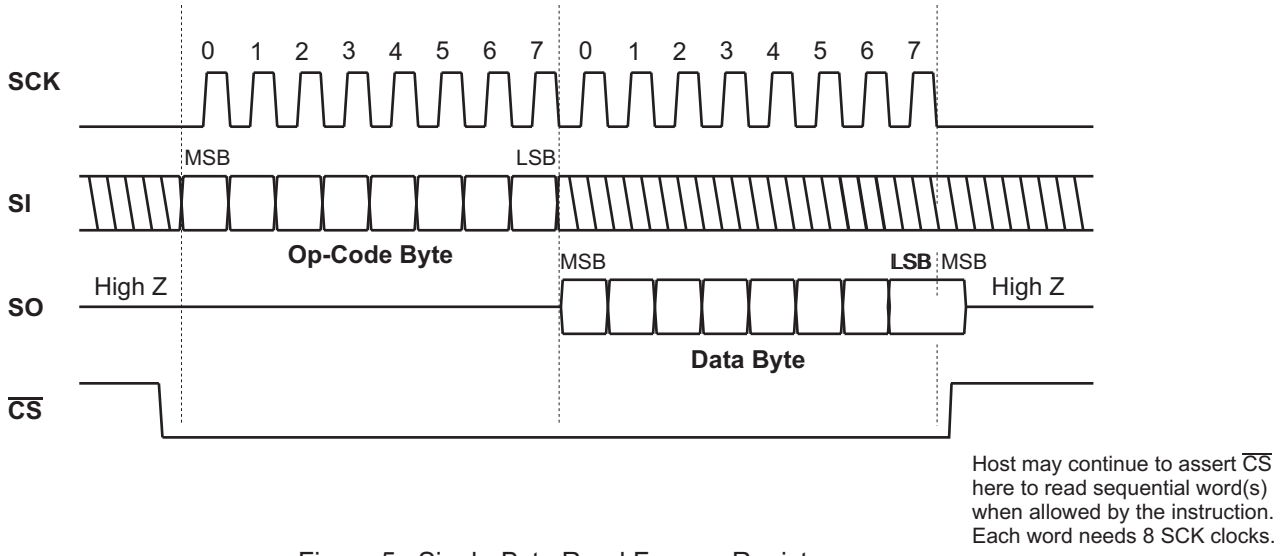


Figure 5. Single-Byte Read From a Register

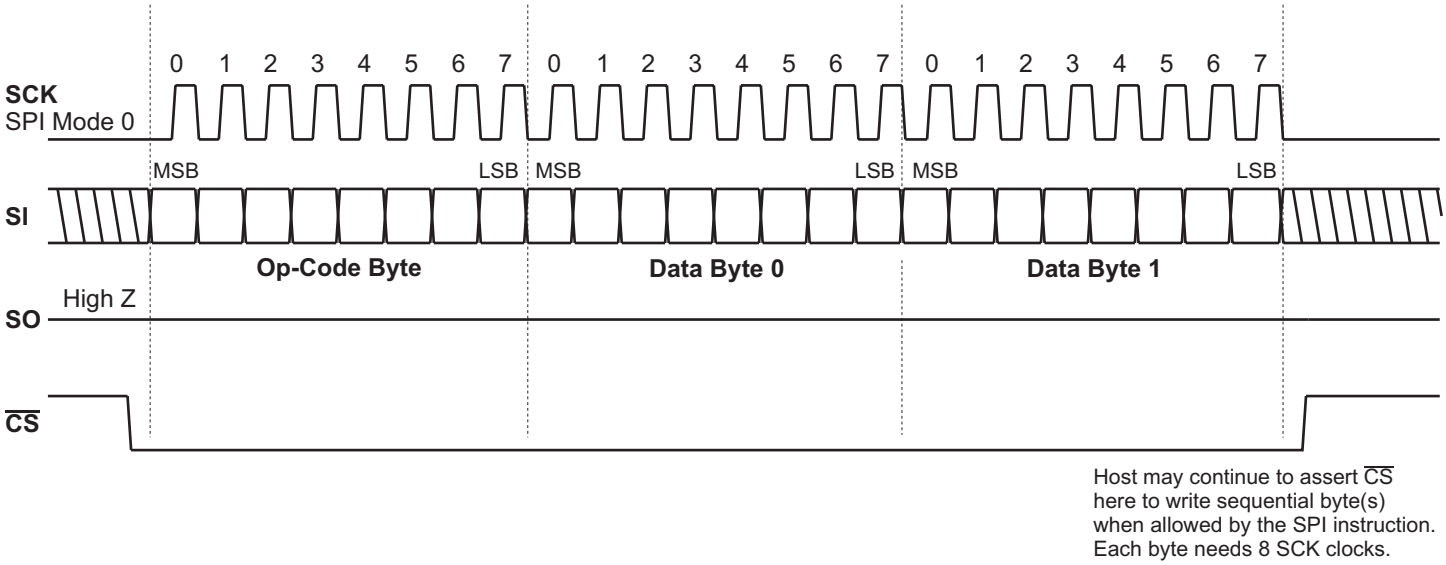
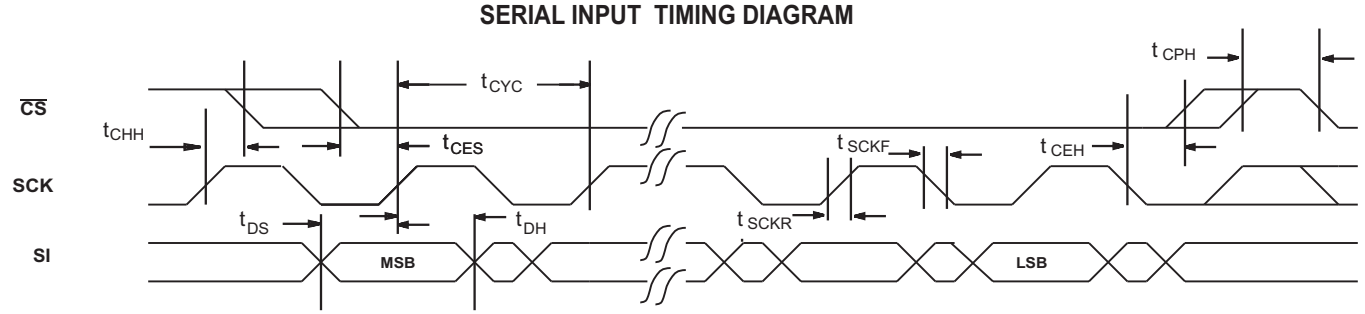


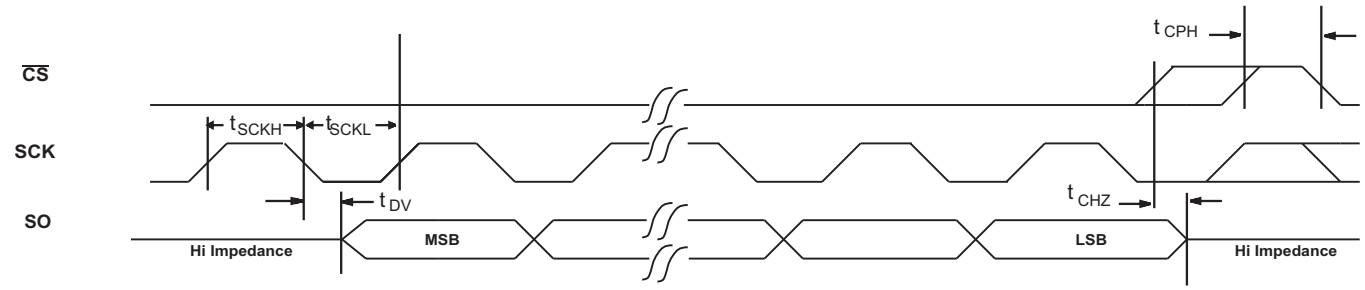
Figure 6. 2-Byte Write example

TIMING DIAGRAMS

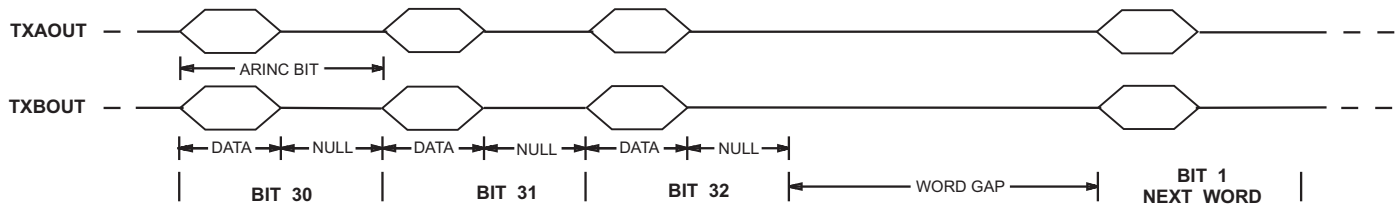
SERIAL INPUT TIMING DIAGRAM



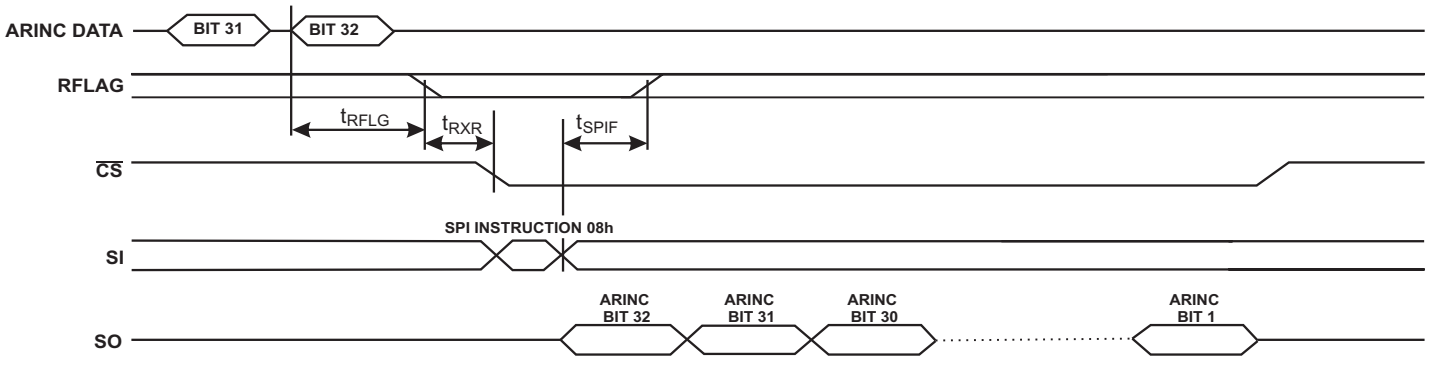
SERIAL OUTPUT TIMING DIAGRAM



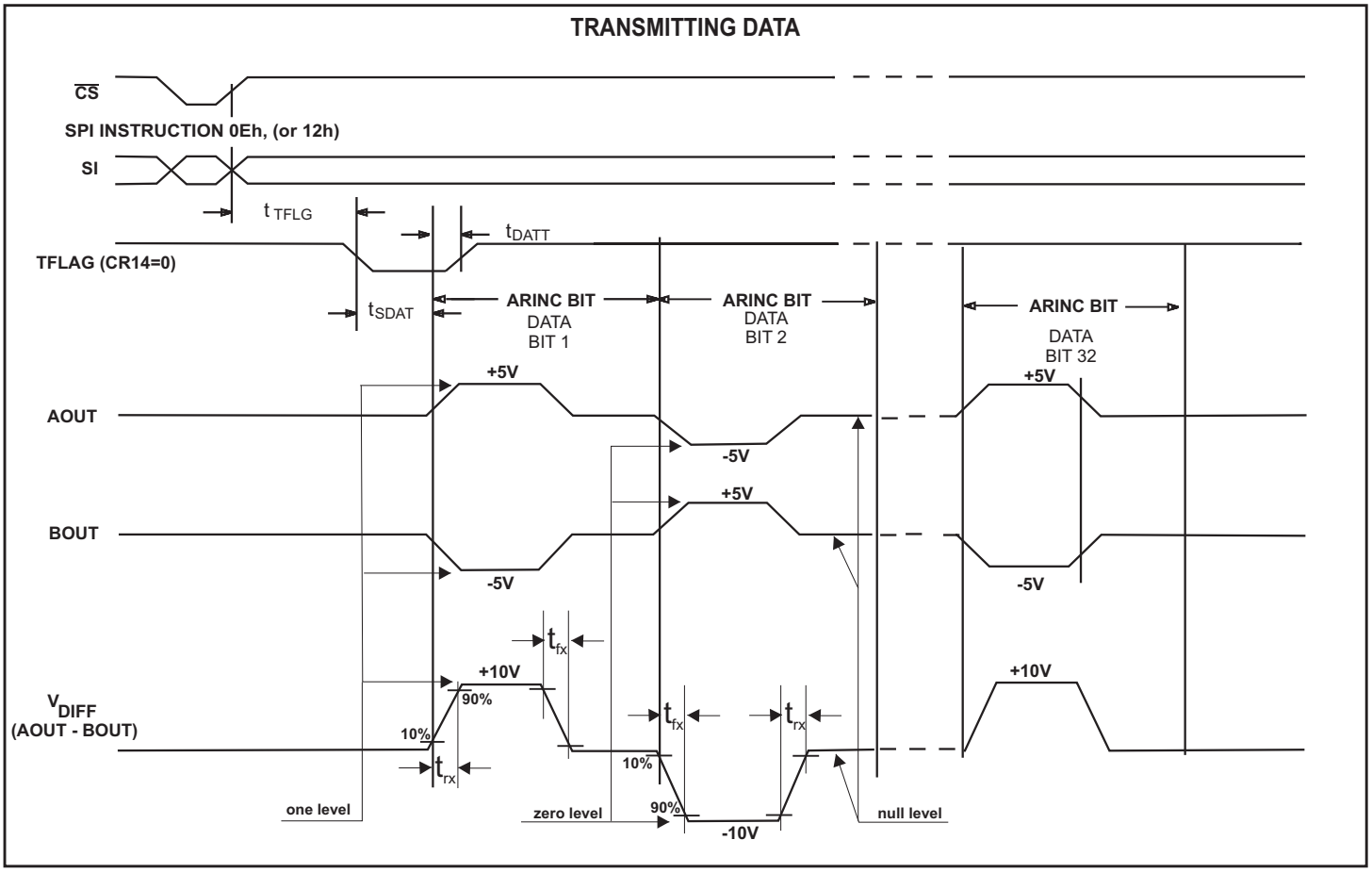
DATA RATE - EXAMPLE PATTERN



RECEIVER OPERATION



TIMING DIAGRAMS (cont.)



ABSOLUTE MAXIMUM RATINGS

Supply Voltages V_{DD} ..... -0.3V to +7.0V V+ ..... +7.0V V- ..... -7.0V	Power Dissipation at 25°C Plastic Quad Flat Pack .....1.5 W, derate 10mW/°C
Voltage at pins RINA, RINB ..... -120V to +120V	DC Current Drain per pin ..... ±10mA
Voltage at ARINC pins AOUT, BOUT ... (V-) – 0.3V to (V+) + 0.3V	Storage Temperature Range ..... -65°C to +150°C
Voltage at any other pin ..... -0.3V to V_{DD} +0.3V	Operating Temperature Range (Industrial): ..... -40°C to +85°C (Hi-Temp): ..... -55°C to +125°C
Solder temperature (Reflow) ..... 260°C	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V or 5.0V , V+ = +5V, V- = -5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

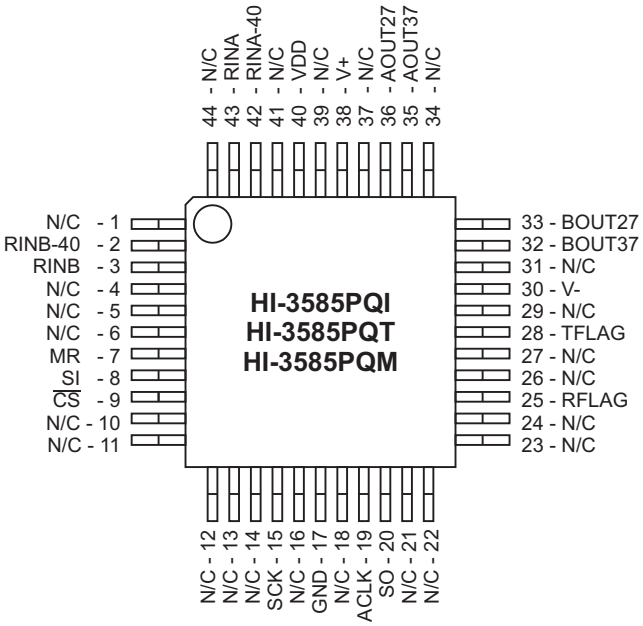
PARAMETER		SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
ARINC INPUTS - Pins RINA, RINB, RINA-40 (with external 40KOhms), RINB-40 (with external 40KOhms)							
Differential Input Voltage: (RINA to RINB)	ONE ZERO NULL	V_{IH} V_{IL} V_{NUL}	Common mode voltages less than ±30V with respect to GND	6.5 -13.0 -2.5	10.0 -10.0 0	13.0 -6.5 2.5	V V V
Input Resistance:	Differential To GND To V_{DD}	R_I R_G R_H		- - -	140 140 100	- - -	KΩ KΩ KΩ
Input Current:	Input Sink Input Source	I_{IH} I_{IL}		 -450		200	µA µA
Input Capacitance: (Guaranteed but not tested)	Differential To GND To V_{DD}	C_I C_G C_H	(RINA to RINB)			20 20 20	pF pF pF
LOGIC INPUTS							
Input Voltage:	Input Voltage HI Input Voltage LO	V_{IH} V_{IL}		80% VDD		 20% VDD	V V
Input Current:	Input Sink Input Source Pull-down Current (MR, SI, SCK, ACLK pins) Pull-up current (CS pin)	I_{IH} I_{IL} I_{PD} I_{PU}		 -1.5 250 -600		1.5 600 -300	µA µA µA µA
ARINC OUTPUTS - Pins AOUT37, BOUT37, (or AOUT27, BOUT27 with external 10 Ohms)							
ARINC output voltage (Ref. To GND)	One or zero Null	V_{DOUT} V_{NOUT}	No load and magnitude at pin,	4.50 -0.25	5.00	5.50 0.25	V V
ARINC output voltage (Differential)	One or zero Null	V_{DDIF} V_{NDIF}	No load and magnitude at pin,	9.0 -0.5	10.0	11.0 0.5	V V
ARINC output current		I_{OUT}	Momentary current	80			mA
LOGIC OUTPUTS							
Output Voltage:	Logic "1" Output Voltage Logic "0" Output Voltage	V_{OH} V_{OL}	I_{OH} = -100µA I_{OL} = 1.0mA	90%VDD		 10% VDD	V V
Output Current:	Output Sink Output Source	I_{OL} I_{OH}	V_{OUT} = 0.4V V_{OUT} = V_{DD} - 0.4V	1.6		 -1.0	mA mA
Output Capacitance:		C_O			15		pF
Operating Voltage Range							
		VDD		3.15		5.25	V
		V+		4.75		5.5	V
		V-		-4.75		-5.5	V
Operating Supply Current							
VDD		I_{DD1}			2.5	7	mA
V+		I_{DD2}			4	14	mA
V-		I_{EE1}			4	12	mA

AC ELECTRICAL CHARACTERISTICS

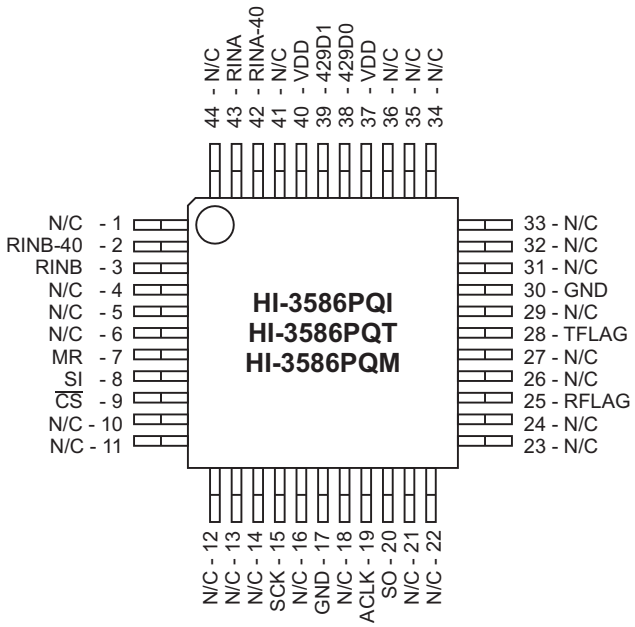
VDD = 3.3V or 5.0V, V+=+5V, V-=-5V, GND = 0V, TA = Operating Temperature Range and fclk=1MHz ±0.1% with 50/50 duty cycle

PARAMETER		SYMBOL	LIMITS			UNITS
			MIN	TYP	MAX	
SPI INTERFACE TIMING - 5.0V						
SCK clock period		t_{CYC}	250			ns
$\overline{CS}$ active after last SCK rising edge		t_{CHH}	10			ns
$\overline{CS}$ setup time to first SCK rising edge		t_{CES}	10			ns
$\overline{CS}$ hold time after last SCK falling edge		t_{CEH}	40			ns
$\overline{CS}$ inactive between SPI instructions		t_{CPH}	20			ns
SPI SI Data set-up time to SCK rising edge		t_{DS}	25			ns
SPI SI Data hold time after SCK rising edge		t_{DH}	15			ns
SCK rise time		t_{SCKR}			10	ns
SCK fall ime		t_{SCKF}			10	ns
SO valid after SCK falling edge		t_{DV}			125	ns
SO high-impedance after $\overline{CS}$ inactive		t_{CHZ}			100	ns
Master Reset pulse width		t_{MR}	150			ns
SPI INTERFACE TIMING - 3.3V						
SCK clock period		t_{CYC}	390			ns
$\overline{CS}$ active after last SCK rising edge		t_{CHH}	10			ns
$\overline{CS}$ setup time to first SCK rising edge		t_{CES}	10			ns
$\overline{CS}$ hold time after last SCK falling edge		t_{CEH}	40			ns
$\overline{CS}$ inactive between SPI instructions		t_{CPH}	35			ns
SPI SI Data set-up time to SCK rising edge		t_{DS}	30			ns
SPI SI Data hold time after SCK rising edge		t_{DH}	30			ns
SCK rise time		t_{SCKR}			10	ns
SCK fall ime		t_{SCKF}			10	ns
SO valid after SCK falling edge		t_{DV}			195	ns
SO high-impedance after $\overline{CS}$ inactive		t_{CHZ}			100	ns
Master Reset pulse width		t_{MR}	150			ns
RECEIVER TIMING						
Delay - Last bit of received ARINC word to RFLAG(Full or Empty) - Hi Speed		t_{RFLG}			16	µs
Delay - Last bit of received ARINC word to RFLAG(Full or Empty) - Lo Speed		t_{RFLG}			126	µs
Received data available to SPI interface. RFLAG to $\overline{CS}$ active		t_{RXR}	0			ns
SPI receiver read or clear FIFO instruction to RFLAG		t_{SPIF}			155	ns
TRANSMITTER TIMING						
SPI transmit data write or FIFO clear instruction to TFLAG (Empty or Full)		t_{TFLG}			120	ns
SPI instruction to ARINC 429 data output - Hi Speed		t_{SDAT}			17	µs
SPI instruction to ARINC 429 data output - Lo Speed		t_{SDAT}			118	µs
Delay TFLAG high after enable transmit - Hi Speed		t_{DATT}			14	µs
Delay TFLAG high after enable transmit - Lo Speed		t_{DATT}			114	µs
Line driver transition differential times:						
(High Speed, control register CR10 = Logic 0)	high to low	t_{fx}	1.0	1.5	2.0	µs
	low to high	t_{rx}	1.0	1.5	2.0	µs
(Low Speed, control register CR10 = Logic 1)	high to low	t_{fx}	5.0	10	15	µs
	low to high	t_{rx}	5.0	10	15	µs

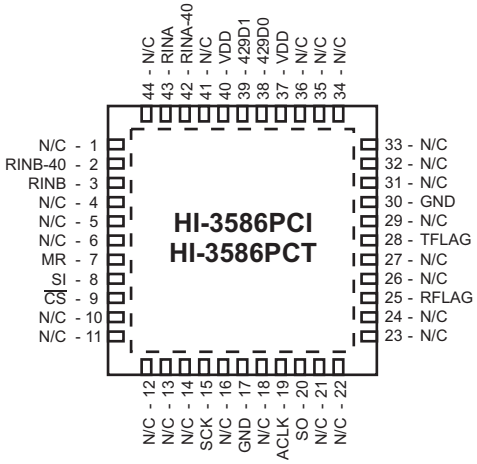
ADDITIONAL HI-3585 & HI-3586 PIN CONFIGURATIONS (Top View)



44 - Pin Plastic Quad Flat Pack (PQFP)



44 - Pin Plastic Quad Flat Pack (PQFP)



44 - Pin Plastic 7mm x 7mm Chip-Scale Package (QFN)

ORDERING INFORMATION

HI - 358x PQ x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
PQ	44 PIN PLASTIC QUAD FLAT PACK, PQFP (44PMQS)

PART NUMBER	PACKAGE DESCRIPTION
3585	On-chip ARINC 429 Line Driver
3586	External ARINC 429 Line Driver

HI - 358x PC x x

PART NUMBER	LEAD FINISH
Blank	NiPdAu
F	NiPdAu (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION
PC	44 PIN PLASTIC CHIP-SCALE, QFN (44PCS)

PART NUMBER	PACKAGE DESCRIPTION
3585	On-chip ARINC 429 Line Driver
3586	External ARINC 429 Line Driver

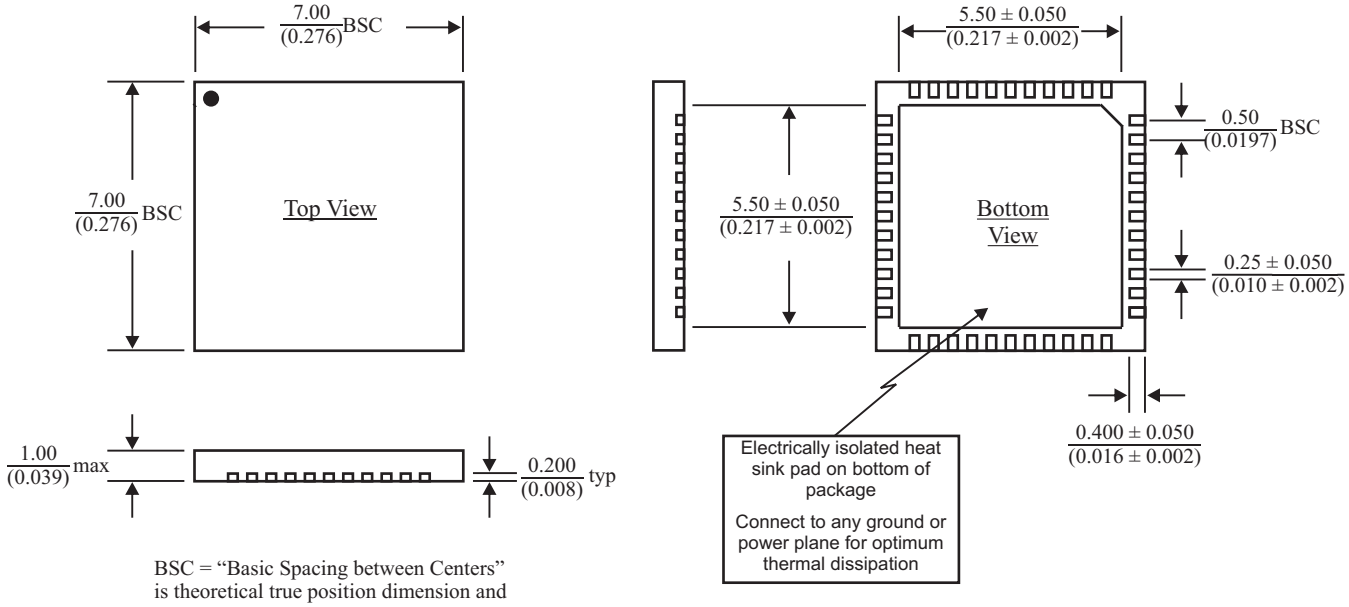
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS3585	NEW	05/08/08	Initial Release
	A	10/10/08	Revised AC Electrical Characteristics table and description of “T” process.
	B	05/22/09	Clarified relationship between SPI bit order and the ARINC 429 bit order.
	C	02/03/10	Clarified op code 09 hex description.
	D	04/20/10	Removed op code 09 hex.
	E	05/19/10	Corrected ARINC receiver nomenclature.
	F	09/03/10	Added HI-3586 digital-only product option
	G	11/02/10	Enhanced description of HI-3586 digital-only product option, added basics of SPI communications and added M flow for QFP package.
	H	06/04/12	Clarified the description of receiver parity. Updated PQFP package drawing. Corrected typo in clock source tolerance on p. 5 from 0.1% to 1%.
	I	07/02/12	Update SPI Interface Timing at 5.0V and 3.3V
	J	07/25/13	Update QFN package drawing. Remove note on heat sink connection for QFN package.
	K	06/23/14	Update solder reflow temperature. Correct typo in ordering information. Update package drawings.
	L	07/18/14	Clarify absolute maximum voltage at ARINC bus pins AOUT, BOUT.
	M	10/23/15	Update SPI Output timing diagram. Update AC Characteristics for tCHZ.
	N	11/11/15	Update AC Characteristics for tCHZ parameter at 3.3V.
	O	12/07/17	Add note to Status Register section to clarify when to read FIFO data.
	P	09/03/2020	Update QFN package lead finish to NiPdAu.

44-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 44PCS

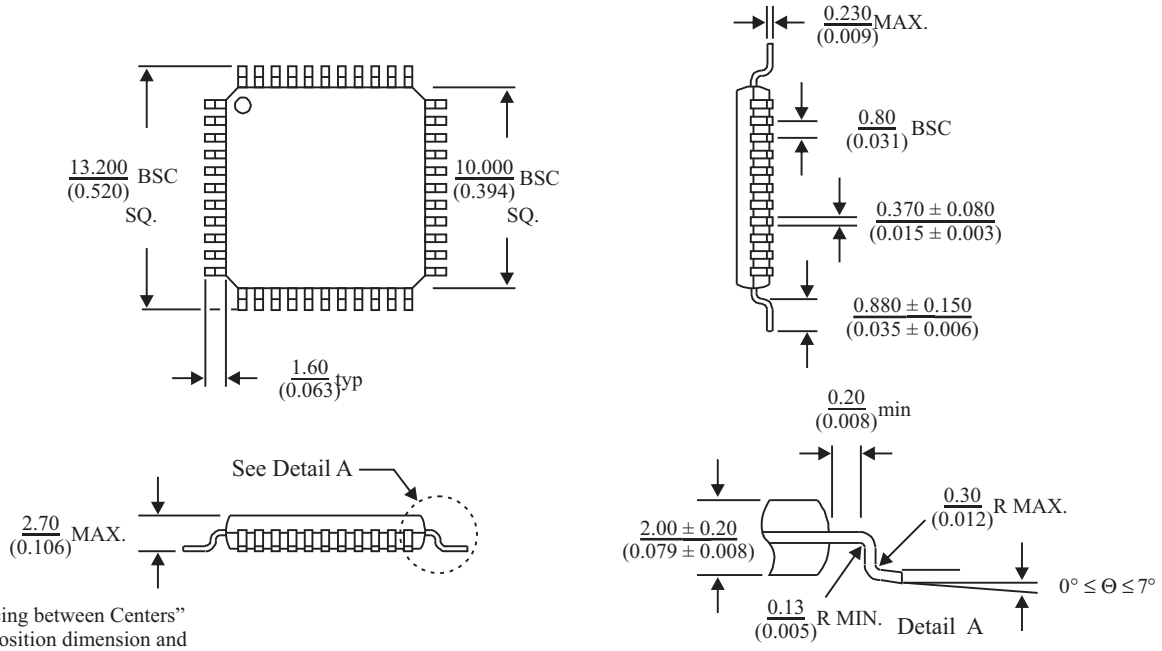


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 44PMQS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)