March 2015

FDD86102

N-Channel Shielded Gate PowerTrench® MOSFET

100 V, 36 A, 24 mΩ

Features

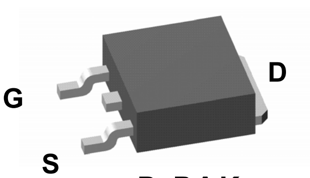
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 24 mΩ at V_{GS} = 10 V, I_D = 8 A
- Max $r_{DS(on)}$ = 38 mΩ at V_{GS} = 6 V, I_D = 6 A
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Very low Qg and Qgd compared to competing trench technologies
- Fast switching speed
- 100% UIL tested
- RoHS Compliant

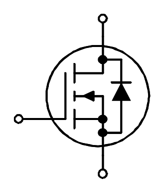
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Application

- DC - DC Conversion





MOSFET Maximum Ratings T_C = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C		36	A
	-Continuous	T_A = 25 °C	(Note 1a)	8	
	-Pulsed		(Note 4)	75	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	121	mJ
P_D	Power Dissipation	T_C = 25 °C		62	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	3.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		2.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD86102	FDD86102	D-PAK(TO-252)	13 ”	16 mm	2500 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		67		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA

On Characteristics (Note 2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	3.1	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-8.5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 8 A		19	24	mΩ
		V_{GS} = 6 V, I_D = 6 A		26	38	
		V_{GS} = 10 V, I_D = 8 A, T_J = 125 °C		33	44	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 8 A		21		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		780	1035	pF
C_{oss}	Output Capacitance			180	240	pF
C_{rss}	Reverse Transfer Capacitance			15	25	pF
R_g	Gate Resistance			0.4		Ω

Switching Characteristics

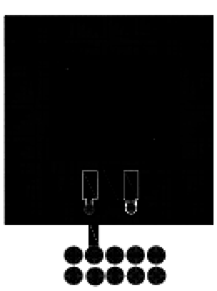
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 8 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		7.6	15	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			13.4	24	ns
t_f	Fall Time			2.9	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 8 A		13.4	19	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 5 V; V_{DD} = 50 V, I_D = 8 A		7.6	11	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 50 V, I_D = 8 A		4.0		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.7		nC

Drain-Source Diode Characteristics

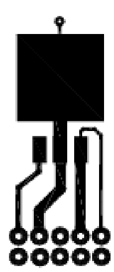
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 8 A (Note 2)		0.8	1.3	V
		V_{GS} = 0 V, I_S = 2.6 A (Note 2)		0.7	1.2	
t_{rr}	Reverse Recovery Time	I_F = 8 A, di/dt = 100 A/μs		43	68	ns
Q_{rr}	Reverse Recovery Charge			43	68	nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 40 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 96 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} 121 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 9 A, V_{DD} = 100 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 30 A.
4. Pulsed Drain current is tested at 300 μs with 2% duty cycle. For repetitive pulses, the pulse width is limited by the maximum junction temperature.

Typical Characteristics T_J = 25 °C unless otherwise noted

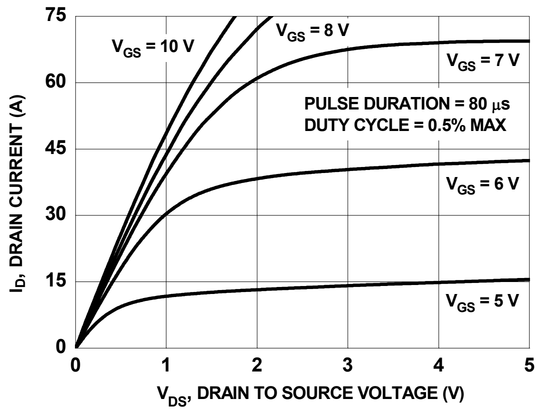


Figure 1. On-Region Characteristics

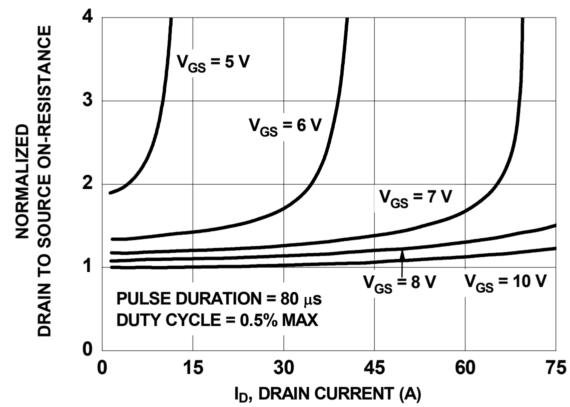


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

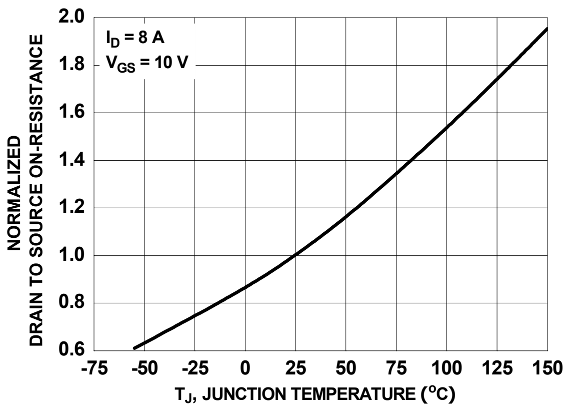


Figure 3. Normalized On-Resistance vs Junction Temperature

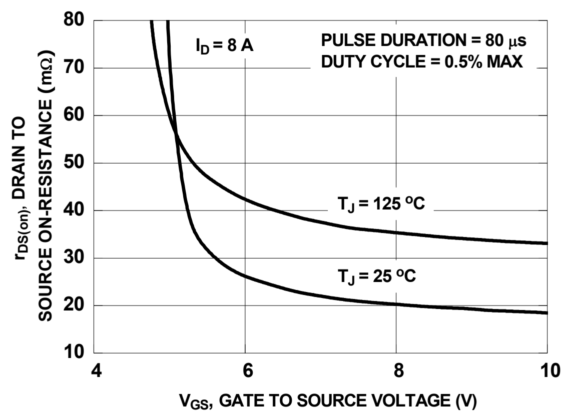


Figure 4. On-Resistance vs Gate to Source Voltage

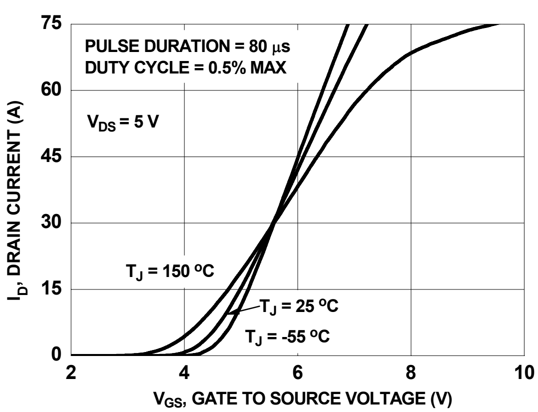


Figure 5. Transfer Characteristics

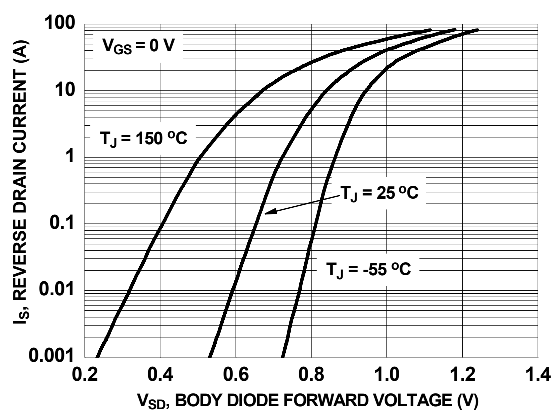


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

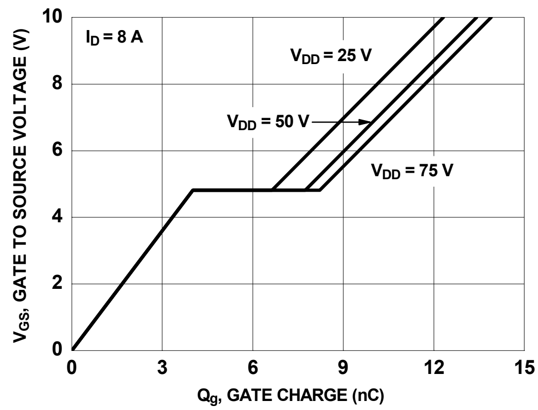


Figure 7. Gate Charge Characteristics

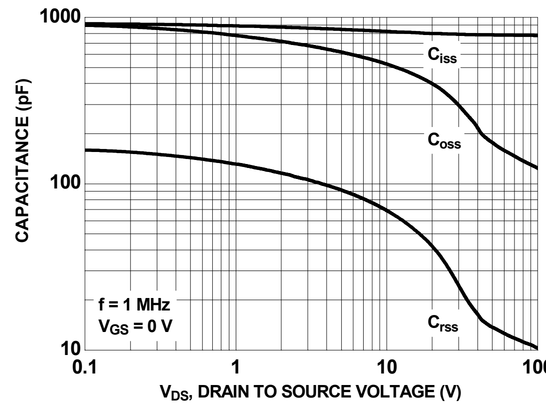


Figure 8. Capacitance vs Drain to Source Voltage

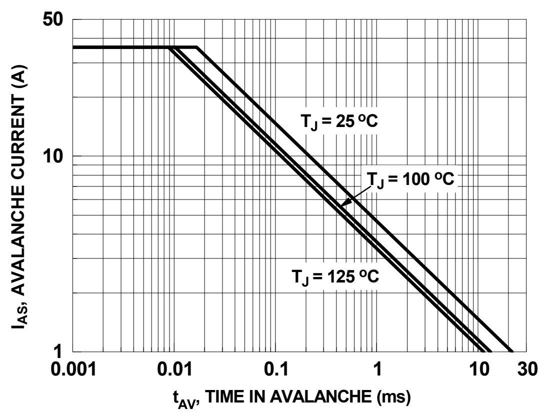


Figure 9. Unclamped Inductive Switching Capability

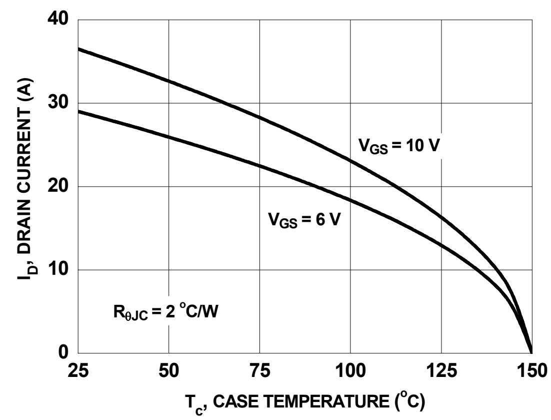


Figure 10. Maximum Continuous Drain Current vs Case Temperature

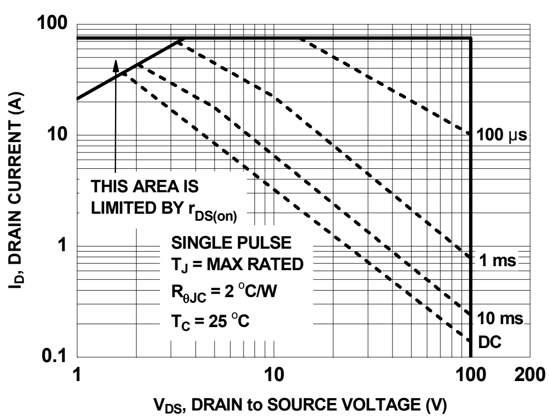


Figure 11. Forward Bias Safe Operating Area

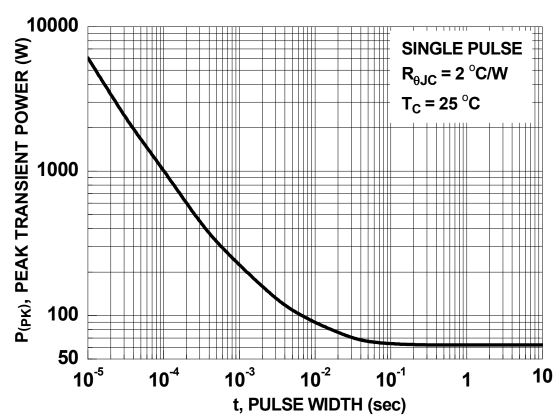


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

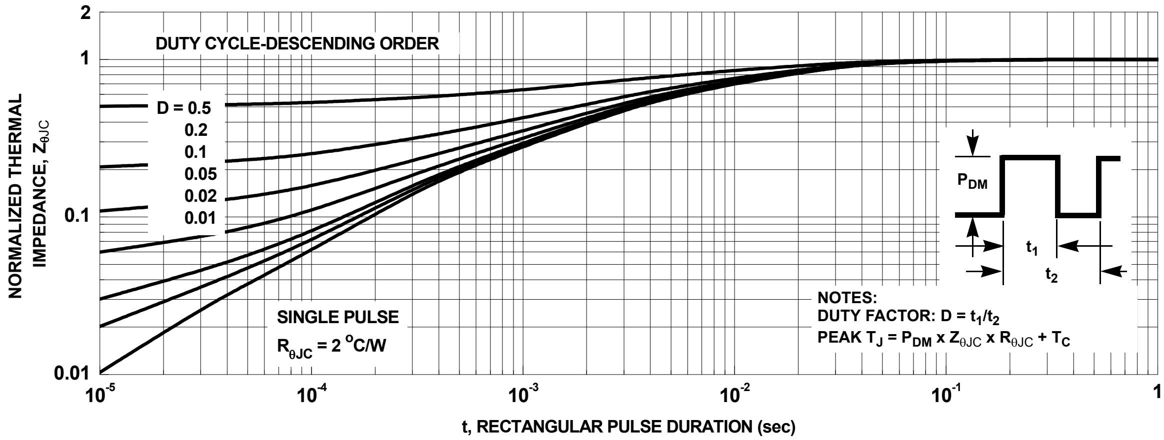
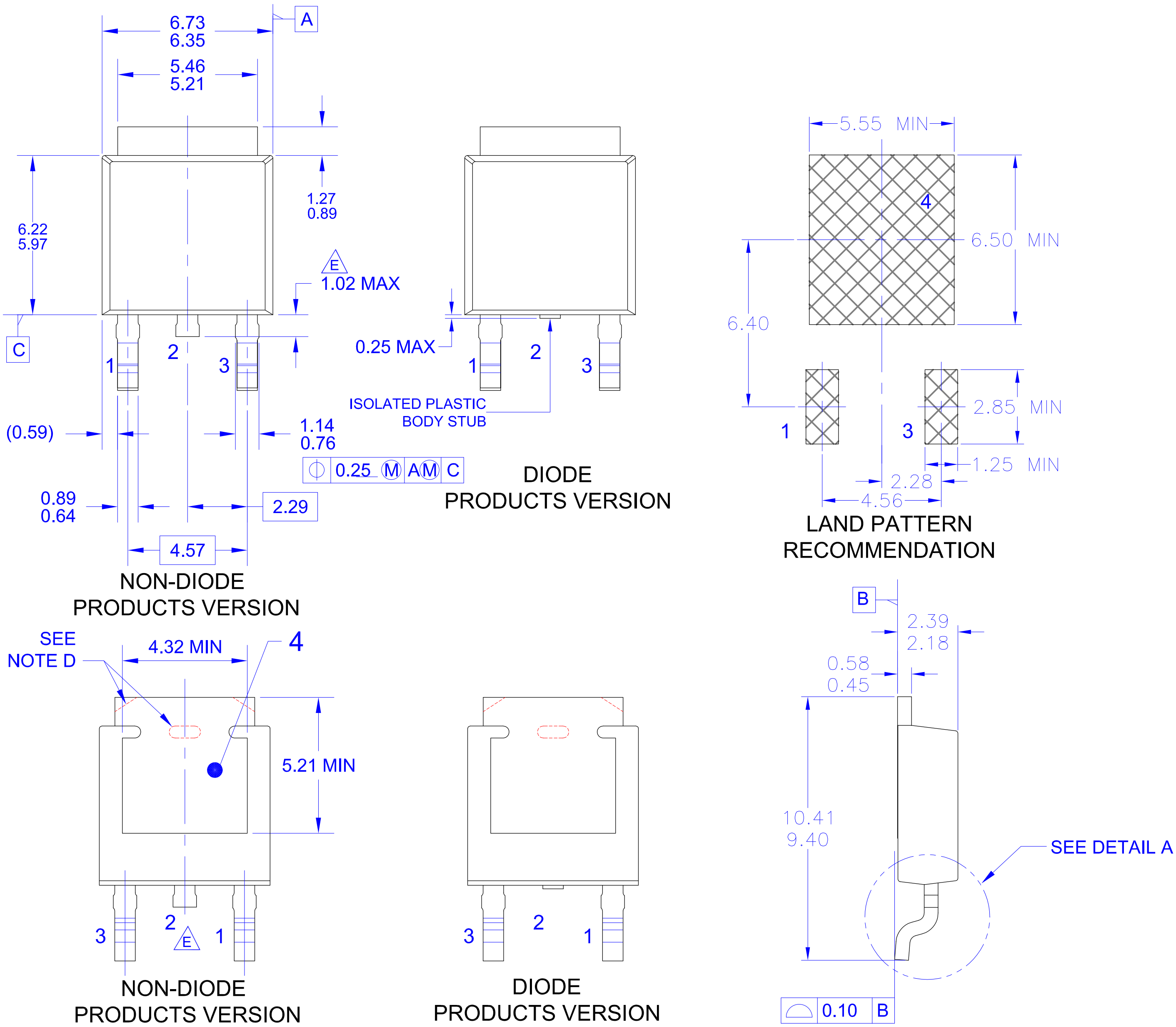
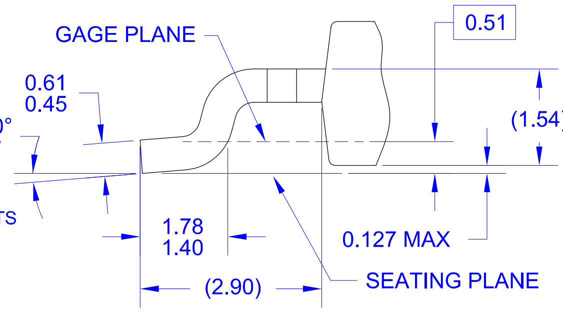


Figure 13. Junction-to-Case Transient Thermal Response Curve



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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