ON Semiconductor®

FDC654P

Single P-Channel Logic Level PowerTrench$^{\delta}$ MOSFET

General Description

This P-Channel Logic Level MOSFET is produced using ON Semiconductor's advanced PowerTrench process. It has been optimized for battery power management applications.

Applications

- Battery management
- Load switch
- Battery protection

Features

- −3.6 A, −30 V. $R_{DS(ON)} = 75\ m\Omega$ @ $V_{GS} = −10\ V$
  $R_{DS(ON)} = 125\ m\Omega$ @ $V_{GS} = −4.5\ V$

- Low gate charge (6.2 nC typical)

- High performance trench technology for extremely low $R_{DS(ON)}$

SuperSOT ™-6
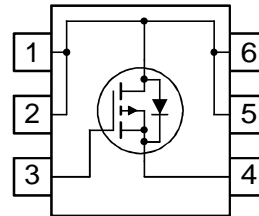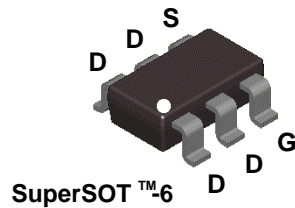
Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		−30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1a)	−3.6	A
	– Pulsed		−10	
P_D	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.654	FDC654P	7"	8mm	3000 units

Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = -250$ µA	−30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250$ µA, Referenced to 25°C		−22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24$ V, $V_{GS} = 0$ V			−1	µA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = 20$ V, $V_{DS} = 0$ V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -20$ V, $V_{DS} = 0$ V			−100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250$ µA	−1	−1.9	−3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250$ µA, Referenced to 25°C		4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10$ V, $I_D = -3.6$ A $V_{GS} = -4.5$ V, $I_D = -2.7$ A $V_{GS} = -10$ V, $I_D = -3.6$A, $T_J=125°C$		63 100 90	75 125 115	mΩ
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -4.5$ V, $V_{DS} = -5$ V	−5			A
g_{FS}	Forward Transconductance	$V_{DS} = -5$ V, $I_D = -3.6$ A		6		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -15$ V, $V_{GS} = 0$ V, f = 1.0 MHz		298		pF
C_{oss}	Output Capacitance			83		pF
C_{rss}	Reverse Transfer Capacitance			39		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -15$ V, $I_D = -1$ A, $V_{GS} = -10$ V, $R_{GEN} = 6$ Ω		6	12	ns
t_r	Turn–On Rise Time			13	23	ns
$t_{d(off)}$	Turn–Off Delay Time			11	20	ns
t_f	Turn–Off Fall Time			6	12	ns
Q_g	Total Gate Charge	$V_{DS} = -15$ V, $I_D = -3.6$ A, $V_{GS} = -10$ V		6.2	9	nC
Q_{gs}	Gate–Source Charge			1		nC
Q_{gd}	Gate–Drain Charge			1.2		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				−1.3	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = -1.3$ A (Note 2)		−0.8	−1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
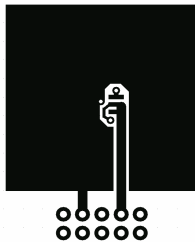
a) 78°C/W when mounted on a 1in^2 pad of 2 oz copper

b) 156°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%
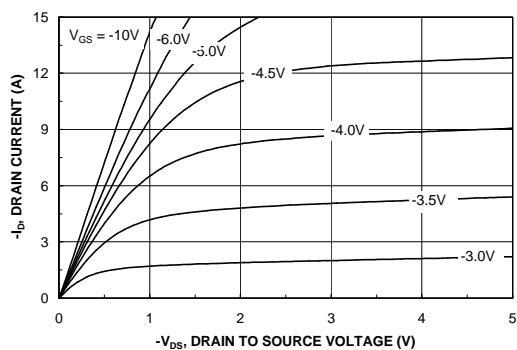
Typical Characteristics

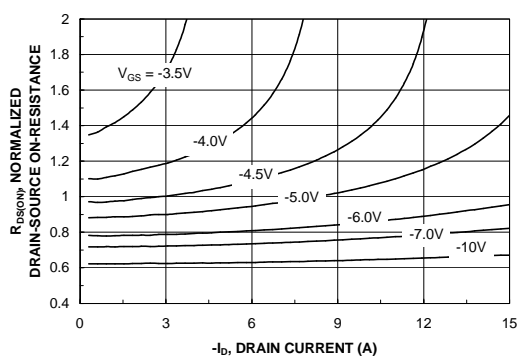Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with
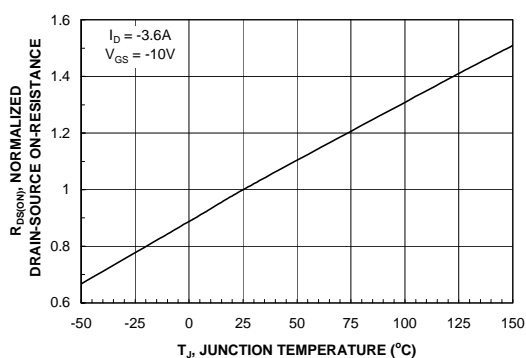Drain Current and Gate Voltage.

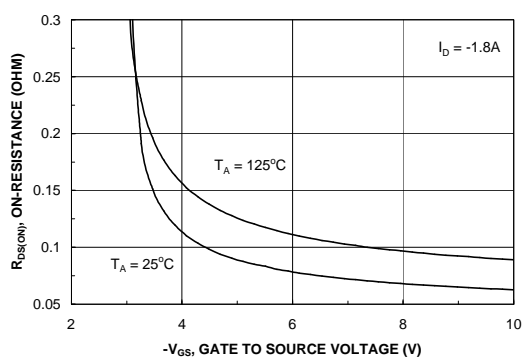Figure 3. On-Resistance Variation with
Temperature.

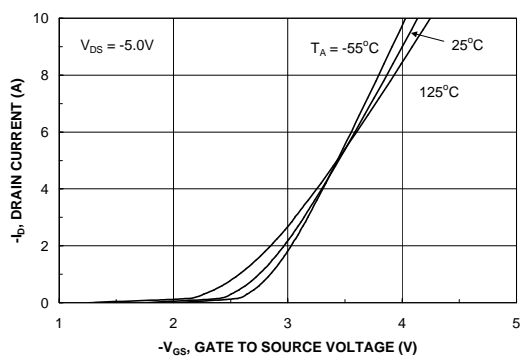Figure 4. On-Resistance Variation with
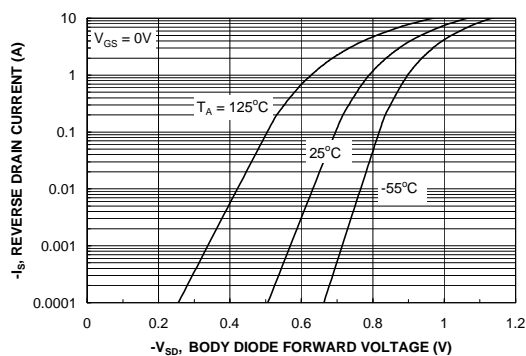Gate-to-Source Voltage.

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation
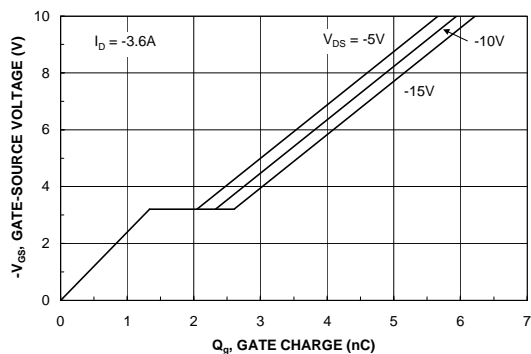with Source Current and Temperature.

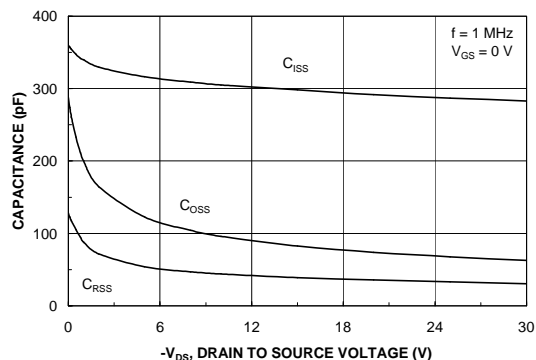## Typical Characteristics

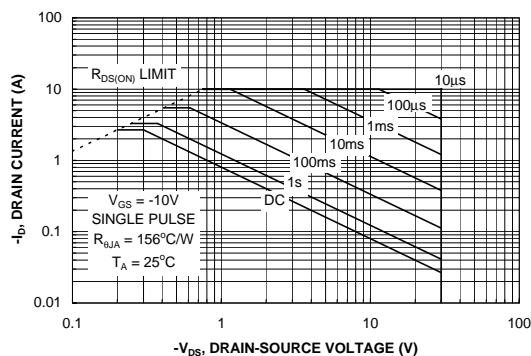Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.

Figure 9. Maximum Safe Operating Area.
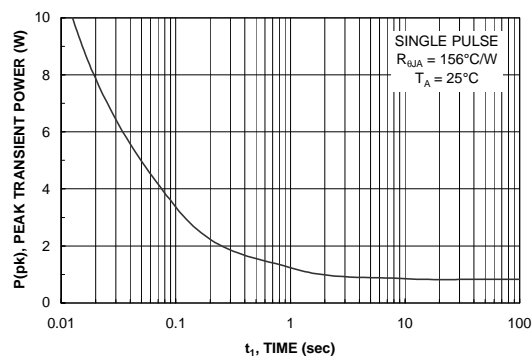
Figure 10. Single Pulse Maximum Power Dissipation.
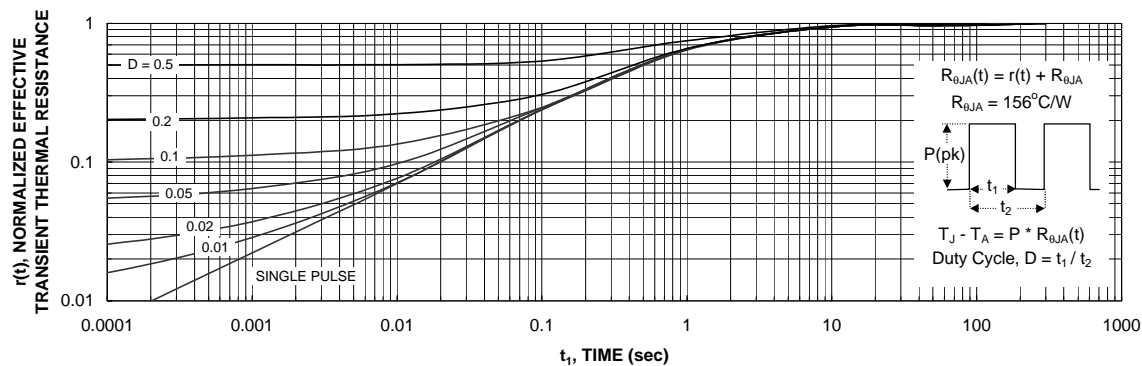
Figure 11. Transient Thermal Response Curve.

**Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.**

PUBLICATION ORDERING INFORMATION

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