

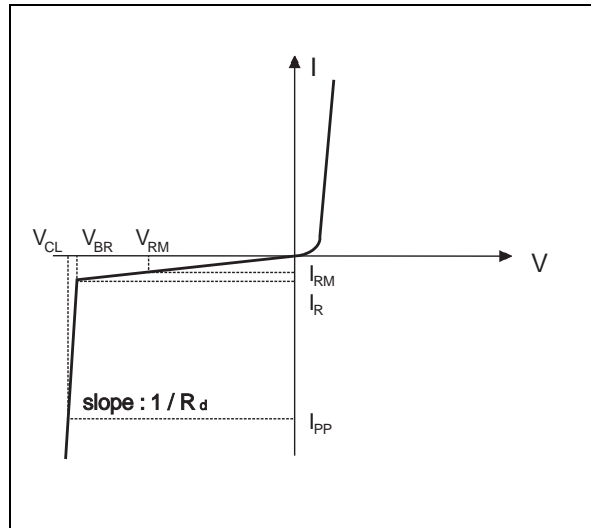
EMIF01-10005W5

ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC1000-4-2, air discharge ESD discharge IEC1000-4-2, contact discharge	16 9	kV
T_j	Junction temperature	150	$^{\circ}\text{C}$
T_{op}	Operating temperature range	-40 to + 85	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to +150	$^{\circ}\text{C}$
T_L	Lead solder temperature (10 second duration)	260	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input and Output
C_{IN}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	6	7	8	V
I_{RM}	$V_{RM} = 3\text{ V}$			1	μA
$R_{I/O}$		80	100	120	Ω
R_d	$I_{pp} = 10\text{ A}$, $t_p = 2.5\text{ }\mu\text{s}$ (see note 1)		1		Ω
C_{IN}	at 0V bias		50		pF

Note 1 : to calculate the ESD residual voltage, please refer to the paragraph "ESD PROTECTION" on pages 4 & 5

TECHNICAL INFORMATION

FREQUENCY BEHAVIOR

The EMIF01-10005W5 is firstly designed as an EMI/RFI filter. This low-pass filter is characterized by the following parameters:

- Cut-off frequency
- Insertion loss
- High frequency rejection

Fig A1: EMIF01-10005W5 frequency response curve.

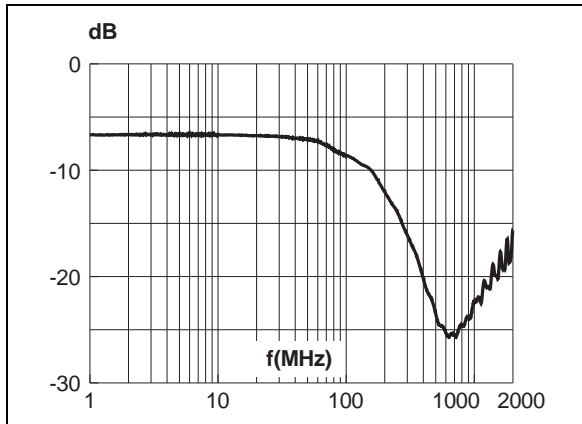
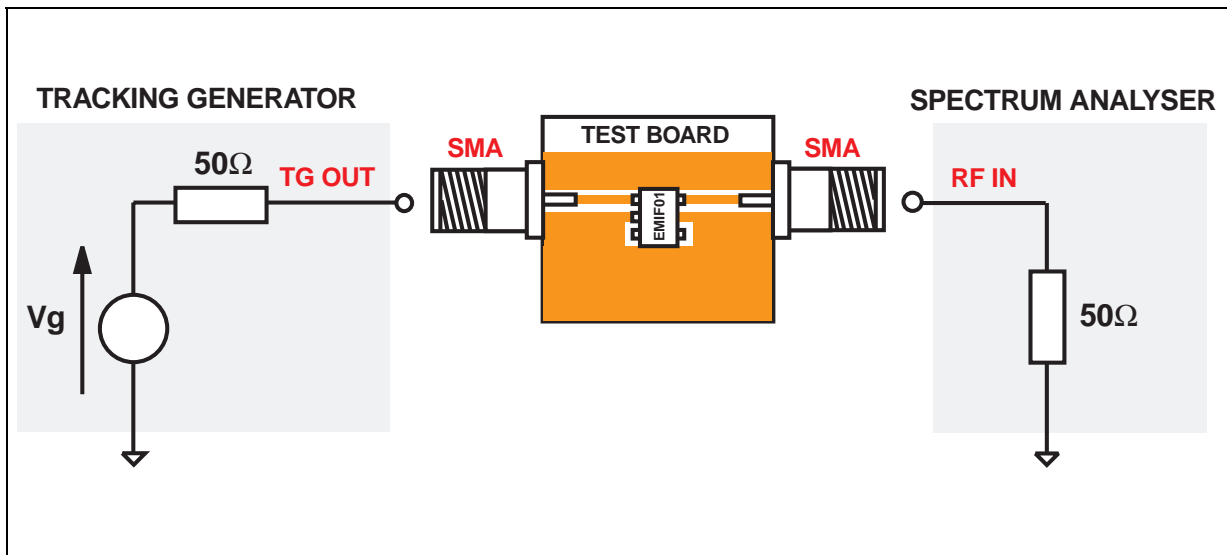


Figure A1 gives these parameters, in particular the signal rejection at the GSM frequency is about -24dB at 900MHz,

Fig A2: Measurement conditions



EMIF01-10005W5

ESD PROTECTION

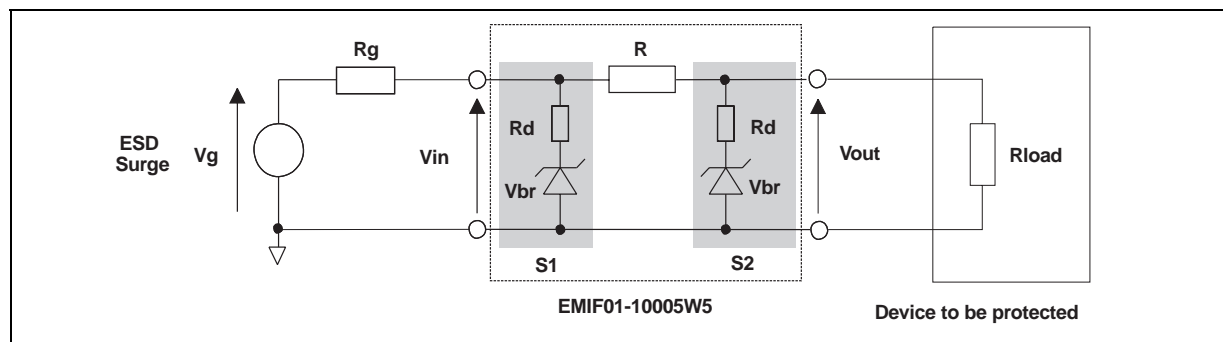
In addition to its filtering function, the EMIF01-10005W5 is particularly optimized to perform ESD protection.

ESD protection is based on the use of device which clamps at :

$$V_{CL} = V_{BR} + R_d \cdot I_{PP}$$

This protection function is splitted in 2 stages. As shown in figure A3, the ESD strikes are clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor R. Such a configuration makes the output voltage very low at the Vout level.

Fig A3 : ESD clamping behavior



To have a good approximation of the remaining voltages at both Vin and Vout stages, we provide the typical dynamical resistance value Rd. By taking into account these following hypothesis : $R \gg R_d$, $R_G \gg R_d$ and $R_{load} \gg R_d$, it gives these formulas:

$$V_{in} = \frac{R_g \cdot V_{br} + R_d \cdot V_g}{R_g}$$

$$V_{out} = \frac{R \cdot V_{br} + R_d \cdot V_{in}}{R}$$

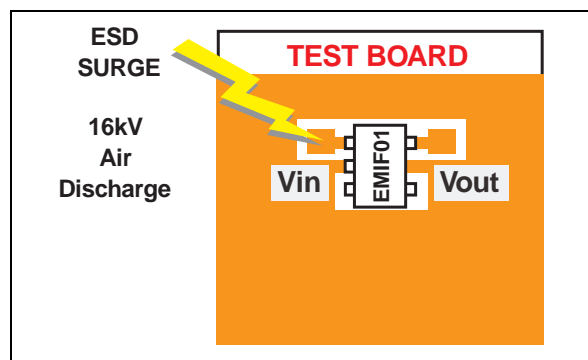
The results of the calculation done for $V_G=8kV$, $R_G=330\Omega$ (IEC1000-4-2 standard) and $V_{BR}=7V$ (typ.) give:

$$V_{in} = 31.2 V$$

$$\underline{V_{out} = 7.3 V}$$

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the Vin side. This parasitic effect is not present at the Vout side due the low current involved after the resistance R.

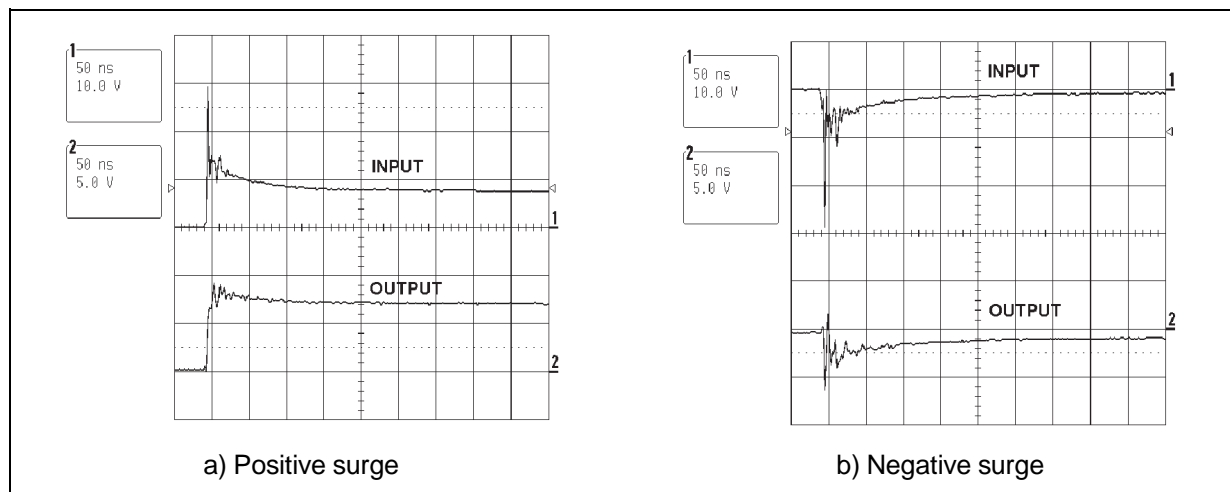
Fig A4 : Measurement conditions



The measurements shown here after illustrate very clearly (Fig. A5a) the high efficiency of the ESD protection :

- no influence of the parasitic inductances on Vout stage
- Vout clamping voltage very close to V_{BR}

Fig A5 : Remaining voltage at both stages S1 (Vin) and S2 (Vout) during ESD surge

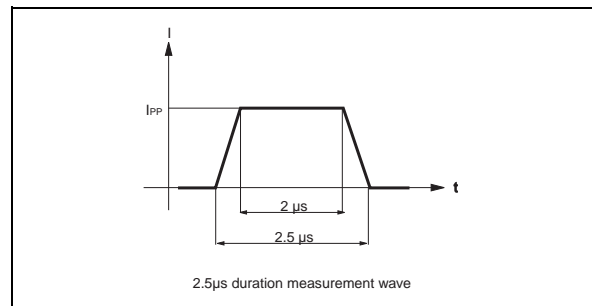


Please note that the EMIF01-10005W5 is not only acting for positive ESD surges but also for negative ones. For these kind of disturbances it clamps close to ground voltage as shown in Fig. A5b.

NOTE: DYNAMIC RESISTANCE MEASUREMENT

As the value of the dynamic resistance remains stable for a surge duration lower than $20\mu\text{s}$, the $2.5\mu\text{s}$ rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of R_d .

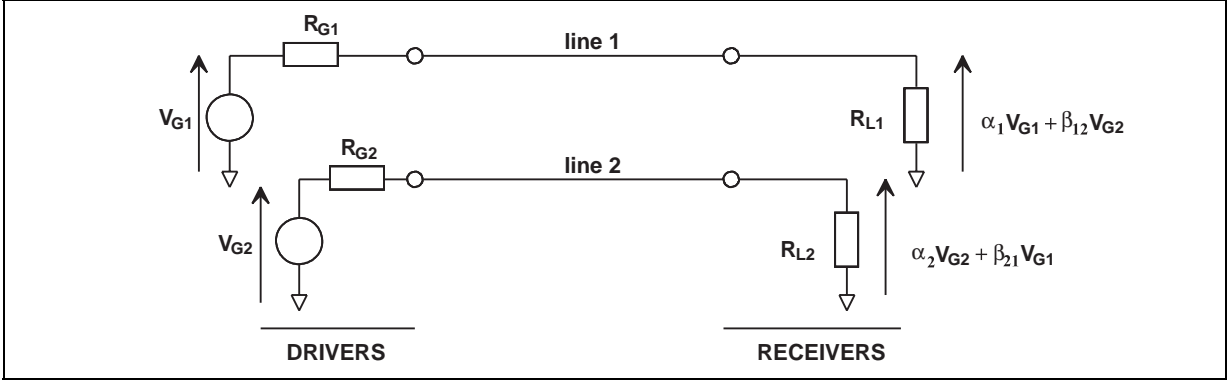
Fig A6 : R_d measurement current wave



CROSSTALK BEHAVIOR

1- Crosstalk phenomena

Fig A7 : Crosstalk phenomena



2- Digital Crosstalk

Fig A8 : Digital crosstalk measurement

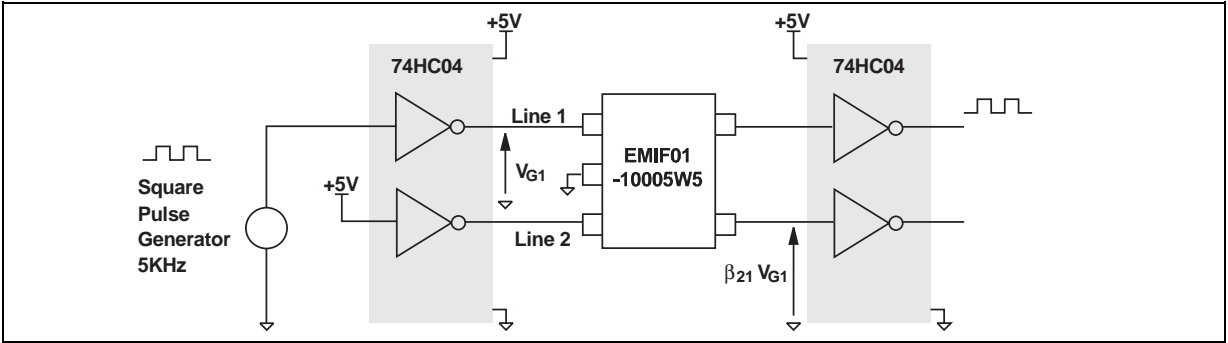
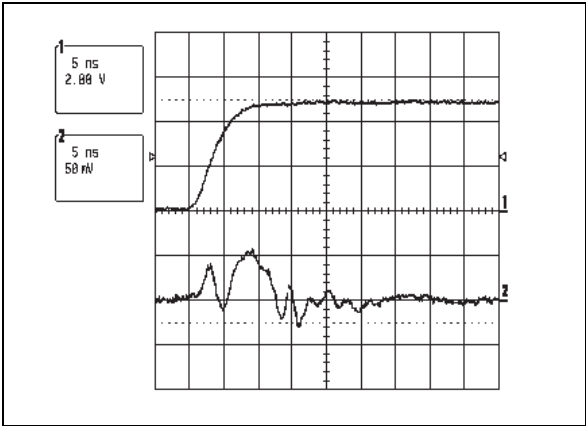


Figure A8 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

Figure A9 shows that in such a condition signal from 0 to 5V and rise time of 3 ns, the impact on the disturbed line is less than 100mV peak to peak. No data disturbance was noted on the concerned line. The same results were obtained with falling edges.

Fig A9 : Digital crosstalk results



3- Analog Crosstalk

Fig A10 : Analog crosstalk measurement

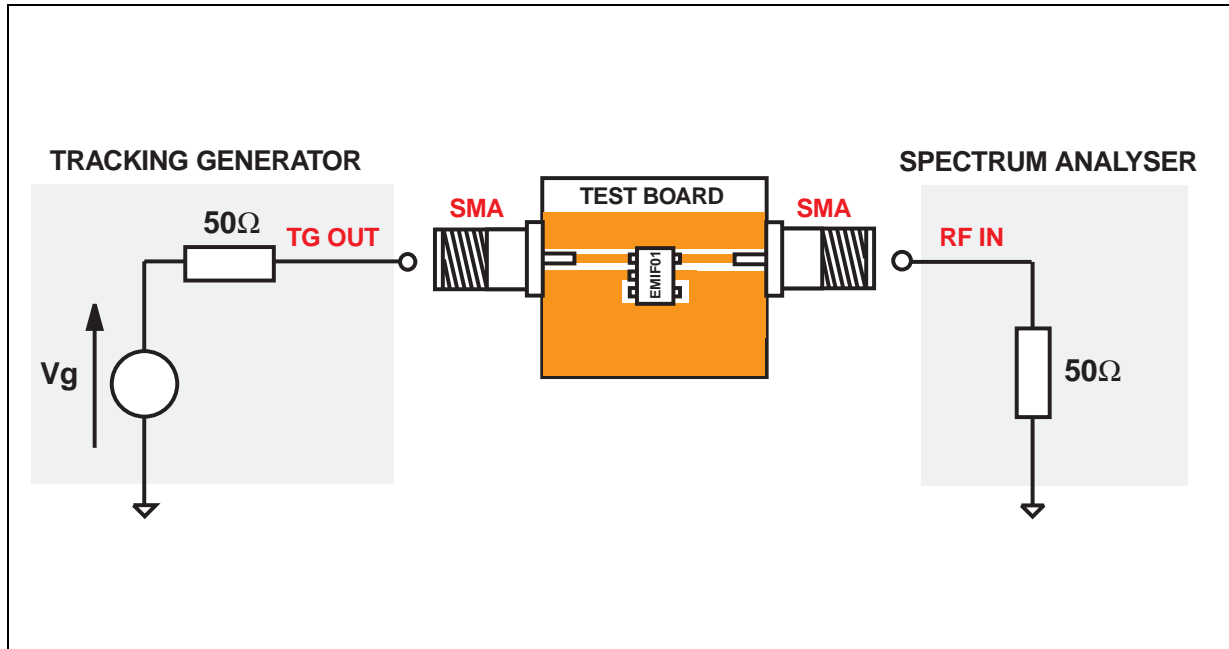


Fig A11 : Typical analog crosstalk result

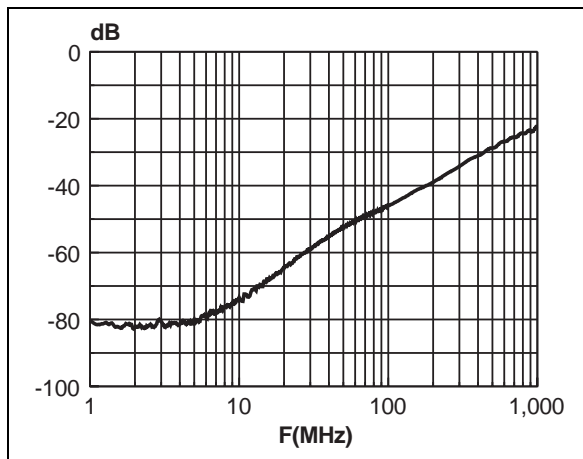


Figure A10 gives the measurement circuit for the analog application. In figure A11, the curve shows the effect of cell I/O1 on cell I/O2. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -43 dB.

EMIF01-10005W5

4 - PSpice model

Fig A12: PSpice model of one EMIF01 cell

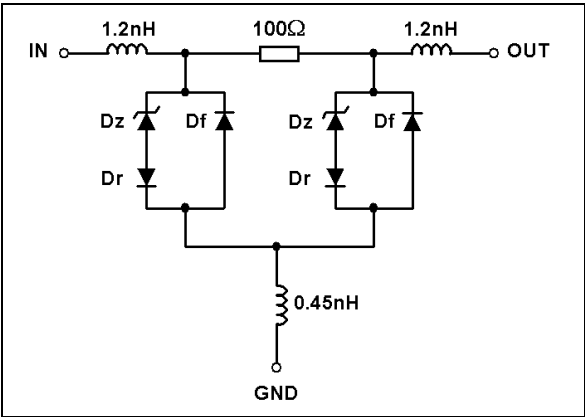


Fig A13: PSpice parameters

	Dz	Df	Dr
BV	7	1000	1000
Cjo	25p	25p	1p
IBV	100u	100u	100u
IKF	1000	1000	1000
IS	10E-15	1.016E-15	10E-15
ISR	100p	100p	100p
N	1	1.0755	0.6
M	0.3333	0.3333	0.3333
RS	1	1	1m
VJ	0.6	0.6	0.6
TT	50n	50n	1n

of 27°C

Note This model is available for an ambient temperature

Fig. A14: PSpice simulation : IEC 1000-4-2 Contact Discharge response

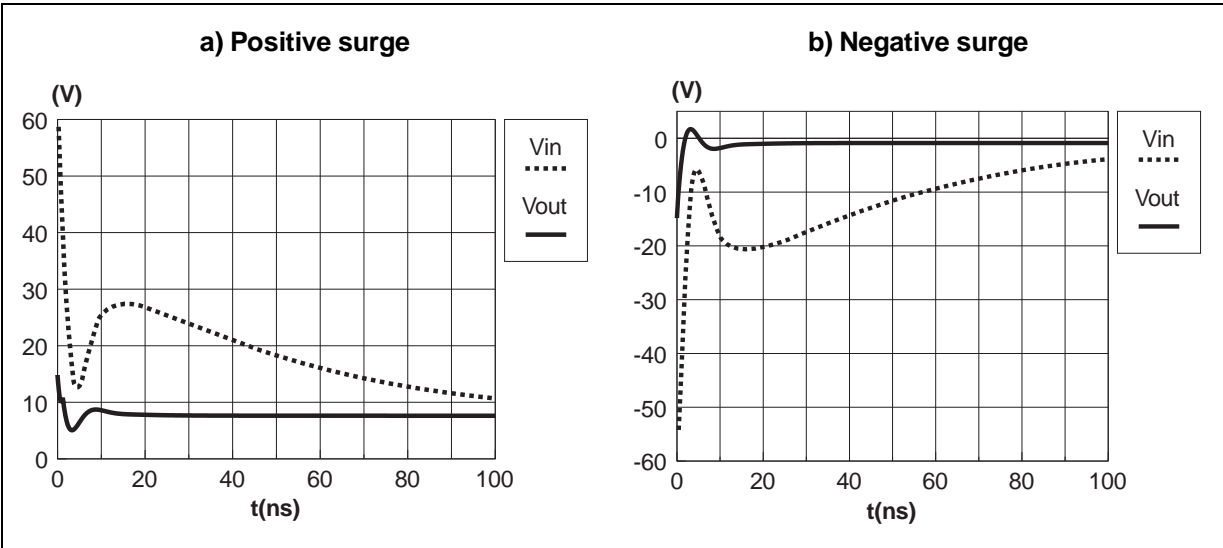
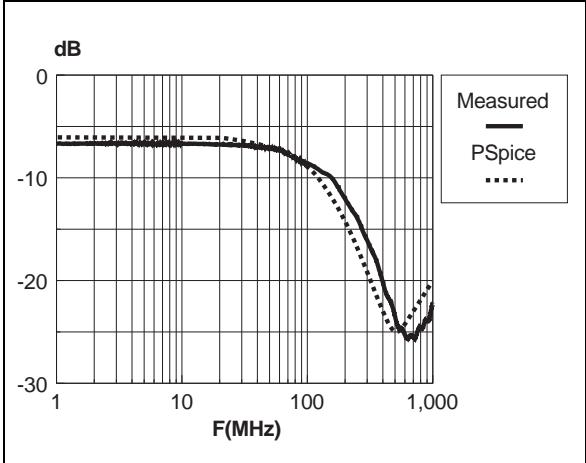
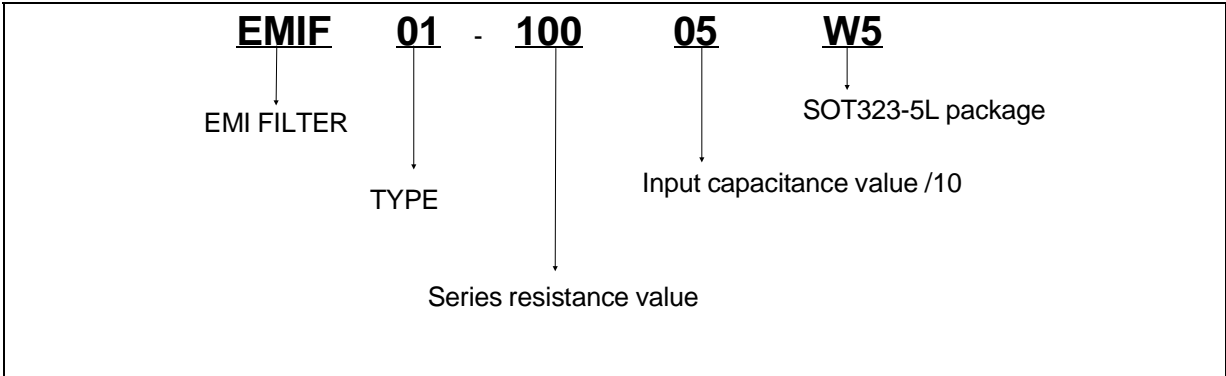


Fig A15: Comparison between PSpice simulation and measured frequency response

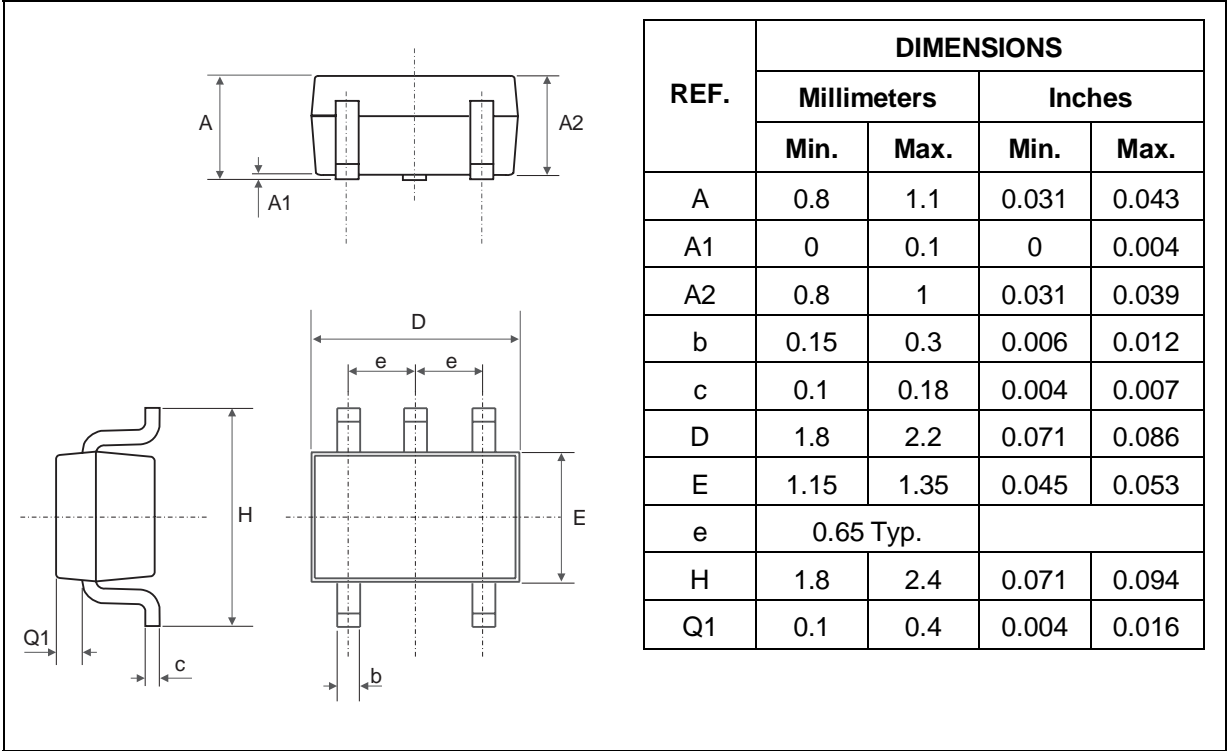


ORDER CODE

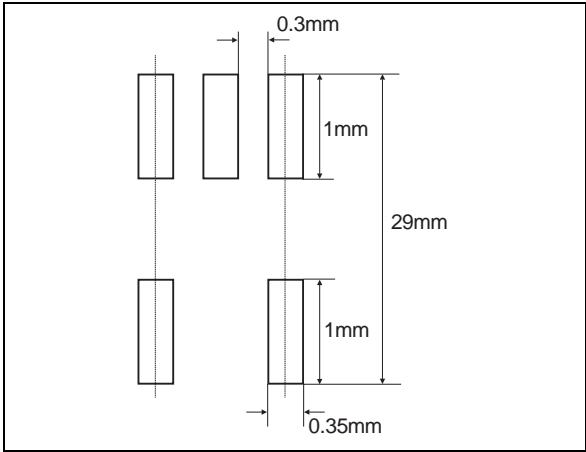


Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF01-10005W5	M12	SOT323-5L	5.4 mg	3000	Tape & reel

PACKAGE MECHANICAL DATA
SOT323-5L



RECOMMENDED FOOTPRINT



Mechanical specifications	
Lead plating	Tin-lead
Lead plating thickness	5µm min. 25 µm max.
Lead material	Sn / Pb (70% to 90% Sn)
Lead coplanarity	100µm max.
Body material	Molded epoxy
Flammability	UL94V-0

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