

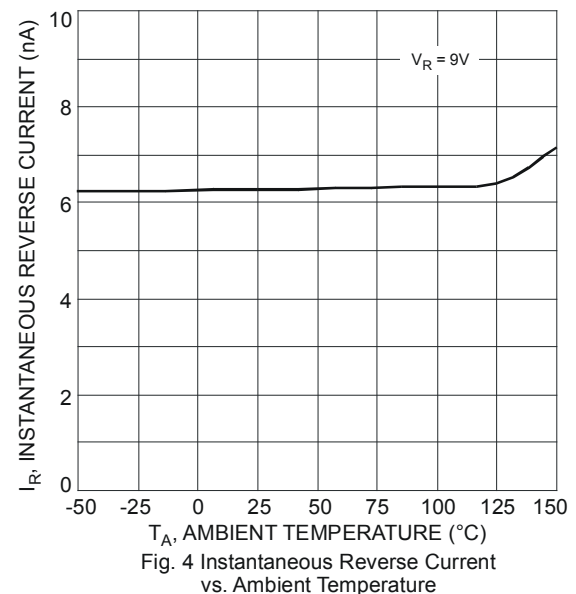
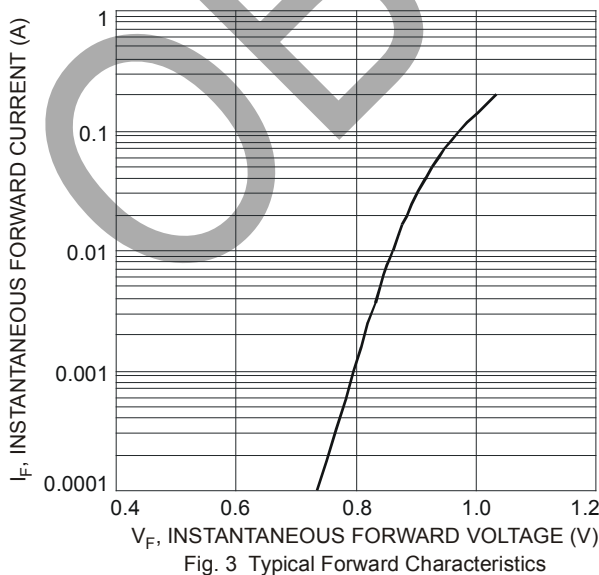
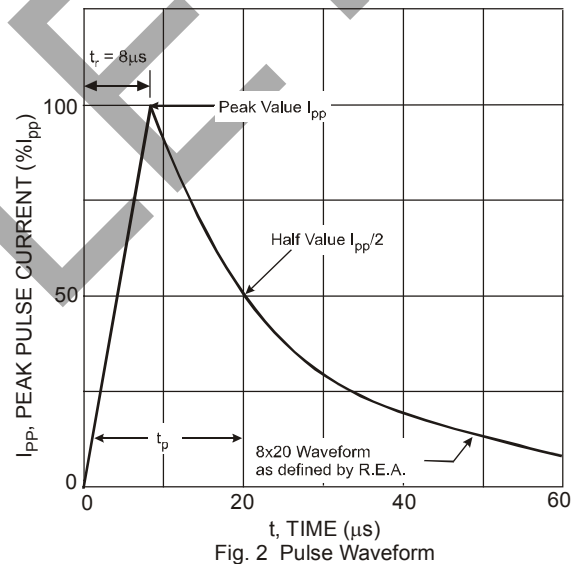
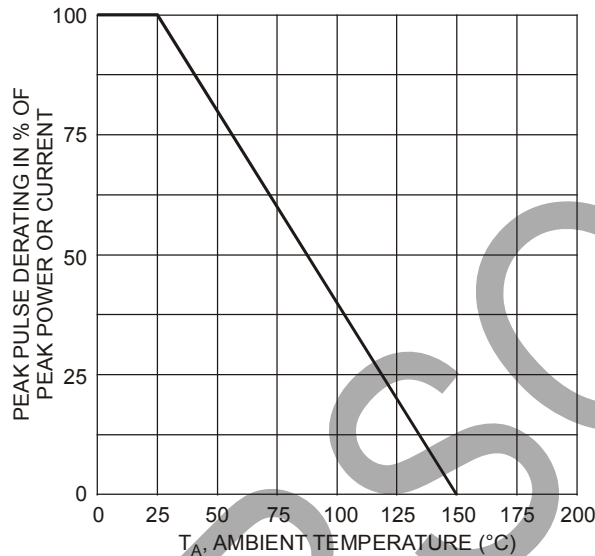
## Thermal Characteristics

Characteristic	Symbol	Value	Unit
Peak Power Dissipation, 8x20 $\mu$ S Waveform (Note 5)	$P_{pk}$	18	W
Thermal Resistance, Junction-to-Ambient (Note 5)	$R_{\theta JA}$	417	$^{\circ}C/W$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^{\circ}C$

## Electrical Characteristics @ $T_A = 25^{\circ}C$ unless otherwise specified

Type Number	Marking Code	Breakdown Voltage (Note 6)			Leakage Current (Note 6)		Capacitance @0V Bias(pF) (Note 7)		Capacitance @3V Bias(pF) (Note 7)	
		$V_{BR} @ I_T = 5mA$			$I_{RM} @ V_{RM}$		$C_T$		$C_T$	
		Min (V)	Nom (V)	Max (V)	Max( $\mu A$ )	(V)	Typ	Max	Typ	Max
DUP412VP5	V1	11.4	12	12.7	0.5	9.0	6.5	10	3.5	5

- Notes:
4. Non-repetitive current pulse per Figure 2 and derate above  $T_A = 25^{\circ}C$  per Figure 1.
  5. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. Suggested Pad Layout Document AP02001, which can be found on our website at <http://www.diodes.com>.
  6. Short duration pulse test used to minimize self-heating effect.
  7. Per element,  $f = 1MHz$ ,  $T_A = 25^{\circ}C$



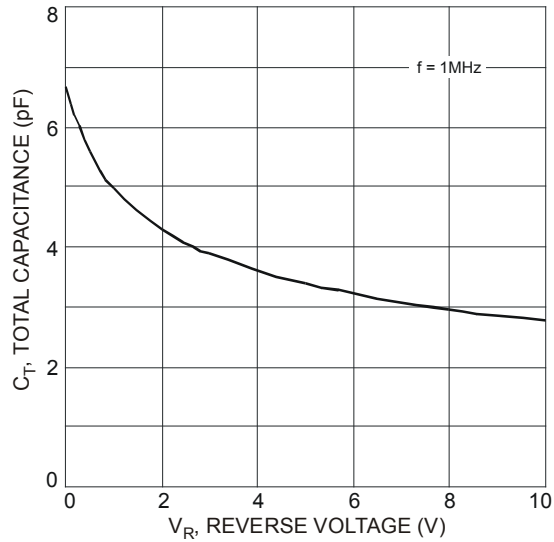
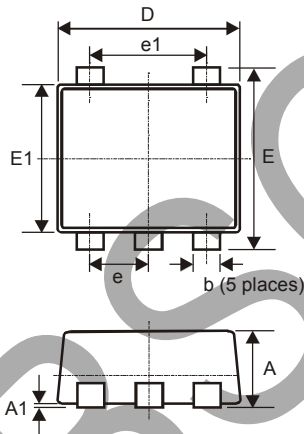


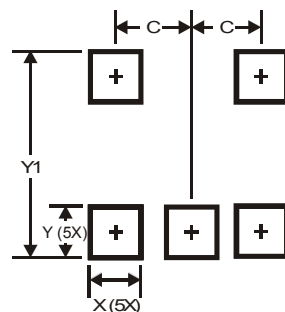
Fig. 5 Typical Total Capacitance vs. Reverse Voltage (Per Element)

## Package Outline Dimensions



SOT-953			
Dim	Min	Max	Typ
A	0.40	0.50	0.45
A1	0	0.05	—
b	0.10	0.20	0.15
c	0.12	0.18	0.15
D	0.95	1.05	1.00
E	0.95	1.05	1.00
E1	0.75	0.85	0.80
e	—	—	0.35
e1	—	—	0.70
L	0.05	0.15	0.10
All Dimensions in mm			

## Suggested Pad Layout



Dimensions	Value (in mm)
C	0.350
X	0.200
Y	0.200
Y1	1.100

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