ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground....-0.3V to +6.0V
Operating Temperature Range (Noncondensing)....-40°C to +85°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10 seconds) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

µSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....206.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....42°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		1.71	3.3	5.5	V
Backup Supply Voltage	V_{BACKUP}		1.3	3.0	3.7	V
	$V_{BACKMIN}$		1.15	1.3		
Logic 1	V_{IH}		0.7 x V_{CC}		5.5	V
Logic 0	V_{IL}		-0.3		0.3 x V_{CC}	V
Power-Fail Voltage	V_{PF}		1.51	1.61	1.71	V

DC ELECTRICAL CHARACTERISTICS

(**V_{CC} = MIN to MAX**, V_{BACKUP} = MIN to MAX, T_A = -40°C to +85°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage	I_{LI}	(Note 3)	-0.1		0.1	µA
I/O Leakage	I_{LO}	(Note 4)	-0.1		0.1	µA
Logic 0 Out (SDA or SQW/$\overline{INT}$) V_{OL} = 0.4V, $V_{CC} \geq V_{CCMIN}$	I_{OL}	(Note 4)			3	mA
Logic 0 Out (SQW/$\overline{INT}$) V_{OL} = 0.2V, V_{CC} = 0V, $V_{BAT} \geq V_{BATMIN}$	I_{OL}	(Note 4)			250	µA
V_{CC} Active Current	I_{CCA}	(Note 5)			450	µA
V_{CC} Standby Current	I_{CCS}	(Note 6)			200	µA
Trickle-Charger Resistor Register 10h = A5h, V_{CC} = Typ, V_{BACKUP} = 0V	R1	(Note 7)		200		Ω

DC ELECTRICAL CHARACTERISTICS (continued)

(**V_{CC} = MIN to MAX**, V_{BACKUP} = MIN to MAX, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Trickle-Charger Resistor Register 10h = A6h, V_{CC} = Typ, V_{BACKUP} = 0V	R2			2000		Ω
Trickle-Charger Resistor Register 10h = A7h, V_{CC} = Typ, V_{BACKUP} = 0V	R3			4000		Ω
V_{BACKUP} Leakage Current	I_{BKLKG}		-100	25	200	nA

DC ELECTRICAL CHARACTERISTICS

(**V_{CC} = 0V**, V_{BACKUP} = MIN to MAX, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BACKUP} Current EOSC = 0, SQW Off	I_{BKOSC}	(Note 8)		300	600	nA
V_{BACKUP} Current EOSC = 0, SQW On	I_{BKSQW}	(Note 8)		500	1100	nA
V_{BACKUP} Current EOSC = 1	I_{BKDR}			10	200	nA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = MIN to MAX, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2, Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		0.03		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 9)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 10, 11)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 12)	100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 13)	$20 + 0.1C_B$		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 13)	$20 + 0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = MIN to MAX, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2, Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitive Load for Each Bus Line	C_B	(Note 13)			400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	(Note 14)			10	pF
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 15)			100	ms
Timeout Interval	$t_{TIMEOUT}$	(Note 16)	25		35	ms

POWER-UP/DOWN CHARACTERISTICS

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 2, Figure 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Recovery at Power-Up	t_{REC}	(Note 17)		1	2	ms
V_{CC} Slew Rate; V_{PF} to 0V	t_{VCCF}				1/50	V/µs
V_{CC} Slew Rate; 0V to V_{PF}	t_{VCCR}				1/1	V/µs

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

Note 2: Limits are 100% production tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.
Note 3: SCL only.
Note 4: SDA and SQW/INT.
Note 5: I_{CCA}—SCL at f_{SCL} max, V_{IL} = 0.0V, V_{IH} = V_{CC}, trickle charger disabled.
Note 6: Specified with the I²C bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}, trickle charger disabled.
Note 7: V_{CC} must be less than 3.63V if the 200Ω resistor is selected.
Note 8: Using recommended crystal on X1 and X2.
Note 9: After this period, the first clock pulse is generated.
Note 10: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 11: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 12: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq$ to 250ns must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT}$ = 1000 + 250 = 1250ns before the SCL line is released.
Note 13: C_B—total capacitance of one bus line in pF.
Note 14: Guaranteed by design; not production tested.
Note 15: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set.
Note 16: The DS1339A can detect any single SCL clock held low longer than $t_{TIMEOUTMIN}$. The device's I²C interface is in reset state and can receive a new START condition when SCL is held low for at least $t_{TIMEOUTMAX}$. Once the device detects this condition, the SDA output is released. The oscillator must be running for this function to work.
Note 17: This delay applies only if the oscillator is running. If the oscillator is disabled or stopped, no power-up delay occurs.

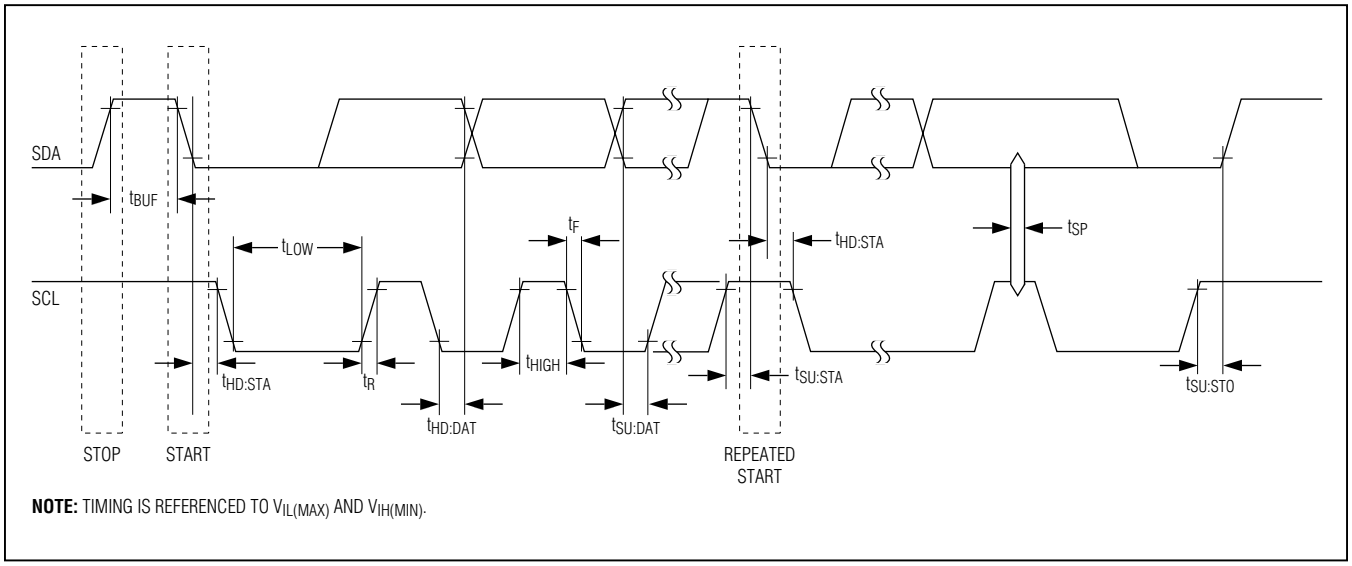


Figure 1. I²C Timing

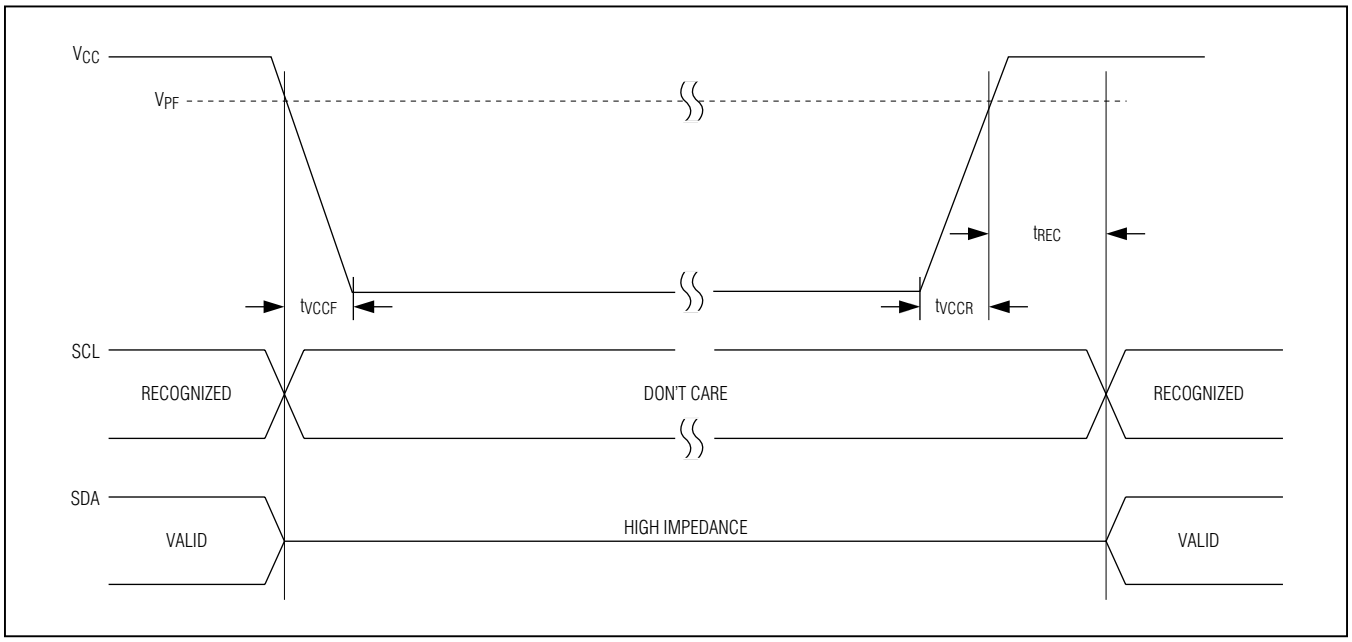
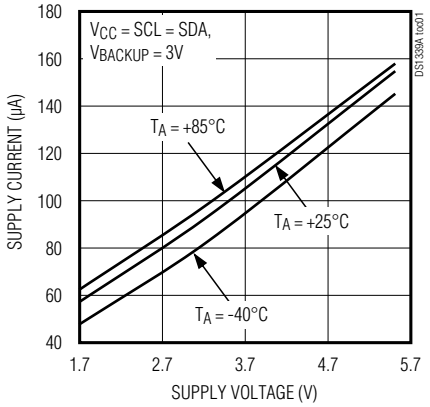


Figure 2. Power-Up/Down Timing

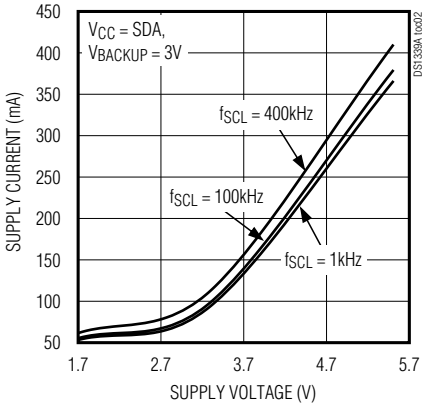
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

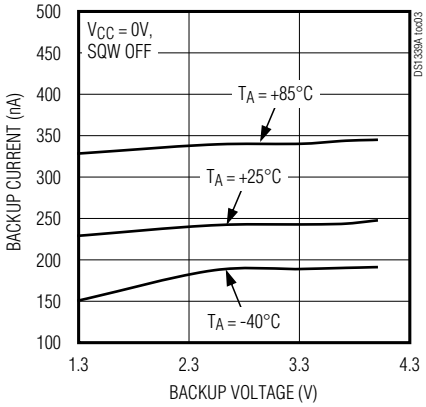
POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE



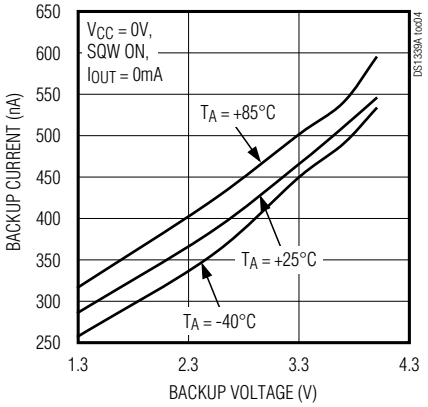
POWER SUPPLY CURRENT vs. SCL FREQUENCY



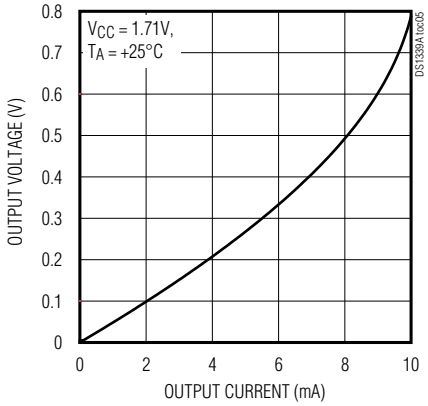
BACKUP SUPPLY CURRENT vs. BACKUP VOLTAGE



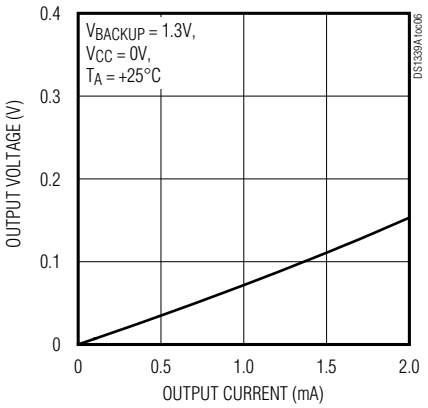
BACKUP SUPPLY CURRENT vs. BACKUP VOLTAGE



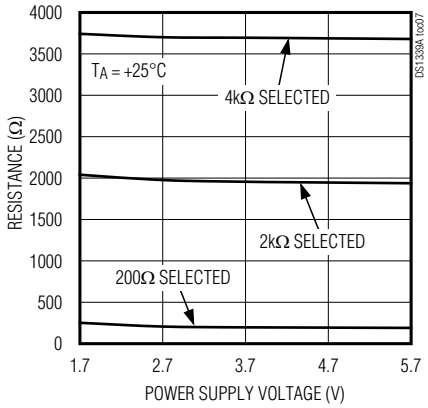
$\overline{INT}$/SQW OUTPUT CURRENT vs. OUTPUT VOLTAGE



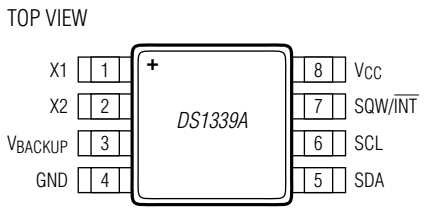
$\overline{INT}$/SQW OUTPUT CURRENT vs. OUTPUT VOLTAGE



TRICKLE CHARGER RESISTORS vs. POWER SUPPLY VOLTAGE



Pin Configuration



µSOP

Pin Description

PIN	NAME	FUNCTION
1	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6pF. For more information about crystal selection and crystal layout considerations, see the *Applications Information* section and refer to Application Note 58: *Crystal Considerations with Dallas Real-Time Clocks*.
2	X2	
3	VBACKUP	Secondary Power Supply. Supply voltage must be held between 1.3V and 3.7V for proper operation. This pin can be connected to a primary cell, such as a lithium coin cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used in conjunction with the trickle-charge feature. Diodes should not be placed in series between the backup source and the VBACKUP input, or improper operation will result. If a backup supply is not required, VBACKUP must be grounded. UL recognized to ensure against reverse charging current when used with a primary lithium cell. For more information, visit **www.maximintegrated.com/qa/info/ul**.
4	GND	Ground
5	SDA	Serial Data Input/Output. SDA is the input/output pin for the I²C serial interface. The SDA pin is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V regardless of the voltage on VCC.
6	SCL	Serial Clock Input. SCL is used to synchronize data movement on the I²C serial interface. The pull up voltage may be up to 5.5V regardless of the voltage on VCC.
7	SQW/$\overline{INT}$	Square-Wave/Interrupt Output. Programmable square-wave or interrupt output signal. The SQW/$\overline{INT}$ pin is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V regardless of the voltage on VCC. If not used, this pin may be left unconnected.
8	VCC	Primary Power Supply. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected and VCC is below VPF, reads and writes are inhibited. The timekeeping and alarm functions operate when the device is powered by VCC or VBACKUP.

Detailed Description

The DS1339A serial real-time clock (RTC) is a low-power clock/date device with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I²C bus. The clock/date provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The DS1339A has a built-in power-sense circuit that detects power failures and automatically switches to the backup supply, maintaining time, date, and alarm operation.

Table 1. Power Control

SUPPLY CONDITION	READ/ WRITE ACCESS	POWERED BY
$V_{CC} < V_{PF}$, $V_{CC} < V_{BACKUP}$	No	V_{BACKUP}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BACKUP}$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BACKUP}$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BACKUP}$	Yes	V_{CC}

Table 2. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			60	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to Application Note 58: Crystal Considerations for Dallas Real-Time Clocks for additional specifications.*

Operation

The DS1339A operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels. The *Functional Diagram* shows the main elements of the serial real-time clock.

Power Control

The power-control function is provided by a precise, temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels (Table 1). After V_{CC} returns above V_{PF}, read and write access is allowed after t_{REC} (Figure 2). On the first application of power to the device the time and date registers are reset to 01/01/00 01 00:00:00 (DD/MM/YY DOW HH:MM:SS).

Oscillator Circuit

The DS1339A uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 2 specifies several crystal parameters for the external crystal. The *Functional Diagram* shows a basic schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may result in the clock running fast. Figure 6 shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to Application Note 58: *Crystal Considerations with Dallas Real-Time Clocks* for detailed information

RTC Address Map

Table 3 shows the address map for the DS1339A registers. During a multibyte access, when the address pointer reaches the end of the register space (10h), it wraps around to location 00h. On an I²C START or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Time and Date Operation

The time and date information is obtained by reading the appropriate register bytes. Table 3 shows the RTC registers. The time and date are set or initialized by writing the appropriate register bytes. The contents of the time and date registers are in the BCD format. The DS1339A can be run in either 12-hour or 24-hour mode. Bit 6 of the HOURS register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the 20-hour bit (20 to 23 hours). All hours values, including the alarms, must be re-entered whenever the 12/$\overline{24}$-hour mode bit is changed.

The Century bit (bit 7 of the MONTH register) is toggled when the YEAR register overflows from 99 to 00. If the Century bit is logic 0, the year will be designated as a Leap Year and February will contain 29 days.

If the Century bit is logic 1, the year will not be designated as a Leap Year and February will contain 28 days.

The Day-Of-Week register increments at midnight. Values that correspond to the day of week are user-defined, but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on a START or when the address pointer rolls over to 00h. The countdown chain is reset whenever the seconds register is written. Write transfers occurs on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within one second. If enabled, the 1Hz square-wave output transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

Table 3. Timekeeping Register Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00h	0	10 Seconds			Seconds				Seconds	00-59
01h	0	10 Minutes			Minutes				Minutes	00-59
02h	0	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hours				Hours	01-12 +AM/PM 00-23
03h	0	0	0	0	0	Day			Day	01-07
04h	0	0	10 Date						Date	01-31
05h	Century	0	0	10 Month	Month				Month	01-12 +Century
06h	10 Year				Year				Year	00-99
07h	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00-59
08h	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00-59
09h	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hours				Alarm 1 Hours	01-12 +AM/PM 00-23
0Ah	A1M4	DY/$\overline{DT}$	10 Date		Day, Date				Alarm 1 Day, Alarm 1 Date	01-07, 01-31
0Bh	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00-59
0Ch	A2M3	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hours				Alarm 2 Hours	01-12 +AM/PM 00-23
0Dh	A2M4	DY/$\overline{DT}$	10 Date		Day, Date				Alarm 2 Day, Alarm 2 Date	01-07, 01-31
0Eh	$\overline{EOSC}$	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE	Control	-
0Fh	OSF	0	0	0	0	0	A2F	A1F	Status	-
10h	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	Trickle Charger	-

"0" - reads as Logic 0.

Note: *Unless otherwise specified, the state of the registers are not defined when power is first applied or when V_{CC} and V_{BACKUP} fall below the $V_{BACKUP(MIN)}$.*

Alarms

The DS1339A contains two time of day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the Alarm Enable and INTCN bits of the Control Register) to activate the SQW/$\overline{INT}$ output on an alarm match condition. Bit 7 of each of the time of day/date alarm registers are mask bits (Table 4). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h to 06h match the values stored in the time of day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 4 shows the possible settings. Configurations not listed in the table result in illogical operation.

The DY/$\overline{DT}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/$\overline{DT}$ is written to a logic 0, the alarm is the result of a match with date of the month. If DY/$\overline{DT}$ is written to a logic 1, the alarm is the result of a match with day of the week.

The device checks for an alarm match once per second. When the RTC register values match alarm register settings, the corresponding Alarm Flag 'A1F' or 'A2F' bit is set to logic 1. If the corresponding Alarm Interrupt Enable 'A1IE' or 'A2IE' is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the SQW/$\overline{INT}$ signal. If the BBSQI bit is set to 1, the $\overline{INT}$ output activates while the part is being powered by V_{BACKUP}. The alarm output remains active until the alarm flag is cleared by the user.

Table 4. Alarm Mask Bits

DY/$\overline{DT}$	ALARM1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/$\overline{DT}$	ALARM2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 sec. of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

Control Register (0Eh)

The control register controls the operation of the SQW/$\overline{INT}$ pin and provides oscillator status.

Bit #	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Name	$\overline{EOSC}$	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE
POR	0	0	0	1	1	0	0	0

Bit 7: Enable Oscillator ($\overline{EOSC}$). When the $\overline{EOSC}$ bit is 0, the oscillator is enabled. When this bit is a 1, the oscillator is disabled. This bit is cleared (0) when power is first applied.

Bit 5: Battery-Backed Square-Wave Interrupt (BBSQI). When set to logic 1, this bit enables the SQW/$\overline{INT}$ output functionality while the part is powered by V_{BACKUP}. When set to logic 0, this bit disables the SQW/$\overline{INT}$ output while the part is powered by V_{BACKUP}.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the SQW/$\overline{INT}$ output when the square-wave has been enabled (INTCN=0). Table 5 lists the square-wave frequencies that can be selected with the RS bits.

Bit 2: Interrupt Control (INTCN). This bit controls the relationship between the two alarms and the interrupt output pin. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the Alarm 1 or Alarm 2 registers activate the SQW/$\overline{INT}$ pin (provided that the alarm is enabled). When the INTCN bit is set to logic 0, a square wave is output on the SQW/$\overline{INT}$ pin. This bit is set to logic 0 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to a logic 1, this bit permits the Alarm 2 Flag (A2F) bit in the status register to assert SQW/$\overline{INT}$ (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Table 5. SQW/$\overline{INT}$ Output

INTCN	RS2	RS1	SQW/$\overline{INT}$ OUTPUT	A2IE	A1IE
0	0	0	1Hz	X	X
0	0	1	4.096kHz	X	X
0	1	0	8.192kHz	X	X
0	1	1	32.768kHz	X	X
1	X	X	$\overline{A1F}$	0	1
1	X	X	$\overline{A2F}$	1	0
1	X	X	$\overline{A2F}$ + $\overline{A1F}$	1	1

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the Alarm 1 Flag (A1F) bit in the status register to assert SQW/$\overline{INT}$ (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate an interrupt signal. The A1IE bit is disabled (logic 0) when power is first applied.

Bit #	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Name	OSF	0	0	0	0	0	A2F	A1F
POR	1	0	0	0	0	0	0	0

Status Register (0Fh)

The control register controls the operation of the SQW/$\overline{INT}$ pin and provides oscillator status.

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator has stopped or was stopped for some time period and can be used to judge the validity of the clock and calendar data. This bit is edge triggered, and is set to logic 1 when the internal circuitry senses the oscillator has transitioned from a normal run state to a stopped condition. The following are examples of conditions that may cause the OSF bit to be set:

The first time power is applied.

The voltage present on V_{CC} and V_{BAT} are insufficient to support oscillation.

The $\overline{EOSC}$ bit is set to 1, disabling the oscillator.

External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to logic 0. Attempting to write OSF to logic 1 leaves the value unchanged.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the Alarm 2 Flag bit indicates that the time matched the Alarm 2 registers. If the A2IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/$\overline{INT}$ pin is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the Alarm 1 Flag bit indicates that the time matched the Alarm 1 registers. If the A1IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/$\overline{INT}$ pin is also asserted. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Trickle Charger (10h)

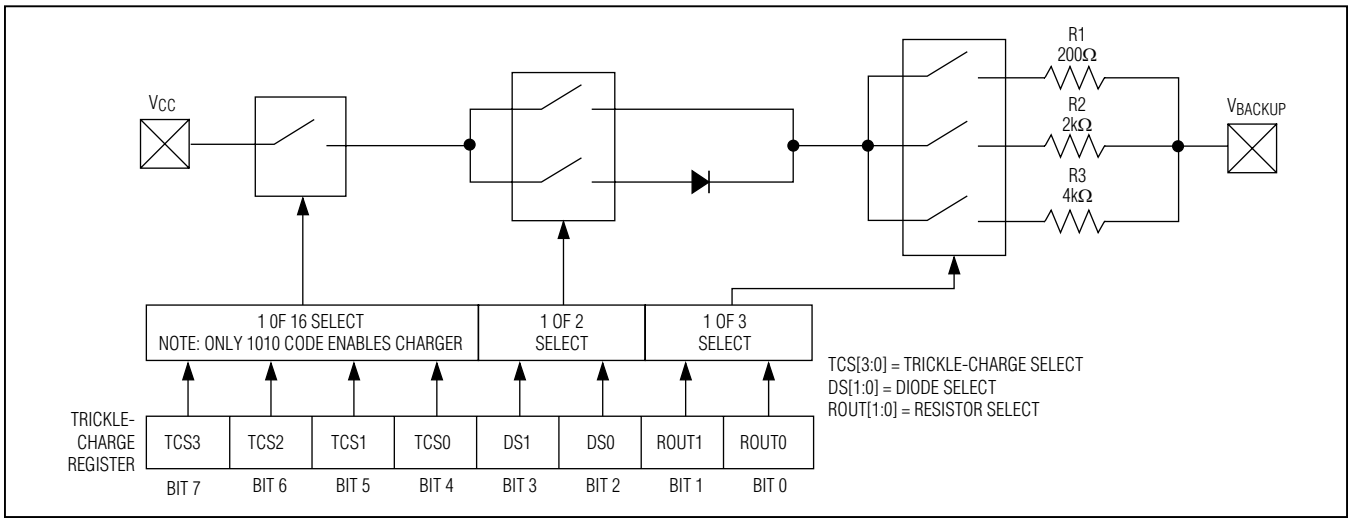


Figure 3. Trickle Charger

Table 6. Trickle Charger Register (10h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 200Ω resistor
1	0	1	0	1	0	0	1	One diode, 200Ω resistor
1	0	1	0	0	1	1	0	No diode, 2kΩ resistor
1	0	1	0	1	0	1	0	One diode, 2kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4kΩ resistor
0	0	0	0	0	0	0	0	Initial power-up values

The simplified schematic in Figure 3 shows the basic components of the trickle charger. The trickle-charge select bits (TCS[3:0]) control the selection of the trickle charger. To prevent accidental enabling, only a pattern on 1010 enables the trickle charger. All other patterns disable the trickle charger. The trickle charger is disabled when power is first applied. The diode-select (DS[1:0]) bits select whether or not a diode is connected between V_{CC} and V_{BACKUP}. The ROUT[1:0] bits select the value of the resistor connected between V_{CC} and V_{BACKUP}. Table 6 shows the register settings.

Warning: The ROUT value of 200Ω must not be selected whenever V_{CC} is greater than 3.63V.

The user determines diode and resistor selection according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a 3.3V system power supply is applied to V_{CC} and a super cap is connected to V_{BACKUP}. Also assume that the trickle charger

has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{MAX} would therefore be calculated as follows:

$$I_{MAX} = (3.3V - \text{diode drop}) / R2 \approx (3.3V - 0.7V) / 2k\Omega \approx 1.3mA$$

As the super cap or battery charges, the voltage drop between V_{CC} and V_{BACKUP} decreases and therefore the charge current decreases.

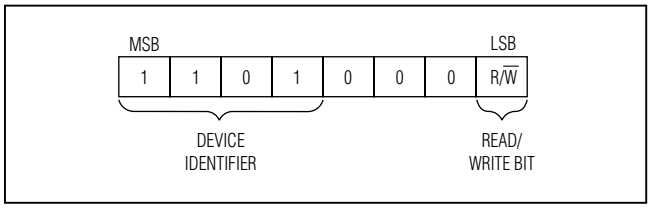


Figure 4. Slave Address Byte

I²C Serial Port Operation

I²C Slave Address

The DS1339A's slave address byte is D0h. The first byte sent to the device includes the device identifier and the R/$\overline{W}$ bit (Figure 4). The device address sent by the I²C master must match the address assigned to the device.

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle it often initiates a low-power mode for slave devices.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 1 for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 1 for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it immediately initiates a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 1 for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (see Figure 1). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end a write operation, the master must release the SDA bus line for the proper amount of setup time (see Figure 1) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledge (ACK and NACK): An Acknowledge (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgment from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgment is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit. The whatever's slave address is D0h and cannot be modified by the user. When the R/$\overline{W}$ bit is 0 (such as in D0h), the master is indicating it writes data to the slave. If R/$\overline{W}$ = 1, (D1h in this case), the master is indicating it wants to read from the slave. If an incorrect slave address is written, the DS1339A assumes the master is communicating with another I²C device and ignores the communication until the next START condition is sent.

Memory Address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgment during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the starting memory address, writes multiple data bytes, and generates a STOP condition.

Reading a Single Byte from a Slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the

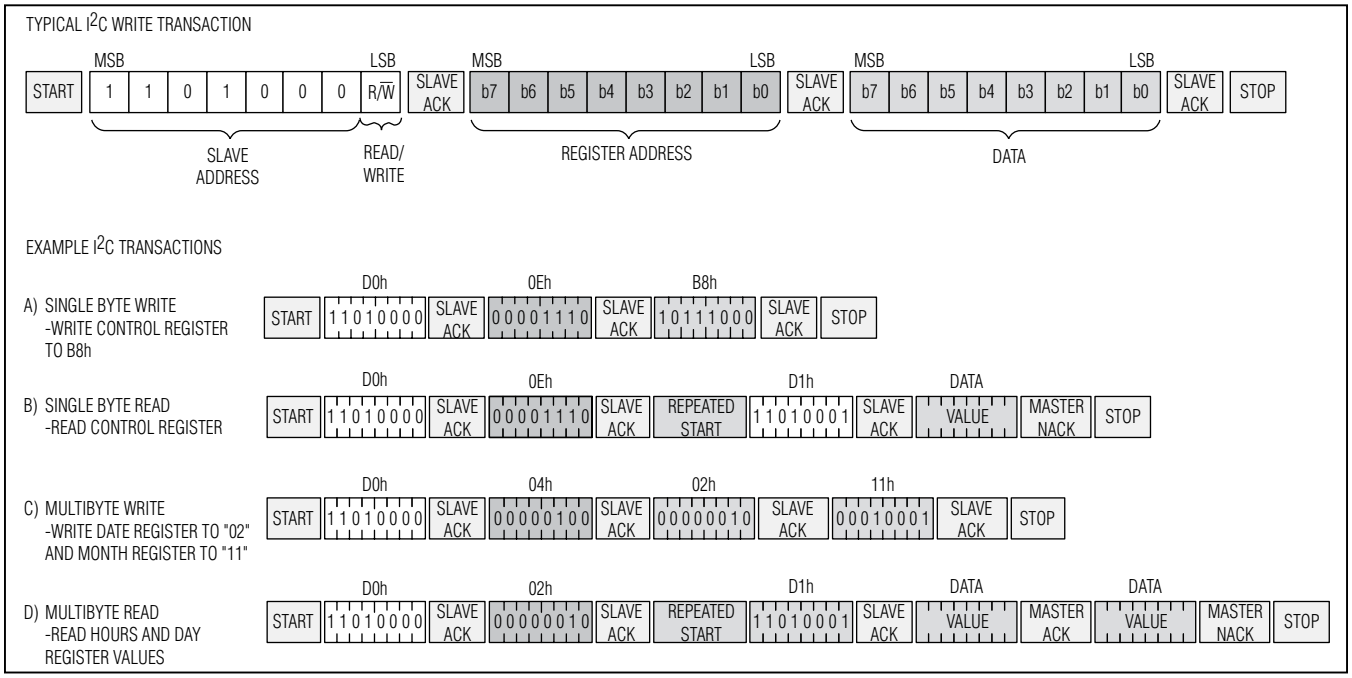


Figure 5. I²C Transactions

slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, since requiring the master to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition. See Figure 5 for a read example using the repeated START condition to specify the starting memory location.

Reading Multiple Bytes From a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it must NACK to indicate the end of the transfer and then it generates a STOP condition.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS1339A, decouple the V_{CC} power supply with a 0.01µF and/or 0.1µF capacitor. Use a high-quality, ceramic, surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Using an Open-Drain Output

The SQW/$\overline{INT}$ output is open-drain and therefore requires an external pullup resistor to realize a logic-high output level.

SDA and SCL Pullup Resistors

SDA is an open-drain output and requires an external pullup resistor to realize a logic-high output level.

Because the DS1339A does not use clock cycle stretching, a master using either an open-drain output with a pullup resistor or CMOS output driver (push-pull) could be used for SCL.

Battery Charge Protection

The DS1339A contains Maxim's redundant battery-charge protection circuit to prevent any charging of an external battery. The DS1339A is recognized by Underwriters Laboratories (UL) under file E141114.

Handling, PCB Layout, and Assembly

Avoid running signal traces under the package, unless a ground plane is placed between the package and the signal line. Do not use external components to compensate for improper crystal selection.

Moisture-sensitive packages are shipped from the factory dry-packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications.

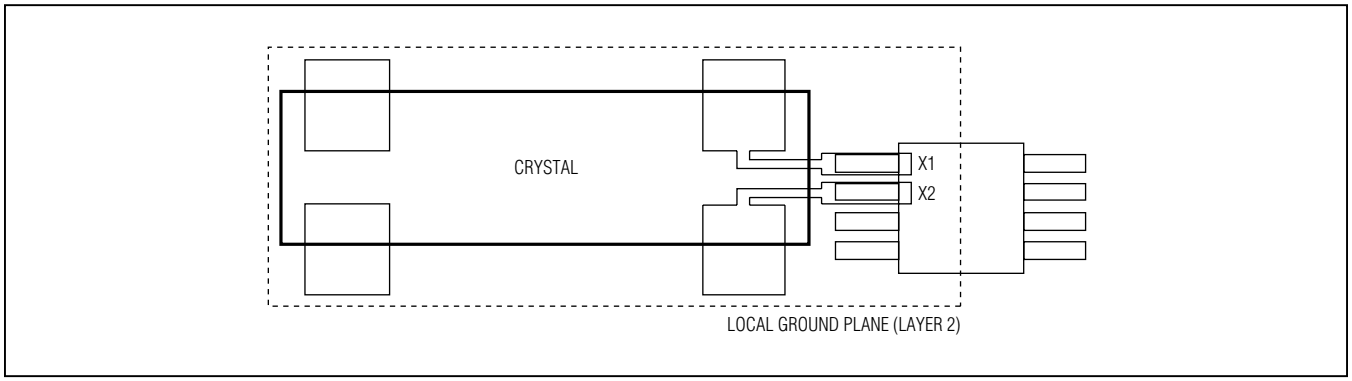


Figure 6. Typical PCB Layout for Crystal

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1339AU+	-40°C to +85°C	8 µSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: CMOS

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8-pin µSOP	U8+1	21-0036	90-0092

Low-Current, I²C, Serial Real-Time Clock

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/12	Initial release	—
1	5/13	Added UL certification reference	1, 17
2	1/15	Updated *Benefits and Features* section	1