ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK*
DS1306	0°C to +70°C	16 DIP (300 mils)	DS1306
DS1306+	0°C to +70°C	16 DIP (300 mils)	DS1306 +
DS1306N	-40°C to +85°C	16 DIP (300 mils)	DS1306N
DS1306N+	0°C to +70°C	16 DIP (300 mils)	DS1306N +
DS1306E	0°C to +70°C	20 TSSOP (173 mils)	DS1306
DS1306E+	0°C to +70°C	20 TSSOP (173 mils)	DS1306 +
DS1306EN	-40°C to +85°C	20 TSSOP (173 mils)	DS1306N
DS1306EN+	-40°C to +85°C	20 TSSOP (173 mils)	DS1306N +
DS1306EN/T&R	-40°C to +85°C	20 TSSOP (173 mils)	DS1306N
DS1306EN+T&R	-40°C to +85°C	20 TSSOP (173 mils)	DS1306N +
DS1306E/T&R	0°C to +70°C	20 TSSOP (173 mils)	DS1306
DS1306E+T&R	0°C to +70°C	20 TSSOP (173 mils)	DS1306 +

+Denotes a lead(Pb)-free/RoHS-compliant package
T&R = Tape and reel.
**An "N" on the top mark indicates an industrial device.*

PIN DESCRIPTION

PIN		NAME	FUNCTION
TSSOP	DIP		
1	1	V_{CC2}	**Backup Power Supply.** This is the secondary power supply pin. In systems using the trickle charger, the rechargeable energy source is connected to this pin.
2	2	V_{BAT}	**Battery Input for Any Standard +3V Lithium Cell or Other Energy Source.** If not used, V_{BAT} must be connected to ground. Diodes must not be placed in series between V_{BAT} and the battery, or improper operation will result. UL recognized to ensure against reverse charging current when used in conjunction with a lithium battery. See "Conditions of Acceptability" at www.maxim-ic.com/TechSupport/QA/ntrl.htm.
3	3	X1	**Connections for Standard 32.768kHz Quartz Crystal.** The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. For more information on crystal selection and crystal layout considerations, refer to *Application Note 58*, "Crystal Considerations with Dallas Real-Time Clocks." The DS1306 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
5	4	X2	
7	5	INT0	**Active-Low Interrupt 0 Output.** The INT0 pin is an active-low output of the DS1306 that can be used as an interrupt input to a processor. The INT0 pin can be programmed to be asserted by Alarm 0. The INT0 pin remains low as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is set. The INT0 pin operates when the DS1306 is powered by V_{CC1}, V_{CC2}, or V_{BAT}. The INT0 pin is an open-drain output and requires an external pullup resistor.
8	6	INT1	**Interrupt 1 Output.** The INT1 pin is an active-high output of the DS1306 that can be used as an interrupt input to a processor. The INT1 pin can be programmed to be asserted by Alarm 1. When an alarm condition is present, the INT1 pin generates a 62.5ms active-high pulse. The INT1 pin operates only when the DS1306 is powered by V_{CC2} or V_{BAT}. When active, the INT1 pin is internally pulled up to V_{CC2} or V_{BAT}. When inactive, the INT1 pin is

			internally pulled low.

PIN DESCRIPTION (continued)

PIN		NAME	FUNCTION
TSSOP	DIP		
9	7	1Hz	**1Hz Output.** The 1Hz pin provides a 1Hz square wave output. This output is active when the 1 Hz bit in the control register is a logic 1. Both `INT0` and 1Hz pins are open-drain outputs. The interrupt, 1Hz signal, and the internal clock continue to run regardless of the level of V_{CC} (as long as a power source is present).
10	8	GND	**Ground**
11	9	SERMODE	**Serial Interface Mode.** The SERMODE pin offers the flexibility to choose between two serial interface modes. When connected to GND, standard 3-wire communication is selected. When connected to V_{CC}, SPI communication is selected.
12	10	CE	**Chip Enable.** The chip enable signal must be asserted high during a read or a write for both 3-wire and SPI communication. This pin has an internal 55kΩ pulldown resistor (typical).
14	11	SCLK	**Serial Clock.** SCLK is used to synchronize data movement on the serial interface for either the SPI or 3-wire interface.
15	12	SDI	**Serial Data In.** When SPI communication is selected, the SDI pin is the serial data input for the SPI bus. When 3-wire communication is selected, this pin must be tied to the SDO pin (the SDI and SDO pins function as a single I/O pin when tied together).
16	13	SDO	**Serial Data Out.** When SPI communication is selected, the SDO pin is the serial data output for the SPI bus. When 3-wire communication is selected, this pin must be tied to the SDI pin (the SDI and SDO pins function as a single I/O pin when tied together). V_{CCIF} provides the logic-high level.
17	14	V_{CCIF}	**Interface Logic Power-Supply Input.** The V_{CCIF} pin allows the DS1306 to drive SDO and 32kHz output pins to a level that is compatible with the interface logic, thus allowing an easy interface to 3V logic in mixed supply systems. This pin is physically connected to the source connection of the p-channel transistors in the output buffers of the SDO and 32kHz pins.
18	15	32kHz	**32.768kHz Output.** The 32kHz pin provides a 32.768kHz output. This signal is always present. V_{CCIF} provides the logic-high level.
20	16	V_{CC1}	**Primary Power Supply.** DC power is provided to the device on this pin. V_{CC1} is the primary power supply.
4, 6, 13, 19	—	N.C.	**No Connection**

DESCRIPTION

The DS1306 serial alarm real-time clock (RTC) provides a full binary coded decimal (BCD) clock calendar that is accessed by a simple serial interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. In addition, 96 bytes of NV RAM are provided for data storage.

An interface logic power-supply input pin (V_{CCIF}) allows the DS1306 to drive SDO and 32kHz pins to a level that is compatible with the interface logic. This allows an easy interface to 3V logic in mixed supply systems. The DS1306 offers dual-power supplies as well as a battery-input pin. The dual-power supplies support a programmable trickle charge circuit that allows a rechargeable energy source (such as a super cap or rechargeable battery) to be used for a backup supply. The V_{BAT} pin allows the device to be backed up by a non-rechargeable battery. The DS1306 is fully operational from 2.0V to 5.5V.

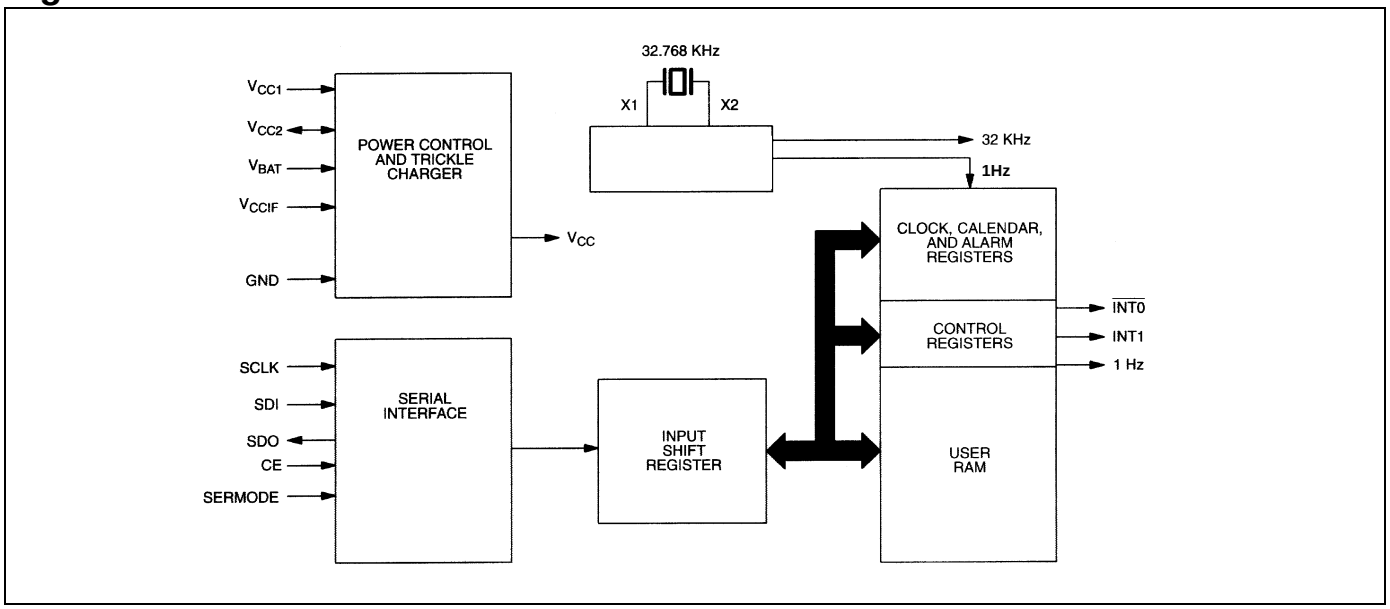
Two programmable time-of-day alarms are provided by the DS1306. Each alarm can generate an interrupt on a programmable combination of seconds, minutes, hours, and day. “Don’t care” states can be inserted into one or more fields if it is desired for them to be ignored for the alarm condition. A 1Hz and a 32kHz clock output are also available.

The DS1306 supports a direct interface to SPI serial data ports or standard 3-wire interface. An easy-to-use address and data format is implemented in which data transfers can occur 1 byte at a time or in multiple-byte burst mode.

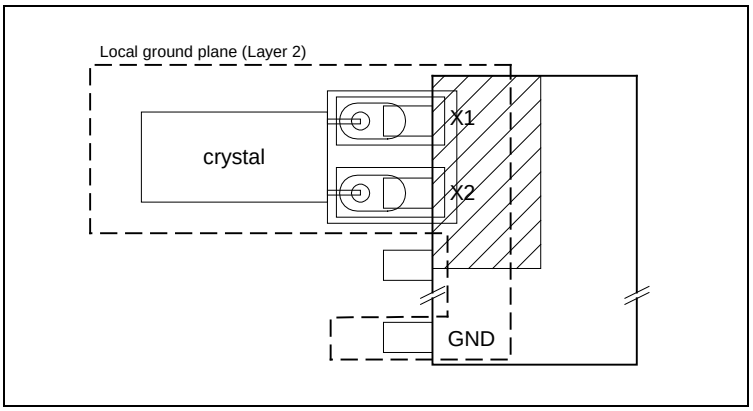
OPERATION

The block diagram in Figure 1 shows the main elements of the serial alarm RTC. The following paragraphs describe the function of each pin.

Figure 1. BLOCK DIAGRAM



RECOMMENDED LAYOUT FOR CRYSTAL



CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks* for detailed information.

Table 1. Crystal Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			45	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

CLOCK, CALENDAR, AND ALARM

The time and calendar information is obtained by reading the appropriate register bytes. The RTC registers are illustrated in Figure 2. The time, calendar, and alarm are set or initialized by writing the appropriate register bytes. Note that some bits are set to 0. These bits always read 0 regardless of how they are written. Also note that registers 12h to 1Fh (read) and registers 92h to 9Fh are reserved. These registers always read 0 regardless of how they are written. The contents of the time, calendar, and alarm registers are in the BCD format.. Values in the day register that correspond to the day of the week are user-defined, but must be sequential (e.g. if 1 equals Sunday, 2 equals Monday and so on). The day register increments at midnight. Illogical time and date entries result in undefined operation.

WRITING TO THE CLOCK REGISTERS

The internal time and date registers continue to increment during write operations. However, the countdown chain is reset when the seconds register is written. Writing the time and date registers within one second after writing the seconds register ensures consistent data.

Terminating a write before the last bit is sent aborts the write for that byte.

READING FROM THE CLOCK REGISTERS

Buffers are used to copy the time and date register at the beginning of a read. When reading in burst mode, the user copy is static while the internal registers continue to increment.

Figure 2. RTC REGISTERS AND ADDRESS MAP

HEX ADDRESS		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	RANGE
READ	WRITE									
00h	80h	0	10 SEC			SEC				00–59
01h	81h	0	10 MIN			MIN				00–59
02h	82h	0	12	P	10-HR	HOURS				01–12 + P/A
				A						
			24	10						00–23
03h	83h	0	0	0	0	0	DAY			01–07
04h	84h	0	0	10-DATE		DATE				1–31
05h	85h	0	0	10-MONTH		MONTH				01–12
06h	86h	10-YEAR				YEAR				00–99
07h	87h	M	10-SEC ALARM 0			SEC ALARM 0				00–59
08h	88h	M	10-MIN ALARM 0			MIN ALARM 0				00–59
09h	89h	M	12	P	10-HR	HOUR ALARM 0				01–12 + P/A
				A						
			24	10						00–23
0Ah	8Ah	M	0	0	0	0	DAY ALARM 0			01–07
0Bh	8Bh	M	10 SEC ALARM 1			SEC ALARM 1				00–59
0Ch	8Ch	M	10 MIN ALARM 1			MIN ALARM 1				00–59
0Dh	8Dh	M	12	P	10-HR	HOUR ALARM 1				01–12 + P/A
				A						
			24	10						00–23
0Eh	8Eh	M	0	0	0	0	DAY ALARM 1			01–07
—										
0Fh	8Fh	CONTROL REGISTER								—
10h	90h	STATUS REGISTER								—
11h	91h	TRICKLE CHARGER REGISTER								—
12h–1Fh	92h–9Fh	RESERVED								—
20h–7Fh	A0h–FFh	96-BYTES USER RAM								—

Note: *Range for alarm registers does not include mask'm' bits.*

The DS1306 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic-high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 to 23 hours).

The DS1306 contains two time-of-day alarms. Time-of-day alarm 0 can be set by writing to registers 87h to 8Ah. Time-of-day Alarm 1 can be set by writing to registers 8Bh to 8Eh. Bit 7 of each of the time-of-day alarm registers are mask bits (Table 2). When all of the mask bits are logic 0, a time-of-day alarm only occurs once per week when the values stored in timekeeping registers 00h to 03h match the values stored in the time-of-day alarm registers. An alarm is generated every day when bit 7 of the day alarm register is set to a logic 1. An alarm is generated every hour when bit 7 of the day and hour alarm

registers is set to a logic 1. Similarly, an alarm is generated every minute when bit 7 of the day, hour, and minute alarm registers is set to a logic 1. When bit 7 of the day, hour, minute, and seconds alarm registers is set to a logic 1, an alarm occurs every second.

During each clock update, the RTC compares the Alarm 0 and Alarm 1 registers with the corresponding clock registers. When a match occurs, the corresponding alarm flag bit in the status register is set to a 1. If the corresponding alarm interrupt enable bit is enabled, an interrupt output is activated.

Table 2. TIME-OF-DAY ALARM MASK BITS

ALARM REGISTER MASK BITS (BIT 7)				FUNCTION
SECONDS	MINUTES	HOURS	DAYS	
1	1	1	1	Alarm once per second
0	1	1	1	Alarm when seconds match
0	0	1	1	Alarm when minutes and seconds match
0	0	0	1	Alarm hours, minutes, and seconds match
0	0	0	0	Alarm day, hours, minutes and seconds match

SPECIAL PURPOSE REGISTERS

The DS1306 has three additional registers (control register, status register, and trickle charger register) that control the real-time clock, interrupts, and trickle charger.

CONTROL REGISTER (READ 0Fh, WRITE 8Fh)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	WP	0	0	0	1Hz	AIE1	AIE0

WP (Write Protect) – Before any write operation to the clock or RAM, this bit must be logic 0. When high, the write protect bit prevents a write operation to any register, including bits 0, 1, and 2 of the control register. Upon initial power-up, the state of the WP bit is undefined. Therefore, the WP bit should be cleared before attempting to write to the device. When WP is set, it must be cleared before any other control register bit can be written.

1Hz (1Hz Output Enable) – This bit controls the 1Hz output. When this bit is a logic 1, the 1Hz output is enabled. When this bit is a logic 0, the 1Hz output is high-Z.

AIE0 (Alarm Interrupt Enable 0) – When set to a logic 1, this bit permits the interrupt 0 request flag (IRQF0) bit in the status register to assert $\overline{\text{INT0}}$. When the AIE0 bit is set to logic 0, the IRQF0 bit does not initiate the $\overline{\text{INT0}}$ signal.

AIE1 (Alarm Interrupt Enable 1) – When set to a logic 1, this bit permits the interrupt 1 request flag (IRQF1) bit in the status register to assert INT1. When the AIE1 bit is set to logic 0, the IRQF1 bit does not initiate an interrupt signal, and the INT1 pin is set to a logic 0 state.

STATUS REGISTER (READ 10H)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	0	0	0	0	0	IRQF1	IRQF0

IRQF0 (Interrupt 0 Request Flag) – A logic 1 in the interrupt request flag bit indicates that the current time has matched the Alarm 0 registers. If the AIE0 bit is also a logic 1, the $\overline{INT0}$ pin goes low. IRQF0 is cleared when the address pointer goes to any of the Alarm 0 registers during a read or write. IRQF0 is activated when the device is powered by V_{CC1}, V_{CC2}, or V_{BAT}.

IRQF1 (Interrupt 1 Request Flag) – A logic 1 in the interrupt request flag bit indicates that the current time has matched the Alarm 1 registers. If the AIE1 bit is also a logic 1, the INT1 pin generates a 62.5ms active-high pulse. IRQF1 is cleared when the address pointer goes to any of the alarm 1 registers during a read or write. IRQF1 is activated only when the device is powered by V_{CC2} or V_{BAT}.

TRICKLE CHARGE REGISTER (READ 11H, WRITE 91H)

This register controls the trickle charge characteristics of the DS1306. The simplified schematic of Figure 3 shows the basic components of the trickle charger. The trickle charge select (TCS) bits (bits 4–7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 enables the trickle charger. All other patterns disable the trickle charger. The DS1306 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2–3) select whether one diode or two diodes are connected between V_{CC1} and V_{CC2}. The diode select (DS) bits (bits 2–3) select whether one diode or two diodes are connected between V_{CC1} and V_{CC2}. The resistor select (RS) bits select the resistor that is connected between V_{CC1} and V_{CC2}. The resistor and diodes are selected by the RS and DS bits as shown in Table 3.

Figure 3. PROGRAMMABLE TRICKLE CHARGER

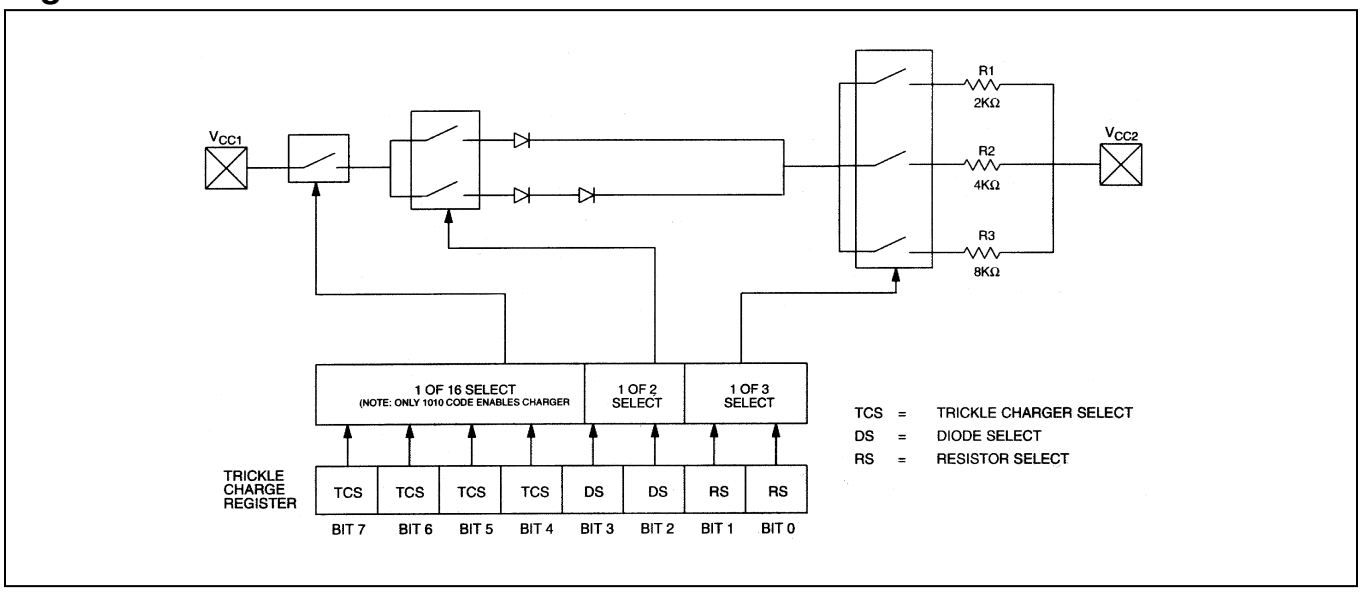


Table 3. TRICKLE CHARGER RESISTOR AND DIODE SELECT

TCS Bit 7	TCS Bit 6	TCS Bit 5	TCS Bit 4	DS Bit 3	DS Bit 2	RS Bit 1	RS Bit 0	FUNCTION
X	X	X	X	X	X	0	0	Disabled
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
1	0	1	0	0	1	0	1	1 Diode, 2kΩ
1	0	1	0	0	1	1	0	1 Diode, 4kΩ
1	0	1	0	0	1	1	1	1 Diode, 8kΩ
1	0	1	0	1	0	0	1	2 Diodes, 2kΩ
1	0	1	0	1	0	1	0	2 Diodes, 4kΩ
1	0	1	0	1	0	1	1	2 Diodes, 8kΩ
0	1	0	1	1	1	0	0	Initial power-on state

If RS is 00, the trickle charger is disabled independently of TCS.

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to V_{CC1} and a super cap is connected to V_{CC2}. Also assume that the trickle charger has been enabled with one diode and resister R1 between V_{CC1} and V_{CC2}. The maximum current I_{MAX} would, therefore, be calculated as follows:

$$I_{MAX} = (5.0V - \text{diode drop}) / R1 \approx (5.0V - 0.7V) / 2k\Omega \approx 2.2mA$$

As the super cap charges, the voltage drop between V_{CC1} and V_{CC2} decreases and, therefore, the charge current decreases.

POWER CONTROL

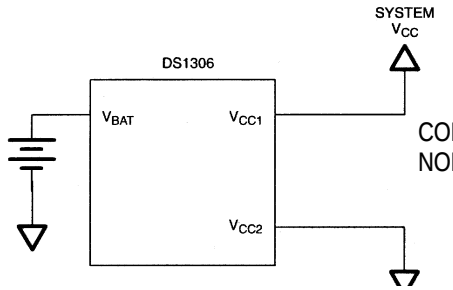
Power is provided through the V_{CC1}, V_{CC2}, and V_{BAT} pins. Three different power supply configurations are illustrated in Figure 4. Configuration 1 shows the DS1306 being backed up by a non-rechargeable energy source such as a lithium battery. In this configuration, the system power supply is connected to V_{CC1} and V_{CC2} is grounded. When V_{CC} falls below V_{BAT} the device switches into a low-current battery backup mode. Upon power-up, the device switches from V_{BAT} to V_{CC} when V_{CC} is greater than V_{BAT} + 0.2V. The device is write-protected whenever it is switched to V_{BAT}.

Configuration 2 illustrates the DS1306 being backed up by a rechargeable energy source. In this case, the V_{BAT} pin is grounded, V_{CC1} is connected to the primary power supply, and V_{CC2} is connected to the secondary supply (the rechargeable energy source). The DS1306 operates from the larger of V_{CC1} or V_{CC2}. When V_{CC1} is greater than V_{CC2} + 0.2V (typical), V_{CC1} powers the DS1306. When V_{CC1} is less than V_{CC2}, V_{CC2} powers the DS1306. The DS1306 does not write-protect itself in this configuration.

Configuration 3 shows the DS1306 in battery-operate mode, where the device is powered only by a single battery. In this case, the V_{CC1} and V_{BAT} pins are grounded and the battery is connected to the V_{CC2} pin.

Only these three configurations are allowed. Unused supply pins must be grounded.

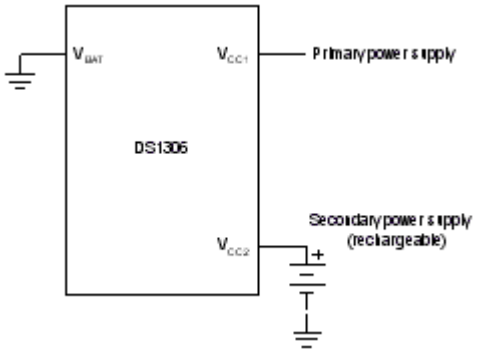
Figure 4. POWER-SUPPLY CONFIGURATIONS



CONFIGURATION 1: BACKUP SUPPLY IS NONRECHARGEABLE LITHIUM BATTERY

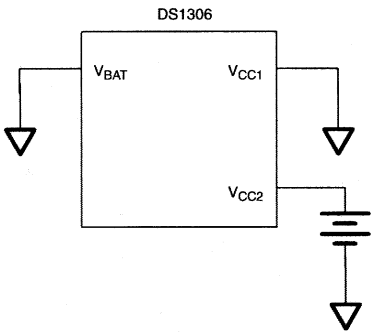
NOTE: DEVICE IS WRITE-PROTECTED IF $V_{CC} < V_{CCTP}$.

CONFIGURATION 2: BACKUP SUPPLY IS A RECHARGEABLE BATTERY OR SUPER CAPACITOR



NOTE: DEVICE DOES NOT PROVIDE AUTOMATIC WRITE PROTECTION.

CONFIGURATION 3: BATTERY OPERATE MODE



SERIAL INTERFACE

The DS1306 offers the flexibility to choose between two serial interface modes. The DS1306 can communicate with the SPI interface or with a standard 3-wire interface. The interface method used is determined by the SERMODE pin. When this pin is connected to V_{CC}, SPI communication is selected. When this pin is connected to ground, standard 3-wire communication is selected.

SERIAL PERIPHERAL INTERFACE (SPI)

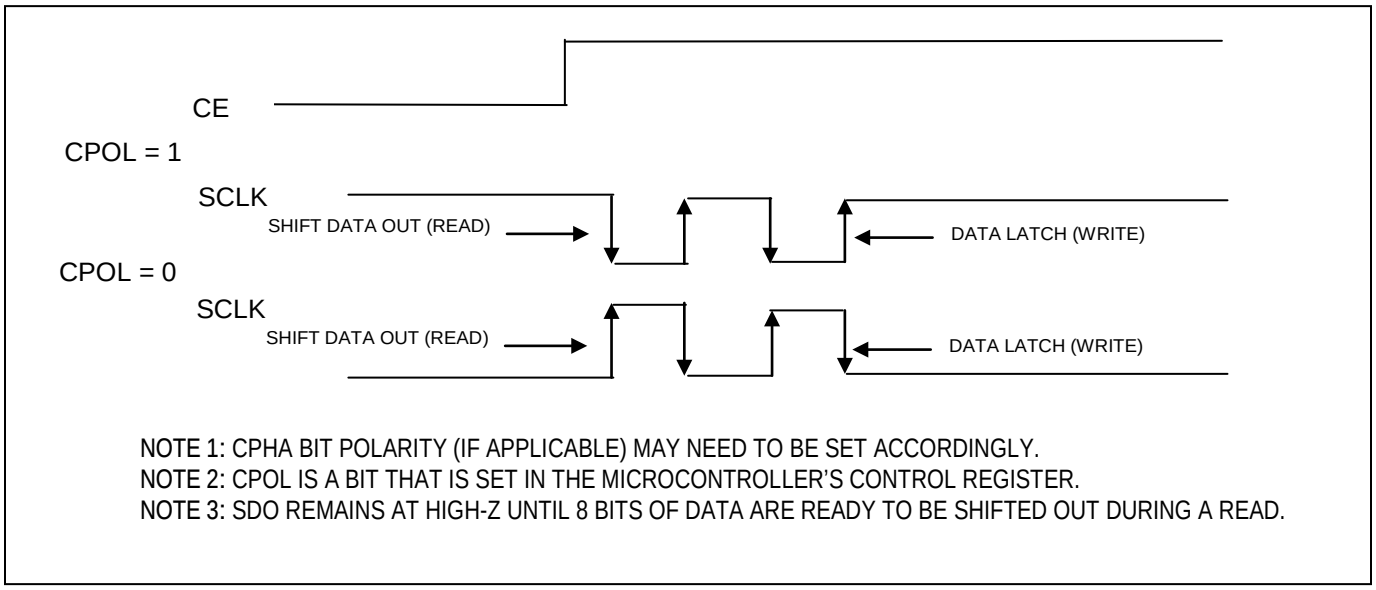
The serial peripheral interface (SPI) is a synchronous bus for address and data transfer and is used when interfacing with the SPI bus on specific Motorola microcontrollers such as the 68HC05C4 and the 68HC11A8. The SPI mode of serial communication is selected by tying the SERMODE pin to V_{CC}.

Four pins are used for the SPI. The four pins are the SDO (serial data out), SDI (serial data in), CE (chip enable), and SCLK (serial clock). The DS1306 is the slave device in an SPI application, with the microcontroller being the master.

The SDI and SDO pins are the serial data input and output pins for the DS1306, respectively. The CE input is used to initiate and terminate a data transfer. The SCLK pin is used to synchronize data movement between the master (microcontroller) and the slave (DS1306) devices.

The shift clock (SCLK), which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus. The inactive clock polarity is programmable in some microcontrollers. The DS1306 determines on the clock polarity by sampling SCLK when CE becomes active. Therefore either SCLK polarity can be accommodated. Input data (SDI) is latched on the internal strobe edge and output data (SDO) is shifted out on the shift edge (Figure 5). There is one clock for each bit transferred. Address and data bits are transferred in groups of eight, MSB first.

Figure 5. SERIAL CLOCK AS A FUNCTION OF MICROCONTROLLER CLOCK POLARITY (CPOL)



NOTE 1: CPHA BIT POLARITY (IF APPLICABLE) MAY NEED TO BE SET ACCORDINGLY.
NOTE 2: CPOL IS A BIT THAT IS SET IN THE MICROCONTROLLER'S CONTROL REGISTER.
NOTE 3: SDO REMAINS AT HIGH-Z UNTIL 8 BITS OF DATA ARE READY TO BE SHIFTED OUT DURING A READ.

ADDRESS AND DATA BYTES

Address and data bytes are shifted MSB first into the serial data input (SDI) and out of the serial data output (SDO). Any transfer requires the address of the byte to specify a write or read to either a RTC or RAM location, followed by one or more bytes of data. Data is transferred out of the SDO for a read operation and into the SDI for a write operation (Figures 6 and 7).

Figure 6. SPI SINGLE-BYTE WRITE

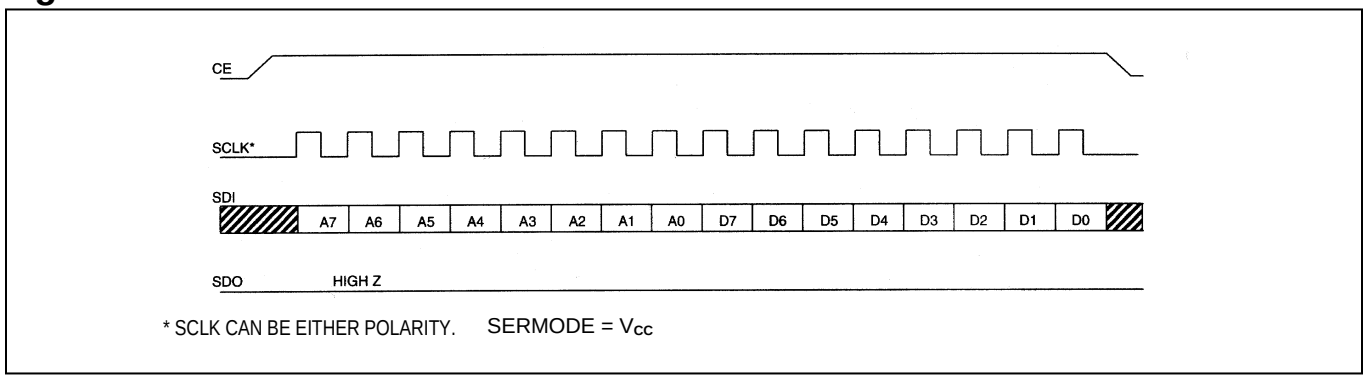
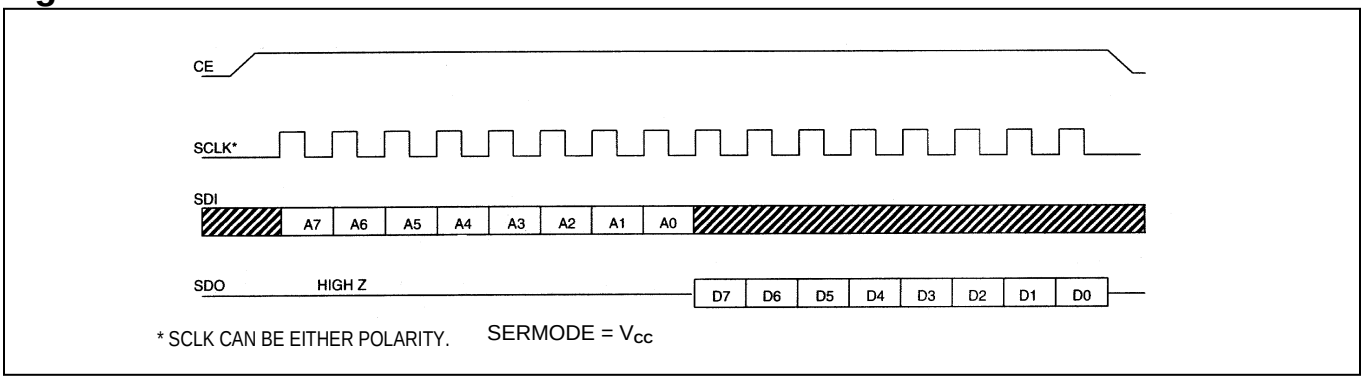


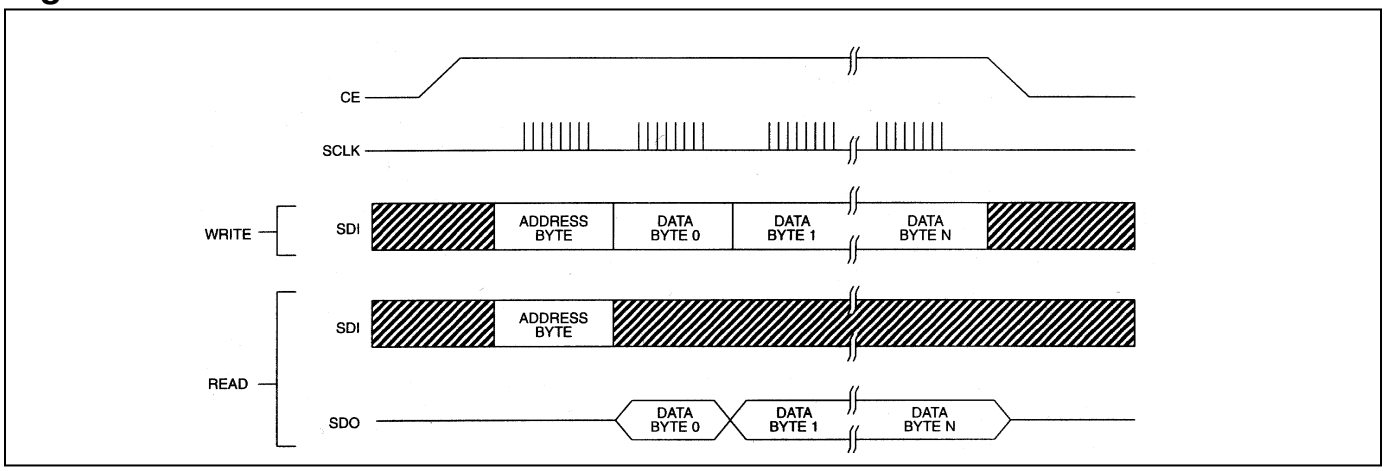
Figure 7. SPI SINGLE-BYTE READ



The address byte is always the first byte entered after CE is driven high. The most significant bit (A7) of this byte determines if a read or write takes place. If A7 is 0, one or more read cycles occur. If A7 is 1, one or more write cycles occur.

Data transfers can occur one byte at a time or in multiple-byte burst mode. After CE is driven high an address is written to the DS1306. After the address, 1 or more data bytes can be written or read. For a single-byte transfer, one byte is read or written and then CE is driven low. For a multiple-byte transfer, however, multiple bytes can be read or written to the DS1306 after the address has been written. Each read or write cycle causes the RTC register or RAM address to automatically increment. Incrementing continues until the device is disabled. When the RTC is selected, the address wraps to 00h after incrementing to 1Fh (during a read) and wraps to 80h after incrementing to 9Fh (during a write). When the RAM is selected, the address wraps to 20h after incrementing to 7Fh (during a read) and wraps to A0h after incrementing to FFh (during a write).

Figure 8. SPI MULTIPLE-BYTE BURST TRANSFER



READING AND WRITING IN BURST MODE

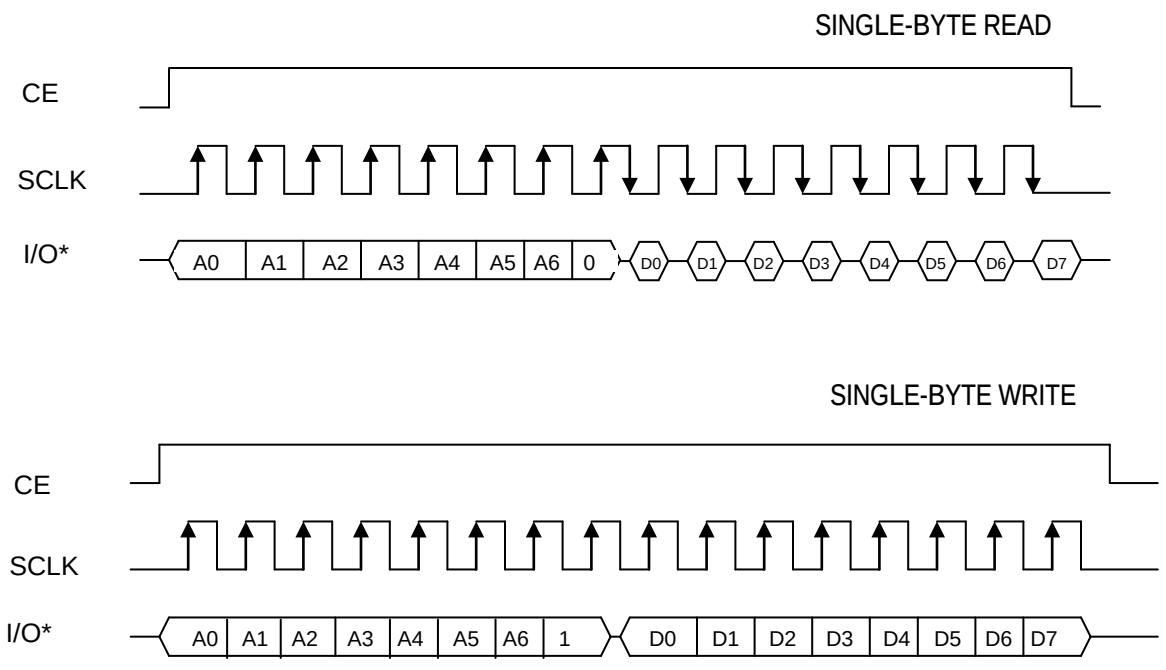
Burst mode is similar to a single-byte read or write, except that CE is kept high and additional SCLK cycles are sent until the end of the burst. The clock registers and the user RAM may be read or written in burst mode. When accessing the clock registers in burst mode, the address pointer will wrap around after reaching 1Fh (9Fh for writes). When accessing the user RAM in burst mode, the address pointer wraps around after reaching 7Fh (FFh for writes).

3-WIRE INTERFACE

The 3-wire interface mode operates similar to the SPI mode. However, in 3-wire mode there is one I/O instead of separate data in and data out signals. The 3-wire interface consists of the I/O (SDI and SDO pins tied together), CE, and SCLK pins. In 3-wire mode, each byte is shifted in LSB first, unlike SPI mode, where each byte is shifted in MSB first.

As is the case with the SPI mode, an address byte is written to the device followed by a single data byte or multiple data bytes. Figure 9 illustrates a read and write cycle. In 3-wire mode, data is input on the rising edge of SCLK and output on the falling edge of SCLK.

Figure 9. 3-WIRE SINGLE BYTE TRANSFER



NOTE: IN BURST MODE, CE IS KEPT HIGH AND ADDITIONAL SCLK CYCLES ARE SENT UNTIL THE END OF THE BURST.
**I/O IS SDI AND SDO TIED TOGETHER.*
SERMODE = GND

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.5V to +7.0V
Storage Temperature Range…….-55°C to +125°C
Soldering Temperature…….Refer to the IPC/JEDEC Standard J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

OPERATING RANGE

RANGE	TEMP RANGE	V_{CC} (V)
Commercial	0°C to +70°C	2.0 to 5.5 V_{CC1} or V_{CC2}
Industrial	-40°C to +85°C	2.0 to 5.5 V_{CC1} or V_{CC2}

RECOMMENDED DC OPERATING CONDITIONS

(T_A = Over the operating range, unless otherwise specified.)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Supply Voltage V_{CC1}, V_{CC2}	V_{CC1}, V_{CC2}		2.0		5.5	V	1, 8
Logic 1 Input	V_{IH}		2.0		V_{CC} + 0.3	V	
Logic 0 Input	V_{IL}	V_{CC} = 2.0V	-0.3		+0.3	V	
		V_{CC} = 5V			+0.8		
V_{BAT} Battery Voltage	V_{BAT}		2.0		5.5	V	
V_{CCIF} Supply Voltage	V_{CCIF}		2.0		5.5	V	10

DC ELECTRICAL CHARACTERISTICS

(T_A = Over the operating range, unless otherwise specified.)

PARAMETER		SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Input Leakage		I_{LI}		-100		+500	µA	
Output Leakage		I_{LO}		-1		+1	µA	
Logic 0 Output	I_{OL} = 1.5mA	V_{OL}	V_{CC} = 2.0			0.4	V	
	I_{OL} = 4.0mA		V_{CC} = 5V			0.4		
Logic 1 Output	I_{OH} = -0.4mA	V_{OH}	V_{CCIF} = 2.0V	1.6			V	
	I_{OH} = -1.0mA		V_{CCIF} = 5V	2.4				
Logic 1 Output Current (INT1 pin)		I_{OH}, INT1	(V_{CC2}, V_{BAT}) -0.3V	-100			µA	
V_{CC1} Active Supply Current		I_{CC1A}	V_{CC1} = 2.0V			0.425	mA	2, 7
			V_{CC1} = 5V			1.28		
V_{CC1} Timekeeping Current		I_{CC1T}	V_{CC1} = 2.0V			25.3	µA	1, 7
			V_{CC1} = 5V			81		
V_{CC2} Active Supply Current		I_{CC2A}	V_{CC2} = 2.0V			0.4	mA	2, 8
			V_{CC2} = 5V			1.2		
V_{CC2} Timekeeping Current		I_{CC2T}	V_{CC2} = 2.0V			0.4	µA	1, 8
			V_{CC2} = 5V			1		
Battery Timekeeping Current		I_{BAT}	V_{BAT} = 3V			550	nA	9
Battery Timekeeping Current (IND)		I_{BAT}	V_{BAT} = 3V			800	nA	9
V_{CC} Trip Point		V_{CCTP}		V_{BAT} - 50		V_{BAT} + 200	mV	
Trickle Charge Resistors		R1			2		kΩ	
		R2			4			
		R3			8			
Trickle Charger Diode Voltage Drop		V_{TD}			0.7		V	

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		10		pF	
Output Capacitance	C_O		15		pF	

3-WIRE AC ELECTRICAL CHARACTERISTICS

(T_A = Over the operating range, unless otherwise specified.) (Figure 10 and Figure 11)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	V_{CC} = 2.0V	200			ns	3, 4
		V_{CC} = 5V	50				
CLK to Data Hold	t_{CDH}	V_{CC} = 2.0V	280			ns	3, 4
		V_{CC} = 5V	70				
CLK to Data Delay	t_{CDD}	V_{CC} = 2.0V			800	ns	3, 4, 5
		V_{CC} = 5V			200		
CLK Low Time	t_{CL}	V_{CC} = 2.0V	1000			ns	4
		V_{CC} = 5V	250				
CLK High Time	t_{CH}	V_{CC} = 2.0V	1000			ns	4
		V_{CC} = 5V	250				
CLK Frequency	t_{CLK}	V_{CC} = 2.0V			0.6	MHz	4
		V_{CC} = 5V	DC		2.0		
CLK Rise and Fall	t_R, t_F	V_{CC} = 2.0V			2000	ns	
		V_{CC} = 5V			500		
CE to CLK Setup	t_{CC}	V_{CC} = 2.0V	4			µs	4
		V_{CC} = 5V	1				
CLK to CE Hold	t_{CCH}	V_{CC} = 2.0V	240			ns	4
		V_{CC} = 5V	60				
CE Inactive Time	t_{CWH}	V_{CC} = 2.0V	4			µs	4
		V_{CC} = 5V	1				
CE to Output High-Z	t_{CDZ}	V_{CC} = 2.0V			280	ns	3, 4
		V_{CC} = 5V			70		
SCLK to Output High-Z	t_{CCZ}	V_{CC} = 2.0V			280	ns	3, 4
		V_{CC} = 5V			70		

Figure 10. TIMING DIAGRAM: 3-WIRE READ DATA TRANSFER

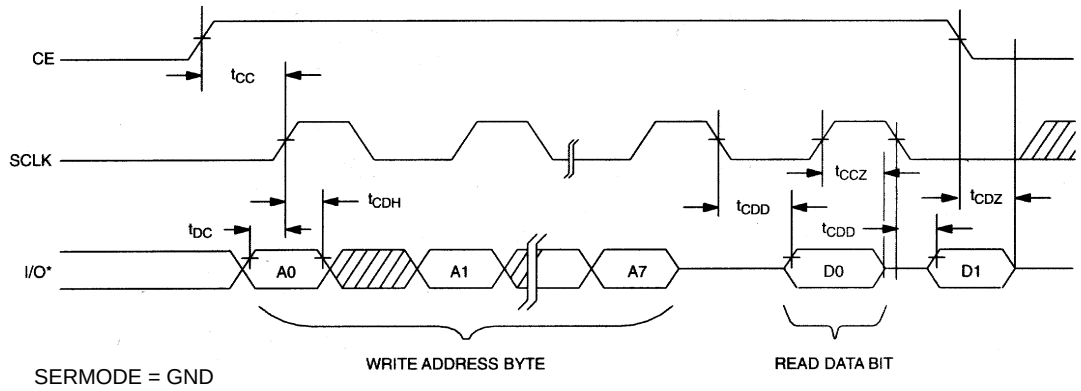
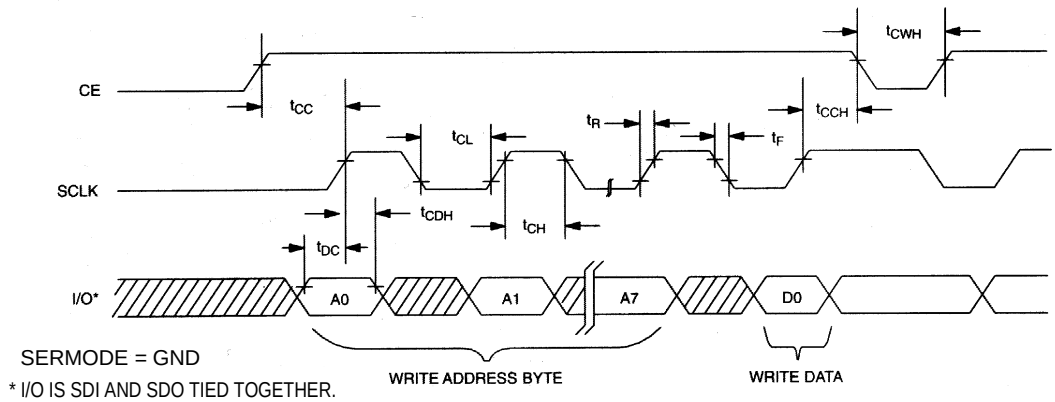


Figure 11. TIMING DIAGRAM: 3-WIRE WRITE DATA TRANSFER

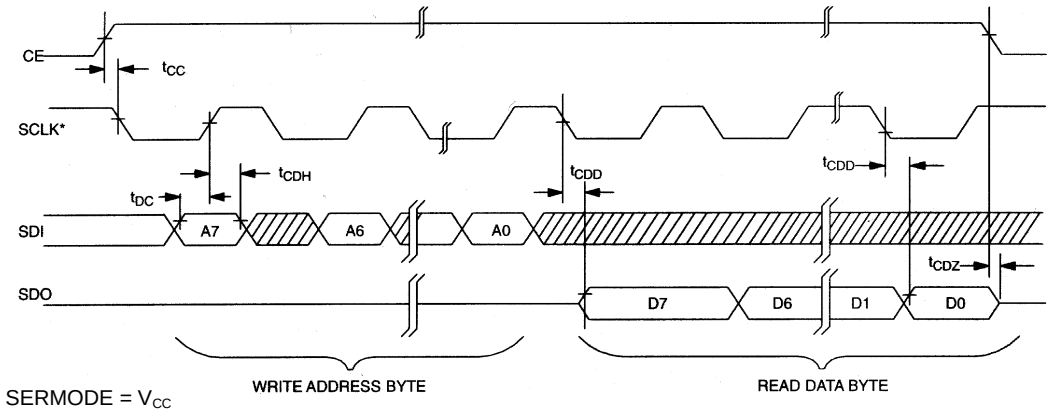


SPI AC ELECTRICAL CHARACTERISTICS

(T_A = Over the operating range, unless otherwise specified.)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	V_{CC} = 2.0V	200			ns	3, 4
		V_{CC} = 5V	50				
CLK to Data Hold	t_{CDH}	V_{CC} = 2.0V	280			ns	3, 4
		V_{CC} = 5V	70				
CLK to Data Delay	t_{CDD}	V_{CC} = 2.0V			800	ns	3, 4, 5
		V_{CC} = 5V			200		
CLK Low Time	t_{CL}	V_{CC} = 2.0V	1000			ns	4
		V_{CC} = 5V	250				
CLK High Time	t_{CH}	V_{CC} = 2.0V	1000			ns	4
		V_{CC} = 5V	250				
CLK Frequency	t_{CLK}	V_{CC} = 2.0V			0.6	MHz	4
		V_{CC} = 5V	DC		2.0		
CLK Rise and Fall	t_R, t_F	V_{CC} = 2.0V			2000	ns	
		V_{CC} = 5V			500		
CE to CLK Setup	t_{CC}	V_{CC} = 2.0V	4			µs	4
		V_{CC} = 5V	1				
CLK to CE Hold	t_{CCH}	V_{CC} = 2.0V	240			ns	4
		V_{CC} = 5V	60				
CE Inactive Time	t_{CWH}	V_{CC} = 2.0V	4			µs	4
		V_{CC} = 5V	1				
CE to Output High-Z	t_{CDZ}	V_{CC} = 2.0V			280	ns	3, 4
		V_{CC} = 5V			70		

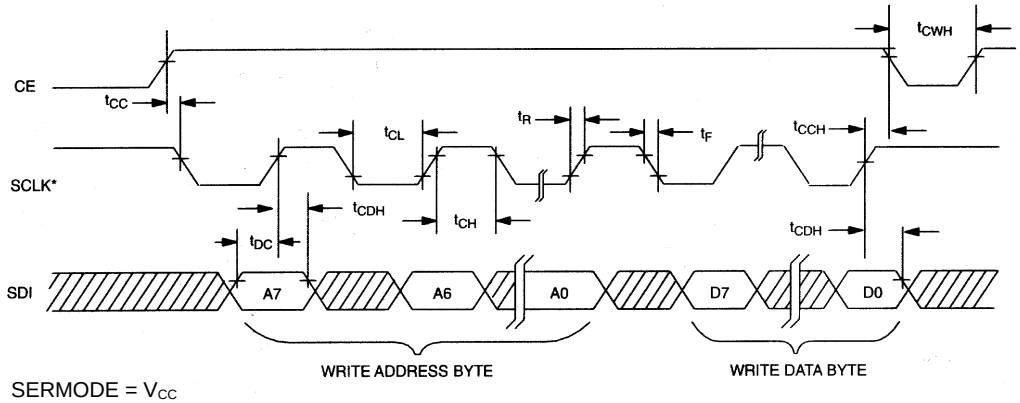
Figure 12. TIMING DIAGRAM: SPI READ DATA TRANSFER



SERMODE = V_{CC}

* SCLK CAN BE EITHER POLARITY, TIMING SHOWN FOR CPOL = 1.

Figure 13. TIMING DIAGRAM: SPI WRITE DATA TRANSFER



SERMODE = V_{CC}

* SCLK CAN BE EITHER POLARITY, TIMING SHOWN FOR CPOL = 1.

NOTES:

1) I_{CC1T} and I_{CC2T} are specified with CE set to a logic 0.
2) I_{CC1A} and I_{CC2A} are specified with CE = V_{CC}, SCLK = 2MHz at V_{CC} = 5V; SCLK = 500kHz at V_{CC} = 2.0V, V_{IL} = 0V, V_{IH} = V_{CC}.
3) Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ms maximum rise and fall time.
4) Measured with 50pF load.
5) Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
6) V_{CC} = V_{CC1}, when V_{CC1} > V_{CC2} + 0.2V (typical); V_{CC} = V_{CC2}, when V_{CC2} > V_{CC1}.
7) V_{CC2} = 0V.
8) V_{CC1} = 0V.
9) V_{CC1} < V_{BAT}.
10) V_{CCIF} must be less than or equal to the largest of V_{CC1}, V_{CC2}, and V_{BAT}.

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 PDIP	P16+1	**21-0043**
20 TSSOP	U20+1	**21-0066**

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
12/09	Added *Table 1. Crystal Specifications* to the *Clock Accuracy* section.	5
	Added "SERMODE = V_{CC}" to Figures 6, 7, 12, and 13.	12, 20
	Added "SERMODE = GND" to Figures 9, 10, and 11.	14, 18
	Removed the "Crystal Capacitance" parameter from the *Capacitance* table.	16
4/15	Revised *Benefits and Features* section	1

Maxim Integrated Products, 160 Rio Robles, San Jose, CA 95134 408-601-1000