

# **Maximum Ratings** (@ $T_A = +25^{\circ}C$ , unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Operating Supply Voltage	V <sub>P</sub> - V <sub>N</sub>	6.0	V	
DC Voltage at any Channel Input	_	$(V_N - 0.5)$ to $(V_P + 0.5)$	V	_
Peak Pulse Current	IPP	5	Α	8/20μs, Per Figure 3
ESD Protection – Contact Discharge	V <sub>ESD_Contact</sub>	±8	kV	Standard IEC 61000-4-2
ESD Protection – Air Discharge	$V_{ESD\_Air}$	±15	kV	Standard IEC 61000-4-2

### **Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	$P_{D}$	400	mW
Thermal Resistance, Junction to Ambient (Note 5)	$R_{ heta JA}$	310	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-65 to +150	°C

### Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Conditions
Operating Supply Voltage	$V_P$	_	3.3	5.5	V	_
Operating Supply Current (Note 6)	l <sub>P</sub>	_	_	8.0	μΑ	$(V_P - V_N) = 3.3V$
Channel Leakage Current (Note 6)	$I_R$	_	±0.1	±1.0	μΑ	$V_P = 5V$ , $V_N = 0V$
Reverse breakdown voltage	$V_{BR}$	6.0	_	_	V	$I_R = 1mA$
Clamping Voltage, Positive Transients	V <sub>CL1</sub>	_	10.0	_	V	$I_{PP} = 1A, t_p = 8/20\mu s$
Clamping Voltage, Negative Transients	V <sub>CL2</sub>	_	-1.7	_	V	$I_{PP} = -1A$ , $t_p = 8/20 \mu s$
Forward Voltage for Top Diode	V <sub>FD1</sub>	0.60	0.80	0.95	V	$I_F$ = 8mA, CH1 to $V_P$ or CH2 to $V_P$
Forward Voltage for Bottom Diode	$V_{FD2}$	0.60	0.80	0.95	V	$I_F = 8mA$ , $V_N$ to CH1 or $V_N$ to CH2
Dynamic Resistance	$R_{DYN}$	_	0.9	_	Ω	$I_{PP} = 1A, t_p = 8/20\mu s$
Channel Input Capacitance	C <sub>T</sub>	_	0.85	1.2	pF	$V_{IN} = 1.65V, V_P = 3.3V,$ $V_N = 0V, f = 1MHz$

Notes:

- 5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes, Inc. suggested pad layout AP02001, which can be found on our website at http://www.diodes.com.

  Short duration pulse test used to minimize self-heating effect.

  Measured from CH1 to VN or CH2 to VN.

- 8. Measured from  $\ensuremath{V_P}$  to  $\ensuremath{V_N}.$
- 9. For information on the impact of Diodes' USB 2.0 compatible ESD protectors on signal integrity including eye diagram plots, please refer to AN77 at the following URL: http://www.diodes.com/destools/appnote\_dnote.html.



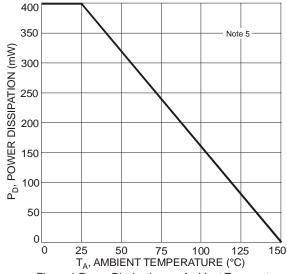
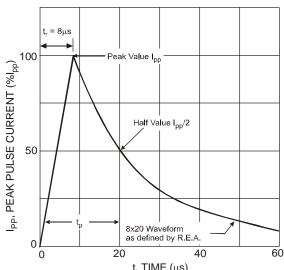
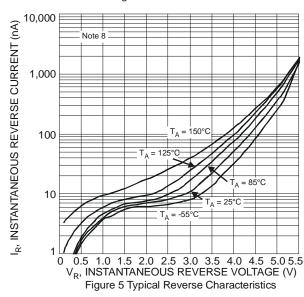
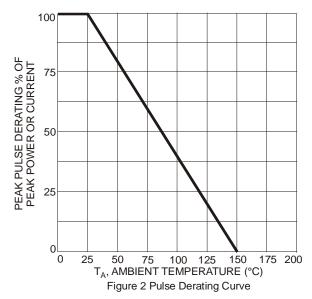


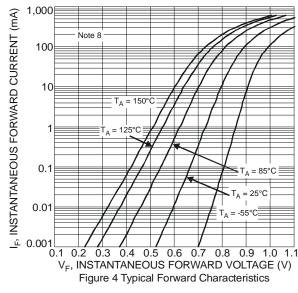
Figure 1 Power Dissipation vs. Ambient Temperature



t, TIME ( $\mu$ s) Figure 3 Pulse Waveform







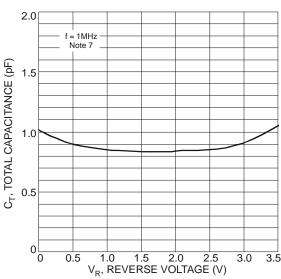
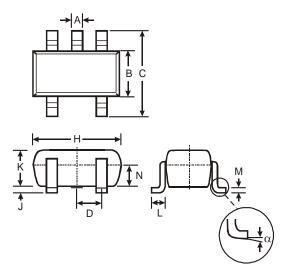


Figure 6 Typical Total Capacitance vs. Reverse Voltage



## **Package Outline Dimensions**

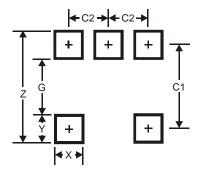
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SOT25					
Dim	Min	Max	Тур		
Α	0.35	0.50	0.38		
В	1.50	1.70	1.60		
С	2.70	3.00	2.80		
D	_		0.95		
Н	2.90	3.10	3.00		
J	0.013	0.10	0.05		
K	1.00	1.30	1.10		
L	0.35	0.55	0.40		
M	0.10	0.20	0.15		
N	0.70	0.80	0.75		
α	0°	8°	_		
All Dimensions in mm					

# **Suggested Pad Layout**

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	3.20
G	1.60
Х	0.55
Y	0.80
C1	2.40
C2	0.95



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