Contents

Pin Configuration

Figure 1. 32-pin STSOP pinout [1]

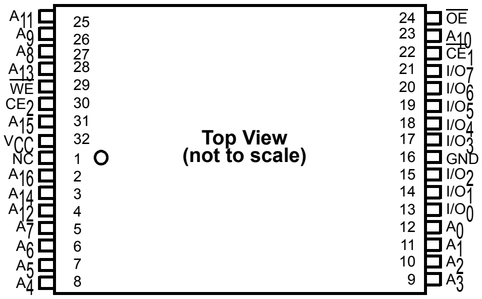


Figure 2. 32-pin TSOP I pinout [1]

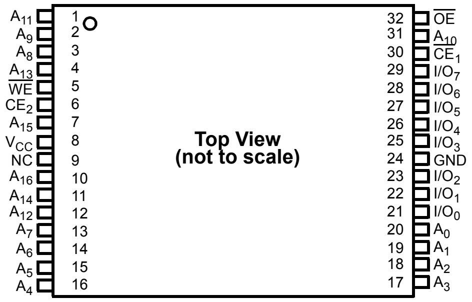
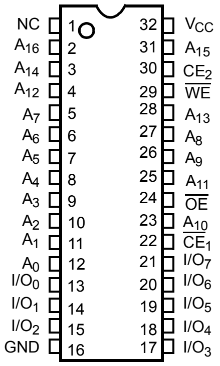


Figure 3. 32-pin SOIC pinout [1]

Top View



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62128EV30LL	Industrial	2.2	3.0	3.6	45	1.3	2.0	11	16	1	4

Notes

1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature
with power applied .... –55 °C to +125 °C

Supply voltage
to ground potential [3, 4] ....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs
in high Z State [3, 4] ....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage [3, 4] ....–0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) .... 20 mA

Static discharge voltage
(MIL-STD-883, method 3015) ....> 2001 V

Latch-up current ....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62128EV30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns (Industrial)			Unit
				Min	Typ [6]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA		2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA		–	–	0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70 V		–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3 V	V
		V_{CC}= 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3 V	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND $\leq V_I \leq V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	GND $\leq V_O \leq V_{CC}$, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = 1/t_{RC}	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels	–	11	16	mA
		f = 1 MHz		–	1.3	2.0	mA
I_{SB1}[7]	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC}$ – 0.2 V, CE_2 < 0.2 V $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V f = f_{max} (address and data only), f = 0 ($\overline{OE}$ and $\overline{WE}$), V_{CC} = 3.60 V		–	1	4	µA
I_{SB2}[7]	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1 \geq V_{CC}$ – 0.2 V, CE_2 < 0.2 V $V_{IN} \geq V_{CC}$ – 0.2 V or V_{IN} < 0.2 V, f = 0, V_{CC} = 3.60 V		–	1	4	µA

Notes

3. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. Full device AC operation assumes a 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
7. Chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	32-pin TSOP I	32-pin SOIC	32-pin STSOP	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	33.01	48.67	32.56	°C/W
Θ_{JC}	Thermal resistance (junction to case)		3.42	25.86	3.59	°C/W

AC Test Loads and Waveforms

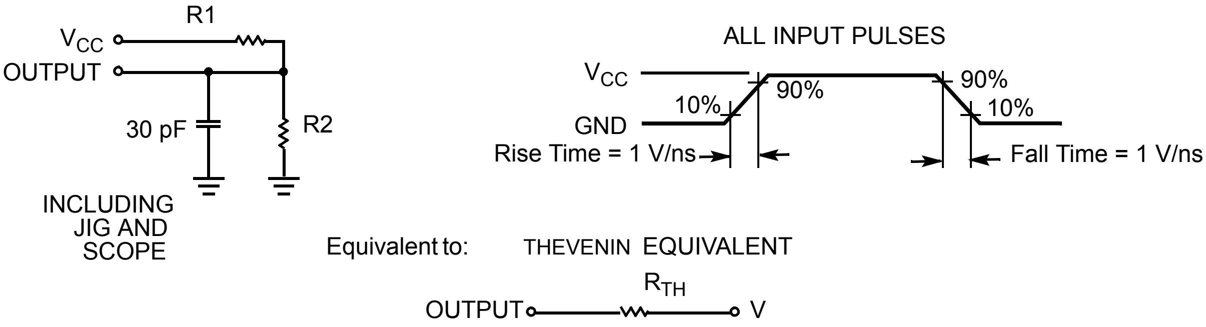


Figure 4. AC Test Loads and Waveforms

Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note

8. Tested initially and after any design or process changes that may affect these parameters.

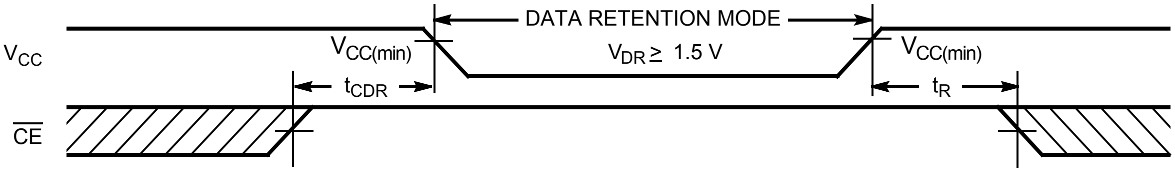
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR}[10]	Data retention current	V_{CC} = 1.5 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial	–	–	3	µA
t_{CDR}[11]	Chip deselect to data retention time			0	–	–	ns
t_R[12]	Operation recovery time			45	–	–	ns

Data Retention Waveform

Figure 5. Data Retention Waveform [13]



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq$ 100 µs or stable at $V_{CC(min)} \geq$ 100 µs.
13. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	45 ns (Industrial)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [16]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [16, 17]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	ns
Write Cycle [18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [16]	10	–	ns

Notes

[14] $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

[15] Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 4 on page 5.

[16] At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.

[17] t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.

[18] The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

[19] The minimum write pulse width for WRITE Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 6. Read Cycle 1 (Address Transition Controlled) [21, 22]

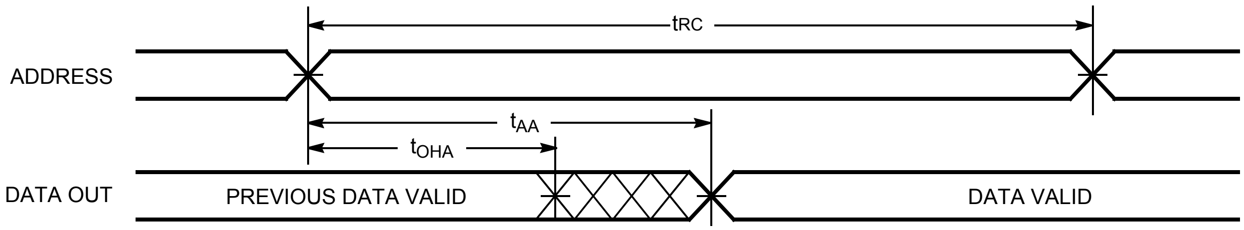
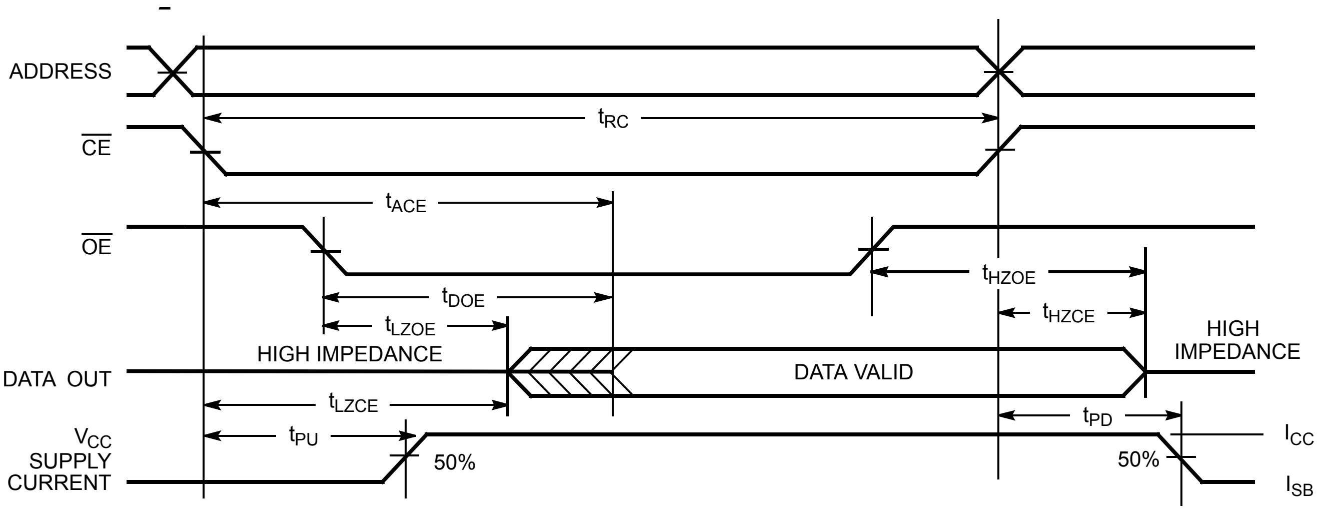


Figure 7. Read Cycle No. 2 ($\overline{OE}$ Controlled) [22, 23, 24]



Notes

20. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
21. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
22. $\overline{WE}$ is HIGH for read cycle.
23. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
24. Address valid before or similar to $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ($\overline{WE}$ Controlled) [25, 26, 27, 28]

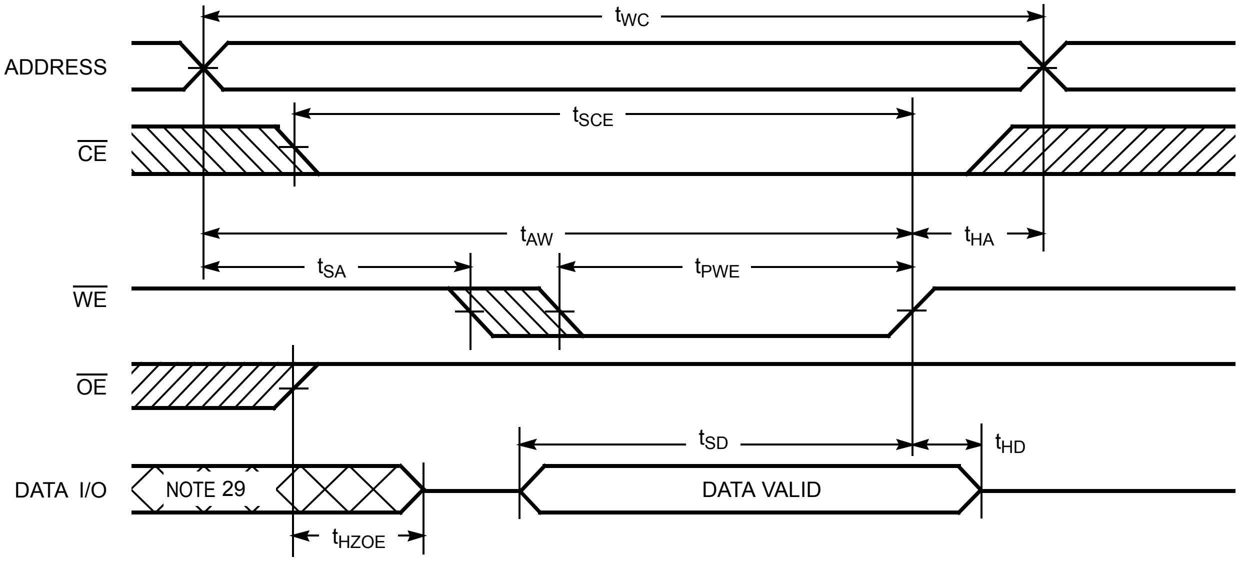
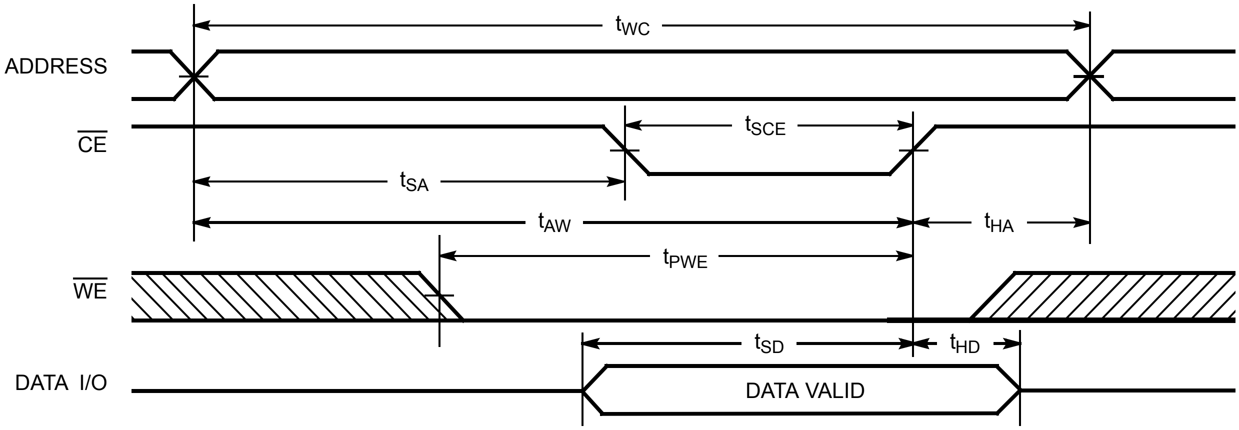


Figure 9. Write Cycle No. 2 ($\overline{CE}_1$ or CE_2 Controlled) [25, 26, 27, 28]



Notes

25. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
26. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
27. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
28. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
29. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

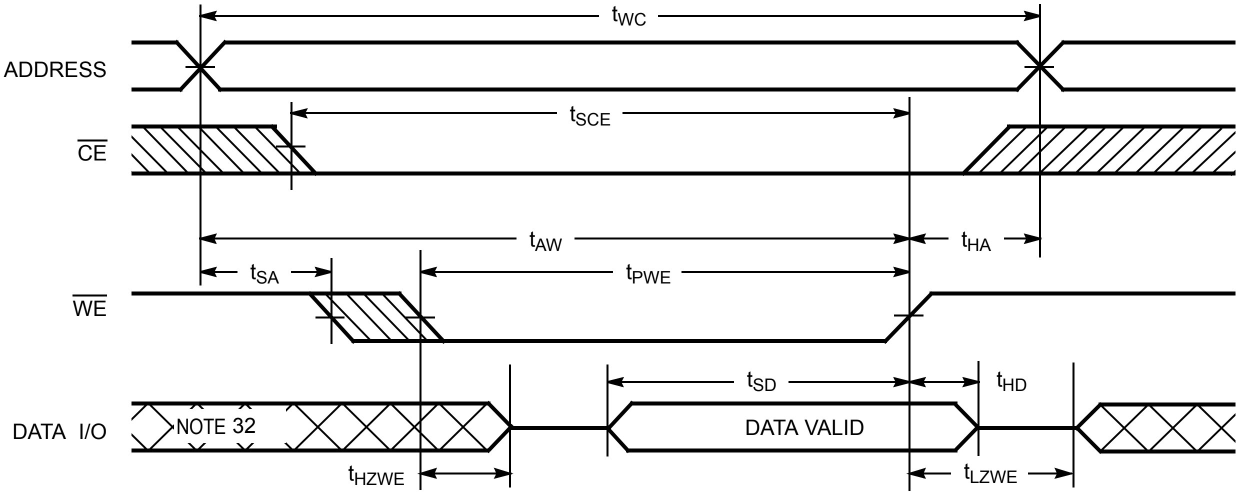


Figure 10. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [30, 31, 33]

Notes

30. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
31. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
32. During this period, the I/Os are in output state. Do not apply input signals.
33. The minimum write pulse width for WRITE Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X [34]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
X [34]	L	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	H	L	Data out	Read	Active (I_{CC})
L	H	L	X	Data in	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

Note

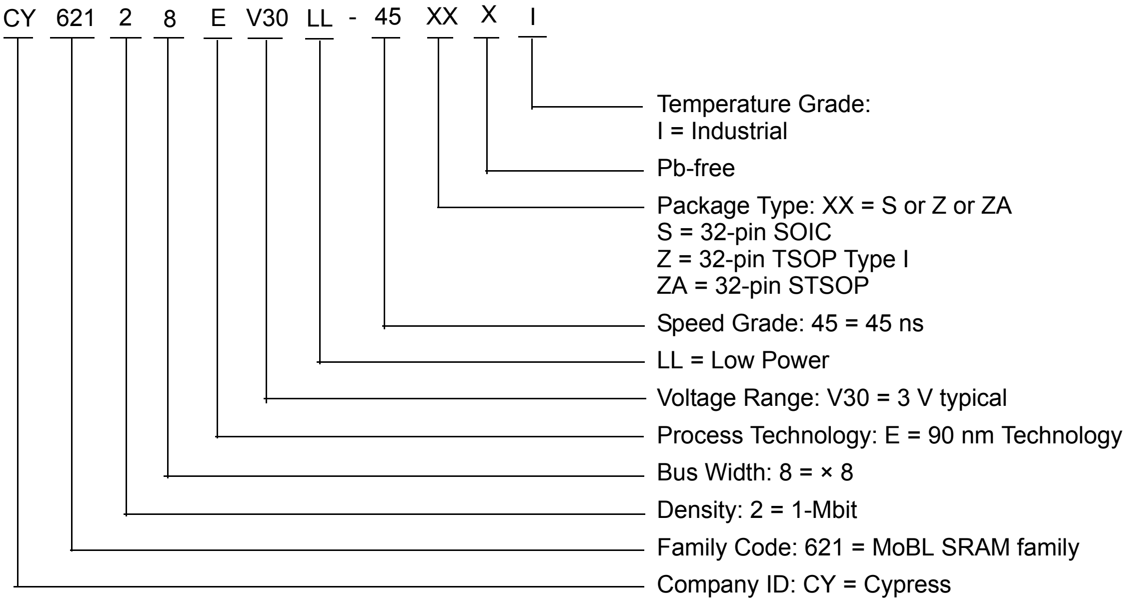
[34] The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62128EV30LL-45SXI	51-85081	32-pin 450-Mil SOIC (Pb-free)	Industrial
	CY62128EV30LL-45ZXI	51-85056	32-pin TSOP Type I (Pb-free)	
	CY62128EV30LL-45ZAXI	51-85094	32-pin STSOP (Pb-free)	

Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



CY 621 2 8 E V30 LL - 45 XX X I

Temperature Grade:
I = Industrial

Pb-free

Package Type: XX = S or Z or ZA
S = 32-pin SOIC
Z = 32-pin TSOP Type I
ZA = 32-pin STSOP

Speed Grade: 45 = 45 ns

LL = Low Power

Voltage Range: V30 = 3 V typical

Process Technology: E = 90 nm Technology

Bus Width: 8 = × 8

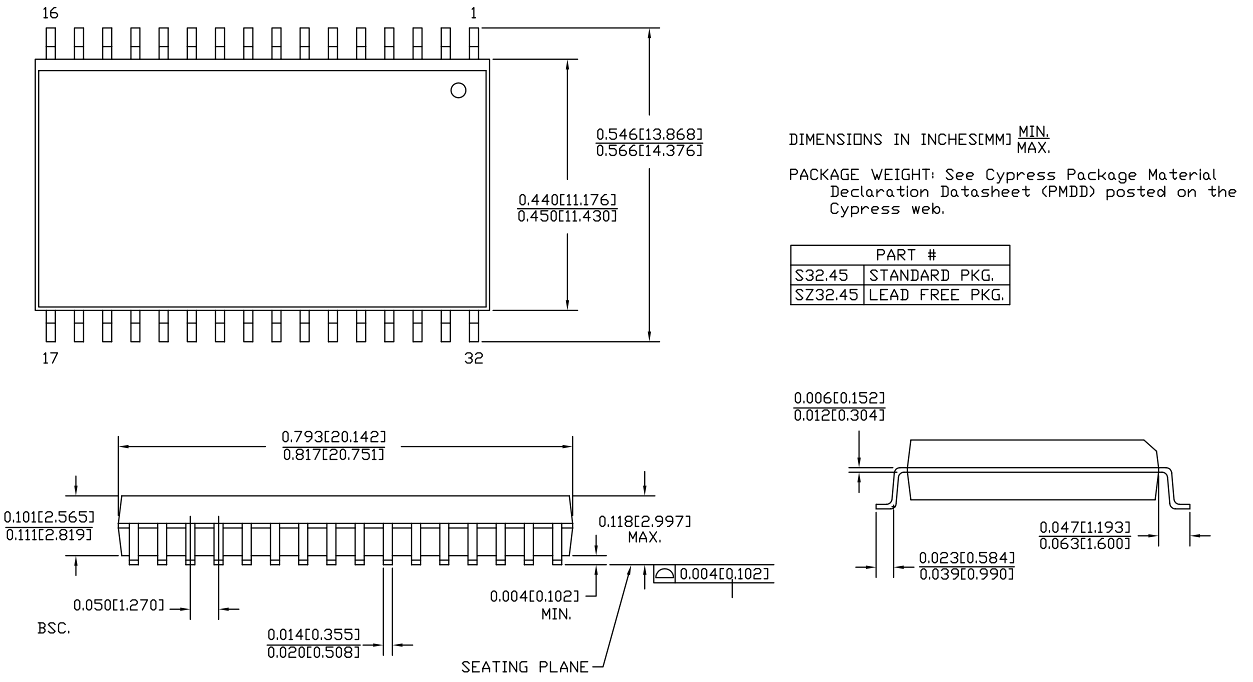
Density: 2 = 1-Mbit

Family Code: 621 = MoBL SRAM family

Company ID: CY = Cypress

Package Diagrams

Figure 11. 32-pin Molded SOIC (450 Mil) S32.45/SZ32.45, 51-85081



DIMENSIONS IN INCHES[MM] MIN./MAX.

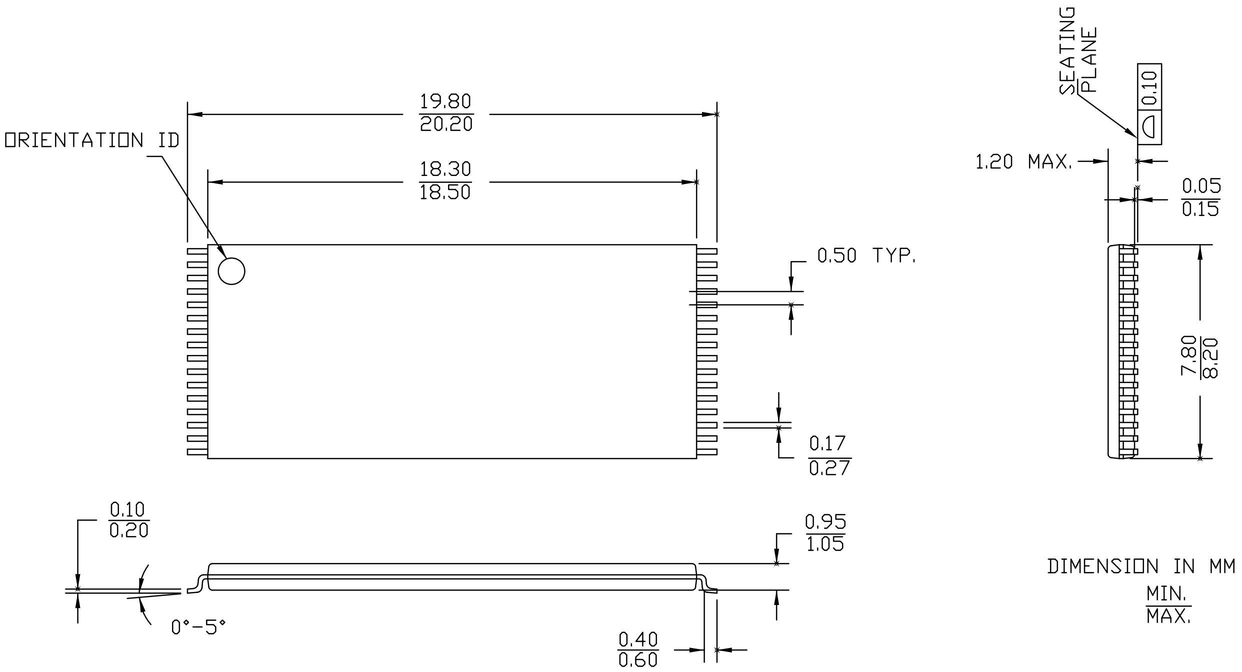
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

PART #	
S32.45	STANDARD PKG.
SZ32.45	LEAD FREE PKG.

51-85081 *E

Package Diagrams (continued)

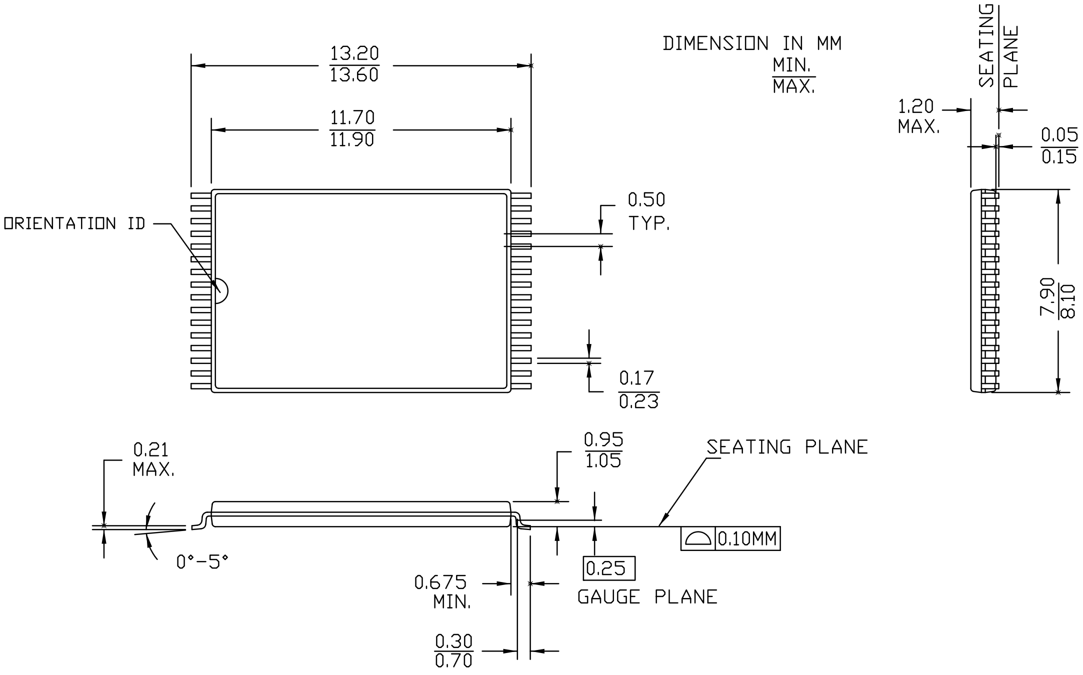
Figure 12. 32-pin TSOP I (8 × 20 × 1.0 mm) Z32, 51-85056



51-85056 *G

Package Diagrams (continued)

Figure 13. 32-pin Small TSOP (8 × 13.4 × 1.2 mm) ZA32, 51-85094



51-85094 *G

Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory
STSOP	Shrunk Thin Small Outline Package
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62128EV30 MoBL®, 1-Mbit (128 K × 8) Static RAM Document Number: 38-05579				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	285473	See ECN	PCI	New data sheet.
*A	461631	See ECN	NXR	Changed status from Preliminary to Final. Removed 35 ns speed bin related information in all instances across the document. Removed "L" version of CY62128EV30 related information in all instances across the document. Removed Reverse TSOP I package related information in all instances across the document. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 8 mA to 11 mA corresponding to Test Condition "f = f_{max}". Changed maximum value of I_{CC} parameter from 12 mA to 16 mA corresponding to Test Condition "f = f_{max}". Changed maximum value of I_{CC} parameter from 1.5 mA to 2.0 mA corresponding to Test Condition "f = 1 MHz". Changed typical value of I_{SB2} parameter from 0.5 µA to 1 µA. Changed maximum value of I_{SB2} parameter from 1 µA to 4 µA. Updated AC Test Loads and Waveforms: Updated Figure 4: Changed value of AC Test load Capacitance from 50 pF to 30 pF. Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 1 µA to 3 µA corresponding to Test Condition "LL". Updated Switching Characteristics: Changed minimum value of t_{LZOE} parameter from 3 ns to 5 ns for 45 ns speed bin. Changed minimum value of t_{LZCE} parameter from 6 ns to 10 ns for 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 22 ns to 18 ns for 45 ns speed bin. Changed minimum value of t_{PWE} parameter from 30 ns to 35 ns for 45 ns speed bin. Changed minimum value of t_{SD} parameter from 22 ns to 25 ns for 45 ns speed bin. Changed minimum value of t_{LZWE} parameter from 6 ns to 10 ns for 45 ns speed bin. Updated Ordering Information.
*B	464721	See ECN	NXR	Updated Logic Block Diagram.
*C	1024520	See ECN	VKN	Added final Automotive-A and Automotive-E information in all instances across the document. Updated Electrical Characteristics: Added Note 7 and referred the same note in I_{SB2} parameter. Updated Data Retention Characteristics: Added Note 10 and referred the same note in I_{CCDR} parameter. Updated Ordering Information.
*D	2257446	See ECN	NXR	Updated Maximum Ratings: Changed the Maximum rating of "Ambient Temperature with Power Applied" from 55 °C to +125 °C to –55 °C to +125 °C.
*E	2702841	05/06/2009	VKN / PYRS	Updated Switching Characteristics: Updated description of t_{PD} parameter. Updated Ordering Information (Added -45SXA part).
*F	2781490	10/08/2009	VKN	Updated Ordering Information (Included "CY62128EV30LL-45ZAXA" part).

Document History Page (continued)

Document Title: CY62128EV30 MoBL®, 1-Mbit (128 K × 8) Static RAM
Document Number: 38-05579

Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
*G	2934428	06/03/10	VKN	Updated Truth Table: Added Note 34 and referred the same note in ‘X’ in “$\overline{CE}_1$” and “CE_2” columns. Updated Package Diagrams. Updated to new template.
*H	3026548	09/12/2010	AJU	Updated Pin Configuration. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Minor edits.
*I	3115909	01/06/2011	RAME	Separated Automotive and Industrial parts from this data sheet. Removed Automotive related information in all instances across the document.
*J	3292906	06/25/2011	AJU	Updated Functional Description: Removed the Note “For best practice recommendations, refer to the Cypress application note “System Design Guidelines” at http://www.cypress.com website.” and its reference. Updated Package Diagrams. Updated to new template.
*K	4499499	09/11/2014	MEMJ	Updated Switching Characteristics: Added Note 19 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 33 and referred the same note in Figure 10. Updated Package Diagrams: spec 51-85081 – Changed revision from *C to *E. spec 51-85056 – Changed revision from *F to *G. spec 51-85094 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review.
*L	4581542	11/27/2014	VINI	Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Updated Maximum Ratings: Referred Notes 3, 4 in “Supply voltage to ground potential”.
*M	4920942	09/15/2015	VINI	Updated to new template. Completing Sunset Review.

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