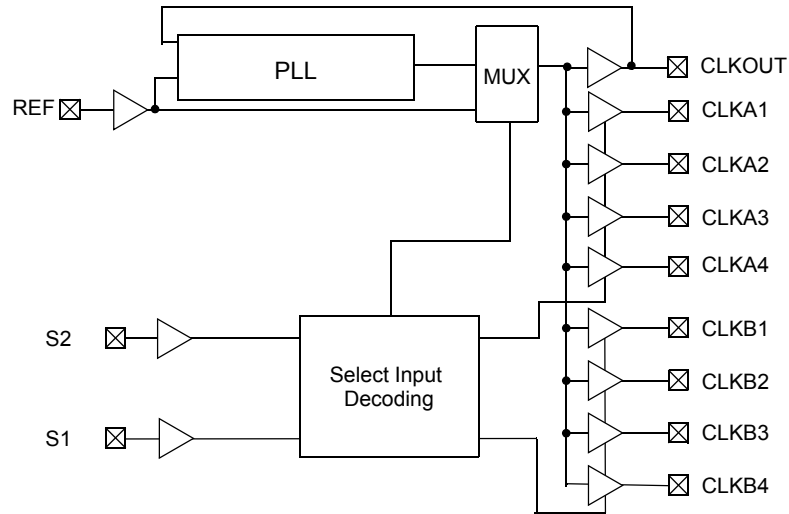


## Logic Block Diagram – CY2309C

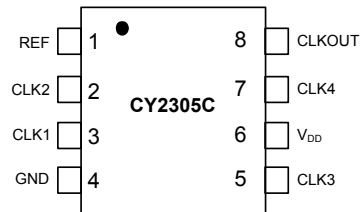


## Contents

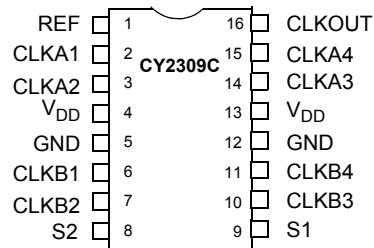
|                                          |           |                                                      |           |
|------------------------------------------|-----------|------------------------------------------------------|-----------|
| <b>Pinouts</b> .....                     | <b>4</b>  | <b>Switching Waveforms</b> .....                     | <b>14</b> |
| <b>Pin Definitions</b> .....             | <b>5</b>  | <b>Ordering Information</b> .....                    | <b>15</b> |
| <b>Pin Definitions</b> .....             | <b>5</b>  | Ordering Code Definitions .....                      | 16        |
| <b>Functional Overview</b> .....         | <b>6</b>  | <b>Package Diagrams</b> .....                        | <b>17</b> |
| Select Input Decoding .....              | 6         | <b>Acronyms</b> .....                                | <b>19</b> |
| Zero Delay and Skew Control .....        | 6         | <b>Document Conventions</b> .....                    | <b>19</b> |
| <b>Absolute Maximum Conditions</b> ..... | <b>7</b>  | Units of Measure .....                               | 19        |
| <b>Operating Conditions</b> .....        | <b>7</b>  | <b>Document History Page</b> .....                   | <b>20</b> |
| <b>Operating Conditions</b> .....        | <b>7</b>  | <b>Sales, Solutions, and Legal Information</b> ..... | <b>22</b> |
| <b>Electrical Characteristics</b> .....  | <b>8</b>  | Worldwide Sales and Design Support .....             | 22        |
| <b>Electrical Characteristics</b> .....  | <b>8</b>  | Products .....                                       | 22        |
| <b>Test Circuits</b> .....               | <b>9</b>  | PSoC®Solutions .....                                 | 22        |
| <b>Thermal Resistance</b> .....          | <b>9</b>  | Cypress Developer Community .....                    | 22        |
| <b>Switching Characteristics</b> .....   | <b>10</b> | Technical Support .....                              | 22        |
| <b>Switching Characteristics</b> .....   | <b>11</b> |                                                      |           |
| <b>Switching Characteristics</b> .....   | <b>12</b> |                                                      |           |
| <b>Switching characteristics</b> .....   | <b>13</b> |                                                      |           |

## Pinouts

**Figure 1. 8-pin SOIC pinout (Top View)**  
**CY2305C**



**Figure 2. 16-pin SOIC / TSSOP pinout (Top View)**  
**CY2309C**



## Pin Definitions

8-pin SOIC

| Pin | Signal                | Description                                          |
|-----|-----------------------|------------------------------------------------------|
| 1   | REF <sup>[1]</sup>    | Input reference frequency                            |
| 2   | CLK2 <sup>[2]</sup>   | Buffered clock output                                |
| 3   | CLK1 <sup>[2]</sup>   | Buffered clock output                                |
| 4   | GND                   | Ground                                               |
| 5   | CLK3 <sup>[2]</sup>   | Buffered clock output                                |
| 6   | V <sub>DD</sub>       | 3.3 V supply                                         |
| 7   | CLK4 <sup>[2]</sup>   | Buffered clock output                                |
| 8   | CLKOUT <sup>[2]</sup> | Buffered clock output, internal feedback on this pin |

## Pin Definitions

16-pin SOIC / TSSOP

| Pin | Signal                | Description                                    |
|-----|-----------------------|------------------------------------------------|
| 1   | REF <sup>[1]</sup>    | Input reference frequency                      |
| 2   | CLKA1 <sup>[2]</sup>  | Buffered clock output, Bank A                  |
| 3   | CLKA2 <sup>[2]</sup>  | Buffered clock output, Bank A                  |
| 4   | V <sub>DD</sub>       | 3.3 V supply                                   |
| 5   | GND                   | Ground                                         |
| 6   | CLKB1 <sup>[2]</sup>  | Buffered clock output, Bank B                  |
| 7   | CLKB2 <sup>[2]</sup>  | Buffered clock output, Bank B                  |
| 8   | S2 <sup>[3]</sup>     | Select input, bit 2                            |
| 9   | S1 <sup>[3]</sup>     | Select input, bit 1                            |
| 10  | CLKB3 <sup>[2]</sup>  | Buffered clock output, Bank B                  |
| 11  | CLKB4 <sup>[2]</sup>  | Buffered clock output, Bank B                  |
| 12  | GND                   | Ground                                         |
| 13  | V <sub>DD</sub>       | 3.3 V supply                                   |
| 14  | CLKA3 <sup>[2]</sup>  | Buffered clock output, Bank A                  |
| 15  | CLKA4 <sup>[2]</sup>  | Buffered clock output, Bank A                  |
| 16  | CLKOUT <sup>[2]</sup> | Buffered output, internal feedback on this pin |

### Notes

1. Weak pull down.
2. Weak pull down on all outputs.
3. Weak pull ups on these inputs.

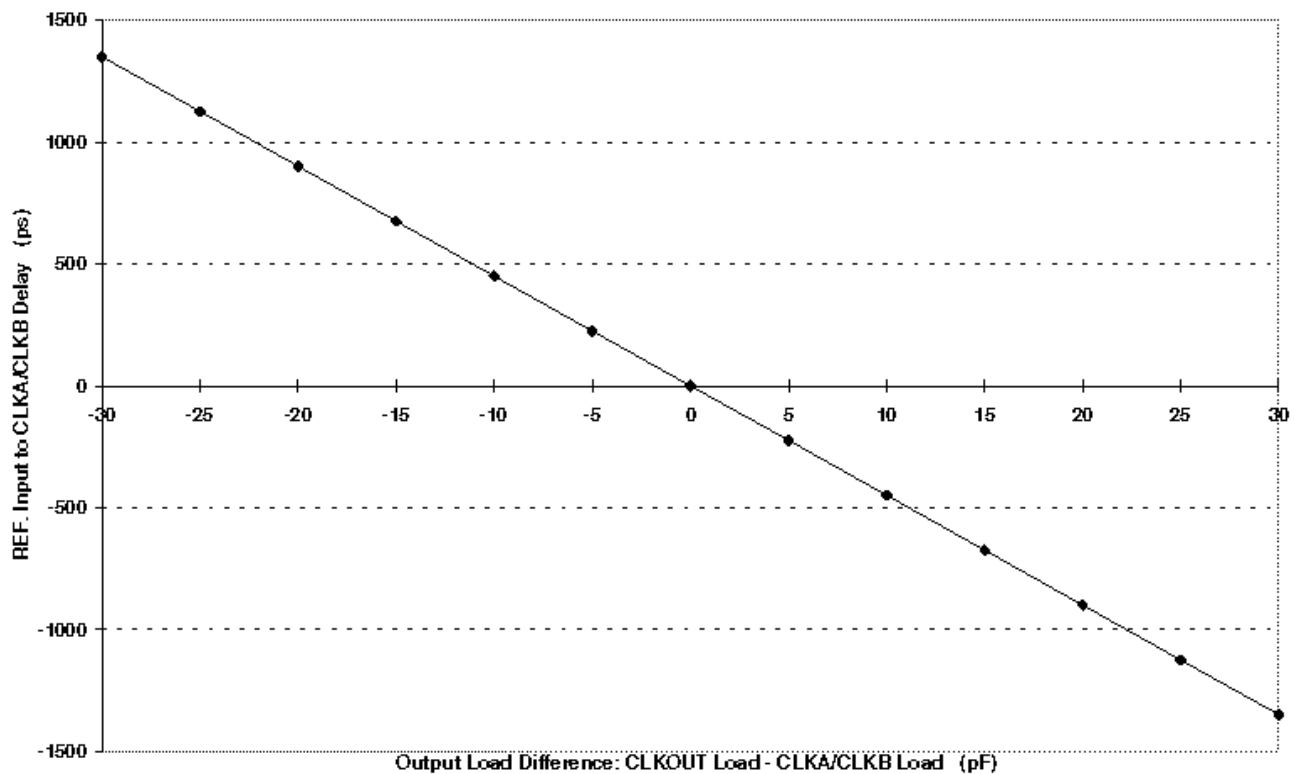
## Functional Overview

### Select Input Decoding

For CY2309C

| S2 | S1 | CLOCK A1–A4 | CLOCK B1–B4 | CLKOUT <sup>[4]</sup> | Output Source | PLL Shutdown |
|----|----|-------------|-------------|-----------------------|---------------|--------------|
| 0  | 0  | Three state | Three state | Driven                | PLL           | N            |
| 0  | 1  | Driven      | Three state | Driven                | PLL           | N            |
| 1  | 0  | Driven      | Driven      | Driven                | Reference     | Y            |
| 1  | 1  | Driven      | Driven      | Driven                | PLL           | N            |

Figure 3. REF. Input to CLKA/CLKB Delay vs. Loading Difference between CLKOUT and CLKA/CLKB pins



### Zero Delay and Skew Control

All outputs must be uniformly loaded to achieve Zero Delay between the input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input or output delay.

For applications requiring zero input or output delay, all outputs including CLKOUT are equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs for obtaining zero input or output delay.

For zero output to output skew, all outputs must be loaded equally.

Even if CLKOUT is not used, it must have a capacitive load, equal to that on other outputs, for obtaining zero input-output delay. If input to output delay adjustments are required, use Figure 3 to calculate loading differences between the CLKOUT pin and other outputs.

#### Note

- This output is driven and has an internal feedback for the PLL. The load on this output is adjusted to change the skew between the reference and output.

## Absolute Maximum Conditions

Supply voltage to ground potential ..... -0.5 V to +4.6 V  
 DC input voltage (Except REF) ..... -0.5 V to  $V_{DD} + 0.5$  V  
 DC input voltage REF ..... -0.5 V to  $V_{DD} + 0.5$  V

Storage temperature ..... -65 °C to +150 °C  
 Junction temperature ..... 150 °C  
 Static discharge voltage  
 (per MIL-STD-883, Method 3015) ..... > 2,000 V

## Operating Conditions

Operating Conditions Table for CY2305CSXC-XX and CY2309CSXC-XX Commercial Temperature devices.

| Parameter | Description                                                                                     | Min  | Max | Unit |
|-----------|-------------------------------------------------------------------------------------------------|------|-----|------|
| $V_{DD}$  | Supply voltage                                                                                  | 3.0  | 3.6 | V    |
| $T_A$     | Operating temperature (ambient temperature)                                                     | 0    | 70  | °C   |
| $C_L$     | Load capacitance, below 100 MHz                                                                 | —    | 30  | pF   |
| $C_L$     | Load capacitance, from 100 MHz to 133 MHz                                                       | —    | 10  | pF   |
| $C_{IN}$  | Input capacitance                                                                               | —    | 7   | pF   |
| $t_{PU}$  | Power-up time for all $V_{DD}$ s to reach minimum specified voltage (power ramps are monotonic) | 0.05 | 50  | ms   |

## Operating Conditions

Operating Conditions Table for CY2305CSXI-XX, CY2305CSXA-XX and CY2309CSXI-XX Industrial / Automotive-A Temperature devices.

| Parameter | Description                                                                                     | Min  | Max | Unit |
|-----------|-------------------------------------------------------------------------------------------------|------|-----|------|
| $V_{DD}$  | Supply voltage                                                                                  | 3.0  | 3.6 | V    |
| $T_A$     | Operating temperature (ambient temperature)                                                     | -40  | 85  | °C   |
| $C_L$     | Load capacitance, below 100 MHz                                                                 | —    | 30  | pF   |
| $C_L$     | Load capacitance, from 100 MHz to 133 MHz                                                       | —    | 10  | pF   |
| $C_{IN}$  | Input capacitance                                                                               | —    | 7   | pF   |
| $t_{PU}$  | Power-up time for all $V_{DD}$ s to reach minimum specified voltage (power ramps are monotonic) | 0.05 | 50  | ms   |

## Electrical Characteristics

Electrical Characteristics Table for CY2305CSXC-XX and CY2309CSXC-XX Commercial Temperature devices.

| Parameter          | Description                        | Test Conditions                                       | Min | Max | Unit          |
|--------------------|------------------------------------|-------------------------------------------------------|-----|-----|---------------|
| $V_{IL}$           | Input LOW voltage <sup>[5]</sup>   |                                                       | –   | 0.8 | V             |
| $V_{IH}$           | Input HIGH voltage <sup>[5]</sup>  |                                                       | 2.0 | –   | V             |
| $I_{IL}$           | Input LOW current                  | $V_{IN} = 0\text{ V}$                                 | –   | 50  | $\mu\text{A}$ |
| $I_{IH}$           | Input HIGH current                 | $V_{IN} = V_{DD}$                                     | –   | 100 | $\mu\text{A}$ |
| $V_{OL}$           | Output LOW voltage <sup>[6]</sup>  | $I_{OL} = 8\text{ mA} (-1)$                           | –   | 0.4 | V             |
|                    |                                    | $I_{OL} = 12\text{ mA} (-1H)$                         |     |     |               |
| $V_{OH}$           | Output HIGH voltage <sup>[6]</sup> | $I_{OH} = -8\text{ mA} (-1)$                          | 2.4 | –   | V             |
|                    |                                    | $I_{OH} = -12\text{ mA} (-1H)$                        |     |     |               |
| $I_{DD}$ (PD mode) | Power-down supply current          | REF = 0 MHz                                           | –   | 12  | $\mu\text{A}$ |
| $I_{DD}$           | Supply current                     | Unloaded outputs at 66.67 MHz, SEL inputs at $V_{DD}$ | –   | 32  | mA            |

## Electrical Characteristics

Electrical Characteristics Table for CY2305CSXI-XX, CY2305CSXA-XX and CY2309CSXI-XX Industrial / Automotive-A Temperature devices.

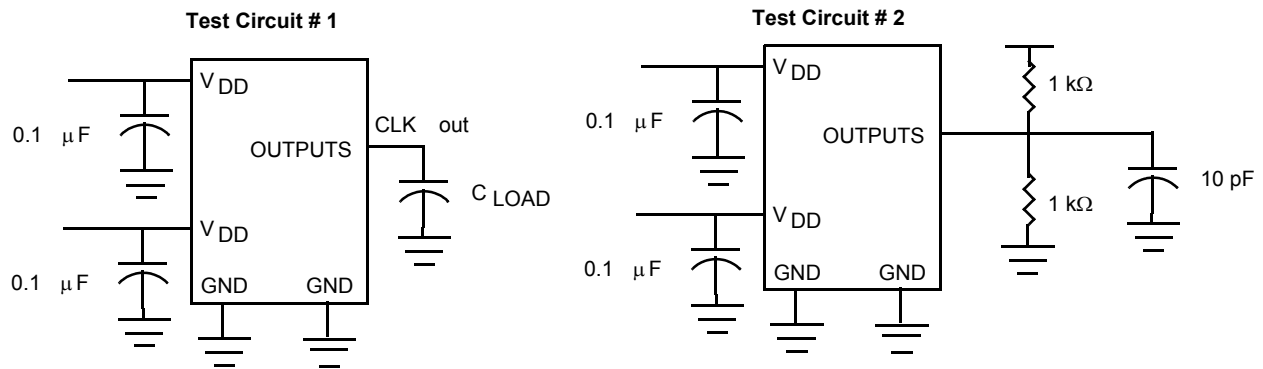
| Parameter          | Description                        | Test Conditions                                       | Min | Max | Unit          |
|--------------------|------------------------------------|-------------------------------------------------------|-----|-----|---------------|
| $V_{IL}$           | Input LOW voltage <sup>[5]</sup>   |                                                       | –   | 0.8 | V             |
| $V_{IH}$           | Input HIGH voltage <sup>[5]</sup>  |                                                       | 2.0 | –   | V             |
| $I_{IL}$           | Input LOW current                  | $V_{IN} = 0\text{ V}$                                 | –   | 50  | $\mu\text{A}$ |
| $I_{IH}$           | Input HIGH current                 | $V_{IN} = V_{DD}$                                     | –   | 100 | $\mu\text{A}$ |
| $V_{OL}$           | Output LOW voltage <sup>[6]</sup>  | $I_{OL} = 8\text{ mA} (-1)$                           | –   | 0.4 | V             |
|                    |                                    | $I_{OL} = 12\text{ mA} (-1H)$                         |     |     |               |
| $V_{OH}$           | Output HIGH voltage <sup>[6]</sup> | $I_{OH} = -8\text{ mA} (-1)$                          | 2.4 | –   | V             |
|                    |                                    | $I_{OH} = -12\text{ mA} (-1H)$                        |     |     |               |
| $I_{DD}$ (PD mode) | Power-down supply current          | REF = 0 MHz                                           | –   | 25  | $\mu\text{A}$ |
| $I_{DD}$           | Supply current                     | Unloaded outputs at 66.67 MHz, SEL inputs at $V_{DD}$ | –   | 35  | mA            |

### Notes

5. REF input has a threshold voltage of  $V_{DD}/2$ .
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Test Circuits

Figure 4. Test Circuits



For parameter  $t_g$  (output slew rate) on -1H devices

## Thermal Resistance

| Parameter <sup>[7]</sup> | Description                              | Test Conditions                                                                                                             | 8-pin SOIC | 16-pin SOIC | 16-pin TSSOP | Unit |
|--------------------------|------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|------------|-------------|--------------|------|
| $\theta_{JA}$            | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 145        | 121         | 111          | °C/W |
| $\theta_{JC}$            | Thermal resistance (junction to case)    |                                                                                                                             | 62         | 53          | 26           | °C/W |

### Note

7. These parameters are guaranteed by design and are not tested.

## Switching Characteristics

Switching Characteristics Table for CY2305CSXC-1 and CY2309CSXC-1 Commercial Temperature devices. All parameters are specified with loaded outputs.

| Parameter  | Description                                                 | Test Conditions                                                            | Min | Typ | Max    | Unit |
|------------|-------------------------------------------------------------|----------------------------------------------------------------------------|-----|-----|--------|------|
| $t_1$      | Output frequency                                            | 30 pF load                                                                 | 10  | –   | 100    | MHz  |
|            |                                                             | 10 pF load                                                                 | 10  | –   | 133.33 | MHz  |
| $t_{DC}$   | Output duty cycle <sup>[8]</sup> = $t_2 \div t_1$           | Measured at 1.4 V, $F_{out} > 50$ MHz                                      | 40  | 50  | 60     | %    |
|            |                                                             | Measured at 1.4 V, $F_{out} \leq 50$ MHz                                   | 45  | 50  | 55     | %    |
| $t_3$      | Rise time <sup>[8]</sup>                                    | Measured between 0.8 V and 2.0 V                                           | –   | –   | 2.25   | ns   |
| $t_4$      | Fall time <sup>[8]</sup>                                    | Measured between 0.8 V and 2.0 V                                           | –   | –   | 2.25   | ns   |
| $t_5$      | Output-to-output skew <sup>[8]</sup>                        | All outputs equally loaded                                                 | –   | –   | 200    | ps   |
| $t_{6A}$   | Delay, REF rising edge to CLKOUT rising edge <sup>[8]</sup> | Measured at $V_{DD}/2$                                                     | –   | 0   | ±350   | ps   |
| $t_{6B}$   | Delay, REF rising edge to CLKOUT rising edge <sup>[8]</sup> | Measured at $V_{DD}/2$ . Measured in PLL Bypass mode, CY2309C device only. | 1   | 5   | 8.7    | ns   |
| $t_7$      | Device-to-device skew <sup>[8]</sup>                        | Measured at $V_{DD}/2$ on the CLKOUT pins of devices                       | –   | 0   | 700    | ps   |
| $t_J$      | Cycle-to-cycle jitter, peak <sup>[8]</sup>                  | Measured at 66.67 MHz, loaded outputs                                      | –   | 50  | 175    | ps   |
| $t_{LOCK}$ | PLL lock time <sup>[8]</sup>                                | Stable power supply, valid clock presented on REF pin                      | –   | –   | 1.0    | ms   |

### Note

8. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Switching Characteristics

Switching Characteristics Table for CY2305CSXC-1H and CY2309CSXC-1H Commercial Temperature devices. All parameters are specified with loaded outputs.

| Parameter  | Description                                                 | Description                                                                | Min | Typ | Max    | Unit |
|------------|-------------------------------------------------------------|----------------------------------------------------------------------------|-----|-----|--------|------|
| $t_1$      | Output frequency                                            | 30 pF load                                                                 | 10  | –   | 100    | MHz  |
|            |                                                             | 10 pF load                                                                 | 10  | –   | 133.33 | MHz  |
| $t_{DC}$   | Output duty cycle <sup>[9]</sup> = $t_2 \div t_1$           | Measured at 1.4 V, $F_{out} > 50$ MHz                                      | 40  | 50  | 60     | %    |
|            |                                                             | Measured at 1.4 V, $F_{out} \leq 50$ MHz                                   | 45  | 50  | 55     | %    |
| $t_3$      | Rise time <sup>[9]</sup>                                    | Measured between 0.8 V and 2.0 V                                           | –   | –   | 1.5    | ns   |
| $t_4$      | Fall time <sup>[9]</sup>                                    | Measured between 0.8 V and 2.0 V                                           | –   | –   | 1.5    | ns   |
| $t_5$      | Output-to-output skew <sup>[9]</sup>                        | All outputs equally loaded                                                 | –   | –   | 200    | ps   |
| $t_{6A}$   | Delay, REF rising edge to CLKOUT rising edge <sup>[9]</sup> | Measured at $V_{DD}/2$                                                     | –   | 0   | ±350   | ps   |
| $t_{6B}$   | Delay, REF rising edge to CLKOUT rising edge <sup>[9]</sup> | Measured at $V_{DD}/2$ . Measured in PLL Bypass mode, CY2309C device only. | 1   | 5   | 8.7    | ns   |
| $t_7$      | Device-to-device skew <sup>[9]</sup>                        | Measured at $V_{DD}/2$ on the CLKOUT pins of devices                       | –   | 0   | 700    | ps   |
| $t_8$      | Output slew rate <sup>[9]</sup>                             | Measured between 0.8 V and 2.0 V using Test circuit #2                     | 1   | –   | –      | V/ns |
| $t_J$      | Cycle-to-cycle jitter, peak <sup>[9]</sup>                  | Measured at 66.67 MHz, loaded outputs                                      | –   | –   | 175    | ps   |
| $t_{LOCK}$ | PLL lock time <sup>[9]</sup>                                | Stable power supply, valid clock presented on REF pin                      | –   | –   | 1.0    | ms   |

### Note

9. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Switching Characteristics

Switching Characteristics Table for CY2305CSXI-1, CY2305CSXA-1, and CY2309CSXI-1 Industrial Temperature devices. All parameters are specified with loaded outputs.

| Parameter  | Description                                                  | Test Conditions                                                            | Min | Typ | Max    | Unit |
|------------|--------------------------------------------------------------|----------------------------------------------------------------------------|-----|-----|--------|------|
| $t_1$      | Output frequency                                             | 30 pF load                                                                 | 10  | –   | 100    | MHz  |
|            |                                                              | 10 pF load                                                                 | 10  | –   | 133.33 | MHz  |
| $t_{DC}$   | Output duty cycle <sup>[10]</sup> = $t_2 \div t_1$           | Measured at 1.4 V, $F_{out} > 50$ MHz                                      | 40  | 50  | 60     | %    |
|            |                                                              | Measured at 1.4 V, $F_{out} \leq 50$ MHz                                   | 45  | 50  | 55     | %    |
| $t_3$      | Rise time <sup>[10]</sup>                                    | Measured between 0.8 V and 2.0 V                                           | –   | –   | 2.25   | ns   |
| $t_4$      | Fall time <sup>[10]</sup>                                    | Measured between 0.8 V and 2.0 V                                           | –   | –   | 2.25   | ns   |
| $t_5$      | Output-to-output skew <sup>[10]</sup>                        | All outputs equally loaded                                                 | –   | –   | 200    | ps   |
| $t_{6A}$   | Delay, REF rising edge to CLKOUT rising edge <sup>[10]</sup> | Measured at $V_{DD}/2$                                                     | –   | 0   | ±350   | ps   |
| $t_{6B}$   | Delay, REF rising edge to CLKOUT rising edge <sup>[10]</sup> | Measured at $V_{DD}/2$ . Measured in PLL Bypass mode, CY2309C device only. | 1   | 5   | 8.7    | ns   |
| $t_7$      | Device-to-device skew <sup>[10]</sup>                        | Measured at $V_{DD}/2$ on the CLKOUT pins of devices                       | –   | 0   | 700    | ps   |
| $t_J$      | Cycle-to-cycle jitter, peak <sup>[10]</sup>                  | Measured at 66.67 MHz, loaded outputs                                      | –   | 50  | 175    | ps   |
| $t_{LOCK}$ | PLL lock time <sup>[10]</sup>                                | Stable power supply, valid clock presented on REF pin                      | –   | –   | 1.0    | ms   |

### Note

10. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Switching characteristics

Switching Characteristics Table for CY2305CSXI-1H, CY2305CSXA-1H and CY2309CSXI-1H Industrial / Automotive-A Temperature devices. All parameters are specified with loaded outputs.

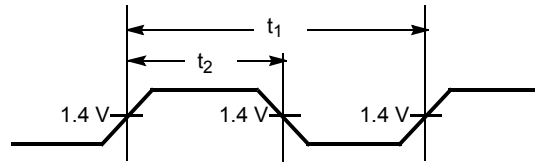
| Parameter  | Description                                                  | Description                                                                | Min | Typ | Max    | Unit |
|------------|--------------------------------------------------------------|----------------------------------------------------------------------------|-----|-----|--------|------|
| $t_1$      | Output frequency                                             | 30 pF load                                                                 | 10  | –   | 100    | MHz  |
|            |                                                              | 10 pF load                                                                 | 10  | –   | 133.33 | MHz  |
| $t_{DC}$   | Output duty cycle <sup>[11]</sup> = $t_2 \div t_1$           | Measured at 1.4 V, $F_{out} > 50$ MHz                                      | 40  | 50  | 60     | %    |
|            |                                                              | Measured at 1.4 V, $F_{out} \leq 50$ MHz                                   | 45  | 50  | 55     | %    |
| $t_3$      | Rise time <sup>[11]</sup>                                    | Measured between 0.8 V and 2.0 V                                           | –   | –   | 1.5    | ns   |
| $t_4$      | Fall time <sup>[11]</sup>                                    | Measured between 0.8 V and 2.0 V                                           | –   | –   | 1.5    | ns   |
| $t_5$      | Output-to-output skew <sup>[11]</sup>                        | All outputs equally loaded                                                 | –   | –   | 200    | ps   |
| $t_{6A}$   | Delay, REF rising edge to CLKOUT rising edge <sup>[11]</sup> | Measured at $V_{DD}/2$                                                     | –   | 0   | ±350   | ps   |
| $t_{6B}$   | Delay, REF rising edge to CLKOUT rising edge <sup>[11]</sup> | Measured at $V_{DD}/2$ . Measured in PLL Bypass mode, CY2309C device only. | 1   | 5   | 8.7    | ns   |
| $t_7$      | Device-to-device skew <sup>[11]</sup>                        | Measured at $V_{DD}/2$ on the CLKOUT pins of devices                       | –   | 0   | 700    | ps   |
| $t_8$      | Output slew rate <sup>[11]</sup>                             | Measured between 0.8 V and 2.0 V using Test circuit #2                     | 1   | –   | –      | V/ns |
| $t_J$      | Cycle-to-cycle jitter, peak <sup>[11]</sup>                  | Measured at 66.67 MHz, loaded outputs                                      | –   | –   | 175    | ps   |
| $t_{LOCK}$ | PLL lock time <sup>[11]</sup>                                | Stable power supply, valid clock presented on REF pin                      | –   | –   | 1.0    | ms   |

### Note

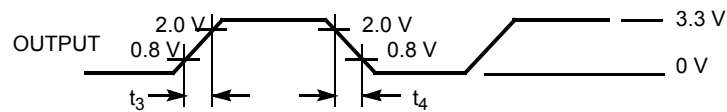
11. Parameter is guaranteed by design and characterization. Not 100% tested in production.

## Switching Waveforms

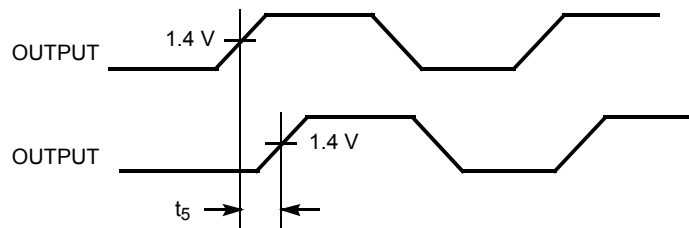
**Figure 5. Duty Cycle Timing**



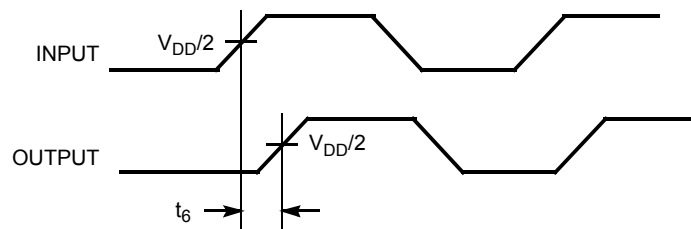
**Figure 6. All Outputs Rise/Fall Time**



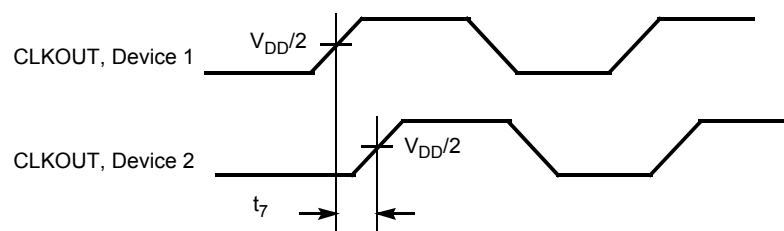
**Figure 7. Output-Output Skew**



**Figure 8. Input-Output Propagation Delay**



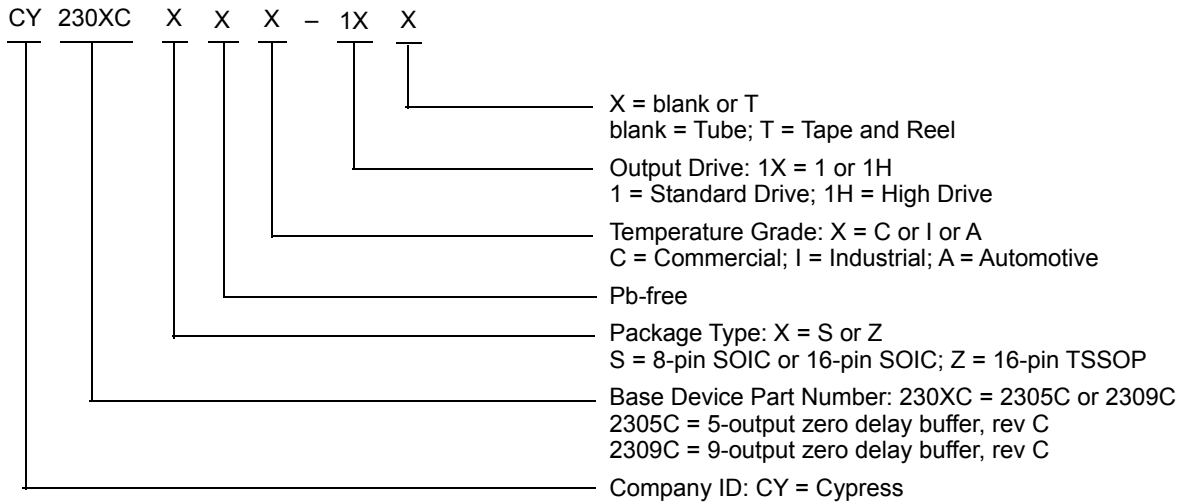
**Figure 9. Device-Device Skew**



## Ordering Information

| Ordering Code            | Package Type                          | Operating Range |
|--------------------------|---------------------------------------|-----------------|
| <b>Pb-free - CY2305C</b> |                                       |                 |
| CY2305CSXC-1             | 8-pin SOIC (150 Mil)                  | Commercial      |
| CY2305CSXC-1T            | 8-pin SOIC (150 Mil) – Tape and Reel  | Commercial      |
| CY2305CSXC-1H            | 8-pin SOIC (150 Mil)                  | Commercial      |
| CY2305CSXC-1HT           | 8-pin SOIC (150 Mil) – Tape and Reel  | Commercial      |
| CY2305CSXI-1             | 8-pin SOIC (150 Mil)                  | Industrial      |
| CY2305CSXI-1T            | 8-pin SOIC (150 Mil) – Tape and Reel  | Industrial      |
| CY2305CSXI-1H            | 8-pin SOIC (150 Mil)                  | Industrial      |
| CY2305CSXI-1HT           | 8-pin SOIC (150 Mil) – Tape and Reel  | Industrial      |
| CY2305CSXA-1H            | 8-pin SOIC (150 Mil)                  | Automotive-A    |
| CY2305CSXA-1HT           | 8-pin SOIC (150 Mil) – Tape and Reel  | Automotive-A    |
| <b>Pb-free - CY2309C</b> |                                       |                 |
| CY2309CSXC-1             | 16-pin SOIC (150 Mil)                 | Commercial      |
| CY2309CSXC-1T            | 16-pin SOIC (150 Mil) – Tape and Reel | Commercial      |
| CY2309CSXC-1H            | 16-pin SOIC (150 Mil)                 | Commercial      |
| CY2309CSXC-1HT           | 16-pin SOIC (150 Mil) – Tape and Reel | Commercial      |
| CY2309CSXI-1             | 16-pin SOIC (150 Mil)                 | Industrial      |
| CY2309CSXI-1T            | 16-pin SOIC (150 Mil) – Tape and Reel | Industrial      |
| CY2309CSXI-1H            | 16-pin SOIC (150 Mil)                 | Industrial      |
| CY2309CSXI-1HT           | 16-pin SOIC (150 Mil) – Tape and Reel | Industrial      |
| CY2309CZXC-1             | 16-pin TSSOP (4.4 mm)                 | Commercial      |
| CY2309CZXC-1T            | 16-pin TSSOP (4.4 mm) – Tape and Reel | Commercial      |
| CY2309CZXC-1H            | 16-pin TSSOP (4.4 mm)                 | Commercial      |
| CY2309CZXC-1HT           | 16-pin TSSOP (4.4 mm) – Tape and Reel | Commercial      |
| CY2309CZXI-1             | 16-pin TSSOP (4.4 mm)                 | Industrial      |
| CY2309CZXI-1T            | 16-pin TSSOP (4.4 mm) – Tape and Reel | Industrial      |
| CY2309CZXI-1H            | 16-pin TSSOP (4.4 mm)                 | Industrial      |
| CY2309CZXI-1HT           | 16-pin TSSOP (4.4 mm) – Tape and Reel | Industrial      |

## Ordering Code Definitions

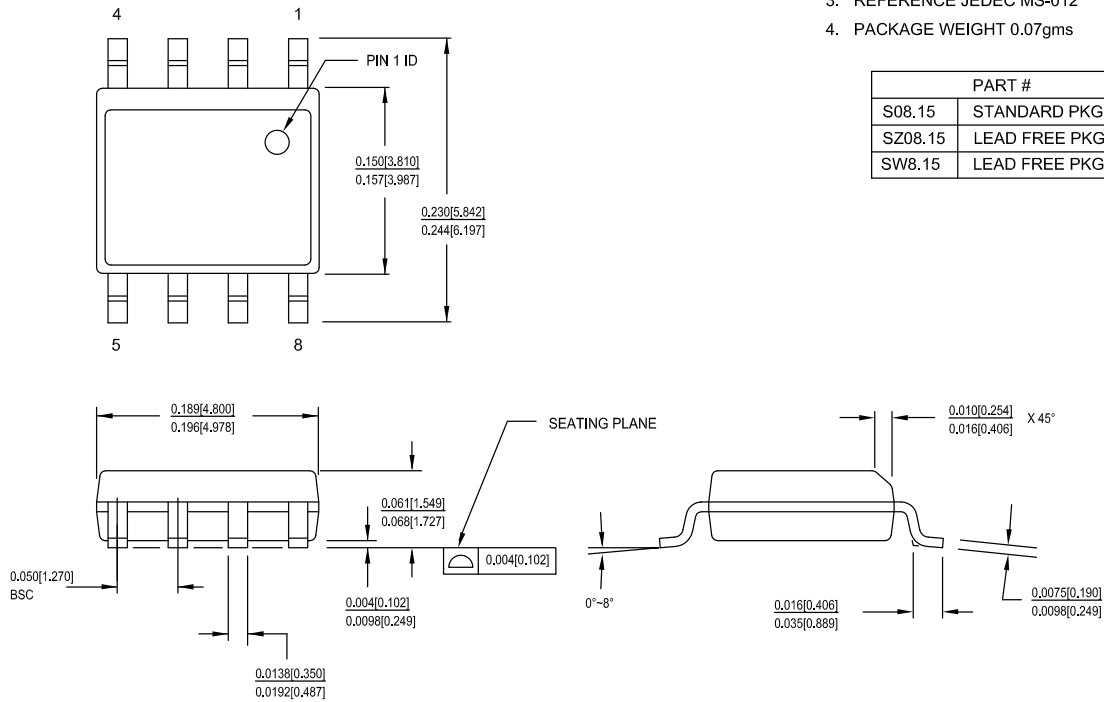


## Package Diagrams

Figure 10. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN.  
MAX.
2. PIN 1 ID IS OPTIONAL,  
ROUND ON SINGLE LEADFRAME  
RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

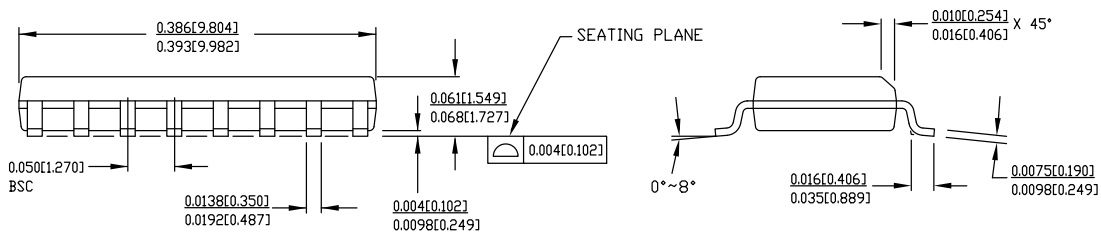
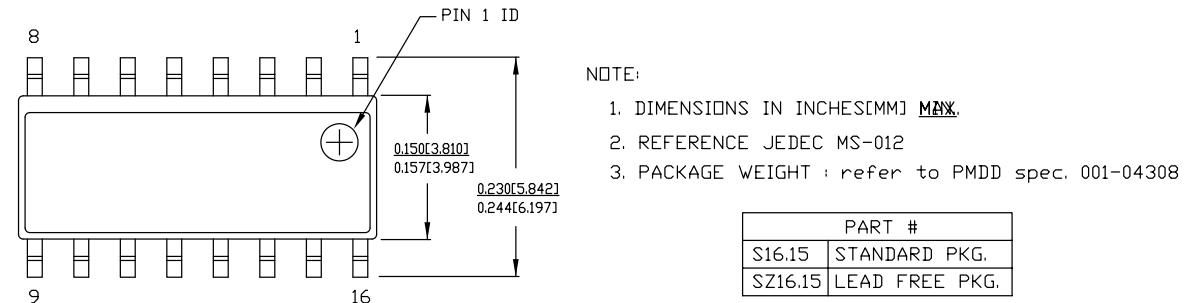
| PART #  |               |
|---------|---------------|
| S08.15  | STANDARD PKG  |
| SZ08.15 | LEAD FREE PKG |
| SW8.15  | LEAD FREE PKG |



51-85066 \*H

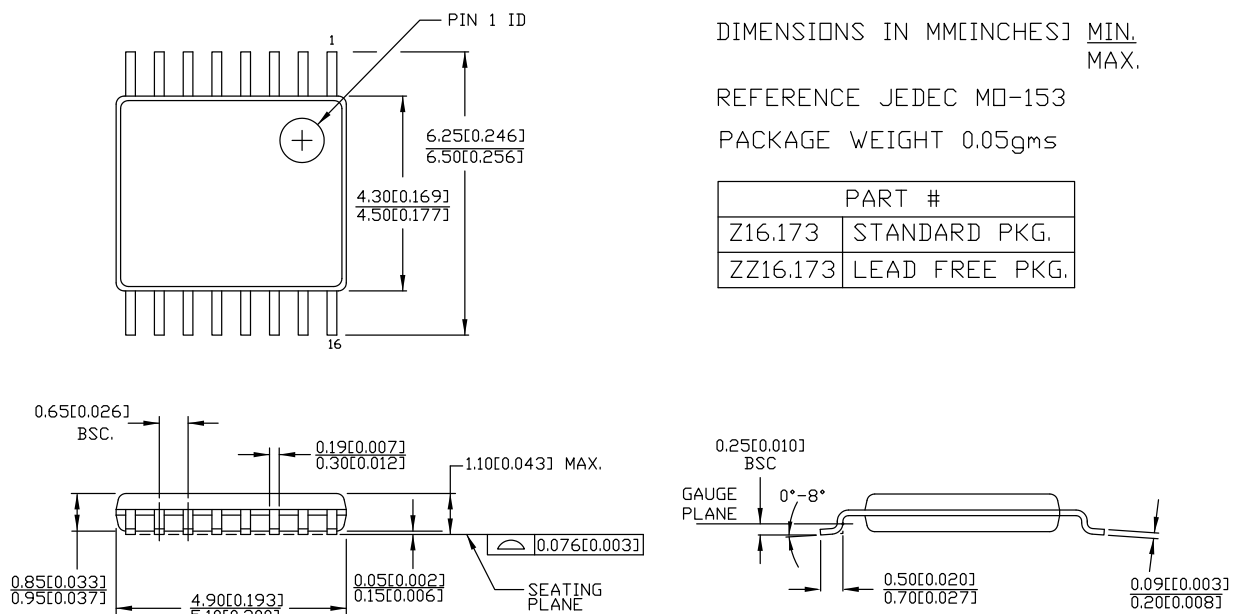
## Package Diagrams (continued)

**Figure 11. 16-pin SOIC (150 Mil) S16.15/SZ16.15 Package Outline, 51-85068**



51-85068 \*E

**Figure 12. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091**



51-85091 \*E

## Acronyms

| Acronym | Description                             |
|---------|-----------------------------------------|
| CMOS    | Complementary Metal Oxide Semiconductor |
| PLL     | Phase Locked Loop                       |
| SOIC    | Small Outline Integrated Circuit        |
| TSSOP   | Thin Shrunk Small Outline Package       |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| kHz    | kilohertz       |
| MHz    | megahertz       |
| μA     | microampere     |
| mA     | milliampere     |
| ms     | millisecond     |
| ns     | nanosecond      |
| pF     | picofarad       |
| ps     | picosecond      |
| V      | volt            |

## Document History Page

| Document Title: CY2305C/CY2309C, 3.3 V Zero Delay Clock Buffer<br>Document Number: 38-07672 |         |            |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------------------------------------------------------------------------------------------|---------|------------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                        | ECN No. | Issue Date | Orig. of Change  | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| **                                                                                          | 224421  | See ECN    | RGL              | New data sheet                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| *A                                                                                          | 268571  | See ECN    | RGL              | Added bullet for 5 V tolerant inputs in the features                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| *B                                                                                          | 276453  | See ECN    | RGL              | Minor Change: Moved one sentence from the features to the Functional Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| *C                                                                                          | 303063  | See ECN    | RGL              | Updated data sheet as per characterization data                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| *D                                                                                          | 318315  | See ECN    | RGL              | Data sheet rewrite                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| *E                                                                                          | 344815  | See ECN    | RGL              | Minor Error: Corrected the header of all the AC/DC tables with the right part numbers.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| *F                                                                                          | 1279889 | See ECN    | KVM              | Changed title from "CY2305C/CY2309C, Low Cost 3.3 V Zero Delay Buffer" to "CY2305C/CY2309C, 3.3 V Zero Delay Clock Buffer".<br>Specified the VIL minimum value to -0.3 V<br>Specified the VIH maximum value to VDD + 0.3 V<br>Changed DC Input Voltage (REF) maximum value in Absolute Maximum section<br>Removed references to 5 V tolerant inputs (pages 1 and 2)<br>Removed Pentium compatibility reference<br>Added CY2305C block diagram<br>Added ,peak to the jitter specifications<br>Changed typical jitter from 75 ps to 50 ps for standard drive devices<br>For standard drive devices, tightened rise/fall times from 2.5 ns to 2.25 ns<br>Tightened cycle-to-cycle jitter from 200 ps to 175 ps<br>Tightened output-to-output skew from 250 ps to 200 ps |
| *G                                                                                          | 1561504 | See ECN    | KVM / NSI / AESA | Changed status from Preliminary to Final.<br>Added CY2305C Automotive-A grade devices<br>Extended duty cycle specs to cover entire frequency range                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| *H                                                                                          | 2558537 | 08/27/08   | KVM / AESA       | Updated <a href="#">Ordering Information</a> :<br>Added CY2305CSXA-1 and CY2305CSXA-1T parts under Pb-free CY2305C.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| *I                                                                                          | 2901743 | 03/30/2010 | VIVG             | Added <a href="#">Ordering Code Definitions</a> under <a href="#">Ordering Information</a> .<br>Updated <a href="#">Package Diagrams</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| *J                                                                                          | 3080990 | 11/10/2010 | BASH             | Updated <a href="#">Pinouts</a> :<br>Updated <a href="#">Figure 1</a> (Modified pin diagram).<br>Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .<br>Updated to new template.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| *K                                                                                          | 3160535 | 02/03/2011 | BASH             | Updated <a href="#">Electrical Characteristics</a> :<br>Removed minimum value of V <sub>IL</sub> parameter and maximum value of V <sub>IH</sub> parameter.<br>Updated <a href="#">Electrical Characteristics</a> :<br>Removed minimum value of V <sub>IL</sub> parameter and maximum value of V <sub>IH</sub> parameter.<br>Updated <a href="#">Ordering Information</a> :<br>Removed Prune parts CY2305CSXA-1 and CY2305CSXA-1T.                                                                                                                                                                                                                                                                                                                                    |
| *L                                                                                          | 3822852 | 11/27/2012 | PURU             | Updated <a href="#">Functional Overview</a> :<br>Updated <a href="#">Select Input Decoding</a> (Added <a href="#">Figure 3</a> only, no edits).<br>Updated <a href="#">Zero Delay and Skew Control</a> (Minor edits).<br>Updated <a href="#">Package Diagrams</a> :<br>spec 51-85091 – Changed revision from *C to *D.<br>spec 51-85068 – Changed revision from *C to *E.<br>spec 51-85066 – Changed revision from *D to *E.                                                                                                                                                                                                                                                                                                                                         |

**Document History Page** *(continued)*

| Document Title: CY2305C/CY2309C, 3.3 V Zero Delay Clock Buffer<br>Document Number: 38-07672 |         |            |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|---------------------------------------------------------------------------------------------|---------|------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                        | ECN No. | Issue Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| *M                                                                                          | 4201564 | 11/25/2013 | CINM            | Updated <a href="#">Package Diagrams</a> :<br>spec 51-85066 – Changed revision from *E to *F.<br>Updated to new template.<br>Completing Sunset Review.                                                                                                                                                                                                                                                                                                                                      |
| *N                                                                                          | 4578443 | 11/25/2014 | TAVA            | Updated <a href="#">Functional Description</a> :<br>Added “For a complete list of related documentation, click <a href="#">here</a> .” at the end.<br>Updated <a href="#">Package Diagrams</a> .                                                                                                                                                                                                                                                                                            |
| *O                                                                                          | 5242528 | 04/15/2016 | SDHK / PSR      | Updated <a href="#">Electrical Characteristics</a> :<br>Updated details in “Test Conditions” column corresponding to $V_{OL}$ and $V_{OH}$ parameters.<br>Updated <a href="#">Electrical Characteristics</a> :<br>Updated details in “Test Conditions” column corresponding to $V_{OL}$ and $V_{OH}$ parameters.<br>Added <a href="#">Thermal Resistance</a> .<br>Updated <a href="#">Package Diagrams</a> :<br>spec 51-85066 – Changed revision from *F to *H.<br>Updated to new template. |
| *P                                                                                          | 5553658 | 12/14/2016 | TAVA            | Updated to new template.<br>Completing Sunset Review.                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| *Q                                                                                          | 5708829 | 04/27/2017 | AESATMP7        | Updated Cypress Logo and Copyright.                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

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